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UniPak 2™

10-950-0059 REV H **MAR 84**
Applies to configuration 950-0059-005

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NOTE

Before using the UniPak 2™, read section 1.2 for programmer mainframe compatibility information.

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SECTION 1
INTRODUCTION

1.1 OVERVIEW

Data I/O's UniPak 2™ reliably programs over 600 popular MOS and bipolar devices. Values for programming variables, including pinouts, voltage levels and timing, are stored in firmware tables. When you choose the family and pinout codes for a particular device, the programmer uses information in these tables to assemble a specialized programming routine in scratch RAM. This method allows high-speed operation with minimum firmware overhead. The UniPak 2™ is designed to adapt to the programming requirements of many different devices. Pinout variations are handled by seven device sockets on the UniPak 2™ and, in some cases, by adapters which connect to socket 1 or 2. Specially designed electronic switches allow programming of both bipolar and MOS devices.

To maximize control speed during programming, the UniPak 2™ makes extensive use of addressable latches for control signals. For flexibility in waveform generation, digital-to-analog converters (DACs) control all major power supplies, with several rise and fall times selected by firmware.

1.2 PROGRAMMER COMPATIBILITY

To be compatible with the UniPak 2™, your programmer may require a hardware and/or firmware update, depending on the model, configuration, and age. The information that follows will help you determine whether your programmer requires updating. If you find that your programmer does require updating, contact your nearest Data I/O Service Center.

- System 17—The System 17 must be converted into a System 19 with the latest firmware installed and latest hardware modifications.
- System 19—Check to determine whether your System 19 contains a 702-1520 or 702-1980 controller board by performing the following steps:

  1. Remove the programming pak (section 2.3).
  2. Remove the metal shield (if any) shown in figure 2-1.
  3. Count the number of EPROM firmware sockets located just behind the pak interface connector. If there are four sockets, it is a 702-1520 board. If there are eight sockets, it is a 702-1980 board.

MODIFICATION STATUS

1	2	3	4	5	6
●	0	0	0	0	0

Figure 1-1. Example of a "Modification Status" Sticker

If your System 19 contains a 702-1520 controller board, check the modification status sticker (figure 1-1) on the bottom of the programmer. If the sticker is not there or if only "1" is marked off, your System 19 requires hardware and firmware updating; contact the nearest Data I/O Service Center. If "2" is marked, your System 19 is compatible with the UniPak 2™. If your System 19 contains a 702-1980 controller board, it may require a firmware update. To display the configuration number of the firmware in your programmer, key in "SELECT-B2-START". If the configuration number displayed matches the number listed below, your firmware needs updating.

Model	Configuration Number
• 990-1902	3599
• 990-1903	CC8B

- 29A Universal Programmer—To be compatible with the UniPak 2™, the 29A programmers must have Rev C or later firmware. To determine the configuration of the firmware in your 29A, key in "SELECT-B2-START" and observe the display. If the hex number matches one listed in table 1-1, your firmware needs to be updated.
- 29B Universal Programmer—The UniPak 2™ is compatible with Rev A or later software.
- 100A Production Programmer—To be compatible with the UniPak 2™, the 100A programmers must have Rev E or later firmware. To determine the configuration of the firmware in your 100A, key in "SELECT-1Ø" and observe the display. If the hex number displayed matches one listed in table 1-1, your firmware needs to be updated.

Table 1-1. Programmer Compatibility

Model	Rev	Configuration Number
29A	A	1ECA
	B	20A4
29A (with computer remote control)	A	BB41
	B	C00B
100A	A	917F
	B	9405
	C	9DEE
	D	9BED

1.3 APPLICATIONS

Table A-1 (in appendix A) lists all the devices that could be programmed with the UniPak 2™ when this manual was published. In many cases when a new device with industry-standard pinout is introduced within a manufacturer's family, the UniPak 2™ WILL NOT require a revision to program it. For some new applications, such as to accommodate a new device family, a firmware update of the UniPak 2™ may be required. The revision number is stamped after the part number (950-0059) along the underside of the top edge of the UniPak 2™ socket assembly.

1.4 SPECIFICATIONS

The UniPak 2™ receives its power from the programmer mainframe. Programming waveforms are generated from raw programmer supplies using regulators controlled by the programmer's microprocessor. The controlling firmware is located on a circuit card within the UniPak 2™.

The physical and environmental specifications are:

- Altitude: Sea level to 3 km (10,000 ft.)
- Dimensions: 20.9 x 17.0 x 10.5 cm (8.2 x 6.7 x 4.2 in.)
- Humidity (operating): 90% maximum (noncondensing)
- Humidity (storage): 95% maximum (noncondensing)
- Temperature (operating): 0 to 40°C (32 to 104°F)
- Temperature (storage): −40 to 55°C (−40 to 131°F)
- Weight: 1.38 kg (3 lb. 0.5 oz.)

1.5 FIELD APPLICATION SUPPORT

Data I/O has field applications engineers (FAE's) throughout the world. They can provide additional information about interfacing Data I/O products with other equipment and answer questions about equipment. FAE's are located within the United States at the addresses listed in the back of this manual. For international applications support, contact your nearest Data I/O representative.

1.6 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period of one year, unless specified otherwise, begins when you receive the equipment. The warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O service center.

1.7 SERVICE

Data I/O maintains service centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. This includes not only repairs, but also calibration of all Data I/O products. A list of all Data I/O service centers is located in the back of this manual.

1.8 ORDERING

To order equipment, contact your Data I/O sales representative. Orders must contain the following information:

- Description of the equipment (see the latest Data I/O price list or contact your sales representative for equipment and part numbers)
- Quantity of each item ordered
- Shipping and billing address of firm, including ZIP code
- Name of person ordering equipment
- Purchase order number
- Desired method of shipment

SECTION 2
INSTALLATION

2.1 INSPECTION

Your UniPak 2™ was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should, therefore, arrive free of any defect, without marks or scratches, and in perfect operating condition. However, carefully inspect the instrument for any damage that may have occurred in transit. If you note any damage, file a claim with the carrier and notify Data I/O.

2.2 UniPak 2™ INSTALLATION

The UniPak 2™ may be installed and removed with the programmer's power on; this feature allows you to retain data in RAM during module changes. If the programmer power is turned on before the UniPak 2™ is installed, you will hear a beep until the UniPak 2™ is installed.

NOTE

Voltage transients can cause device damage. Thus, be sure that all sockets are empty when:

- *switching power on or off*

or

- *installing or removing the UniPak 2™*

To install the UniPak 2™, do the following:

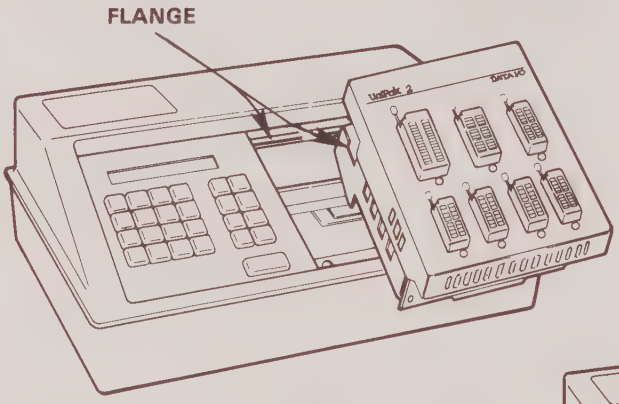
1. Slide the UniPak 2™ into the opening in the programmer (figure 2-1).
2. Tilt the UniPak 2™ up and gently push it back to hook the flange of the UniPak 2™ over the back edge of the programmer opening (figure 2-1, a).
3. Lower the UniPak 2™ into position as shown in figure 2-1, b.
4. Press gently on the front edge of the UniPak 2™ to ensure a good connection (figure 2-1, c).

2.3 UniPak 2™ REMOVAL

1. Check to make sure the programmer is not in the process of an operation. If it is, wait until the operation is complete (the action symbol on the display disappears).
2. Check to make sure a device is not in a socket. If one is in a socket, remove it as described in section 3.7.
3. Tilt the UniPak 2™ up and gently remove it from the programmer.

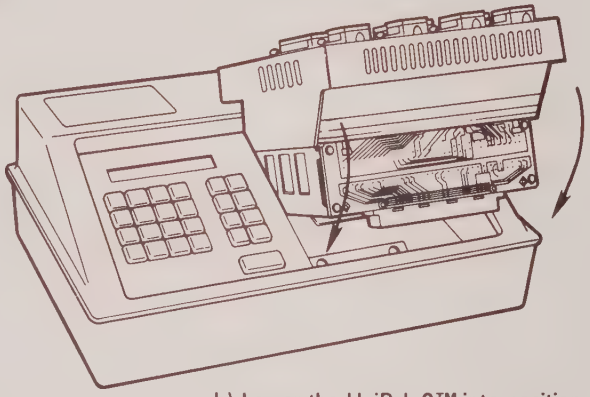
2.4 REPACKING FOR SHIPMENT

If the UniPak 2™ is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by part number, revision level, and name. If the original shipping container is to be used, place the UniPak 2™ in the container with the appropriate packing material and seal the container with strong tape. If another container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

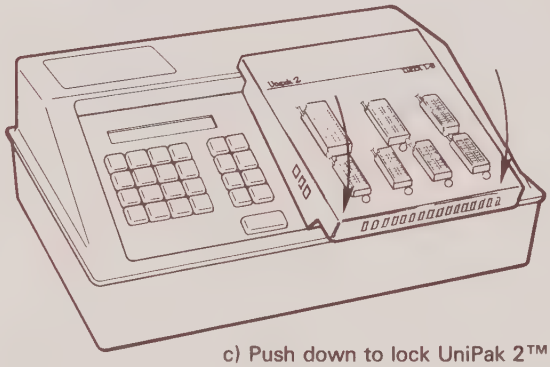


NOTE: Although the System 29A is shown here, the insertion procedure is the same for all systems.

a) Tip the UniPak 2™ up and back to lock flanges.



b) Lower the UniPak 2™ into position.



c) Push down to lock UniPak 2™ into place.

Figure 2-1. UniPak 2™ Installation

SECTION 3
OPERATION

3.1 OVERVIEW

The UniPak 2™ can be used in 29A, 29B, System 19, or 100A programmers of any configuration; see section 1.2 for firmware revision levels required. The typical programming operation with a 29A programmer and a UniPak 2™ is illustrated in figure 3-1. As can be seen from this figure, the UniPak 2™ can obtain data from three sources (a master device, a serial port, or the keyboard). Because the serial port and keyboard operations are unique for each type of programmer, you will be referred to your 29A, 29B, System 19, or 100A programmer manual for details on how to program using these mainframes.

When using a master device as the data source to program a blank device, you must first instruct the programmer to copy the device data into programmer RAM (shown as COPY in figure 3-1 and described in section 3.4). Then enter the family code and pinout code as described in section 3.6. The data in the device will have been copied to the RAM of your 29A when you press START, as shown in figure 3-1. You must then remove the master device and instruct the programmer to copy the information just stored in its RAM to a blank device. This completes the basic programming operation.

The procedures to perform basic operations with your UniPak 2™ are described in this section. You should follow these procedures to properly operate your UniPak 2™. Wherever possible, key sequences have been included for using your UniPak 2™ with a 29A Universal Programmer with Rev C firmware (read section 1.2 carefully to determine your programmer's firmware revision level). Refer to your programmer manual for key sequences for the System 19, 29B, and 100A programmers.

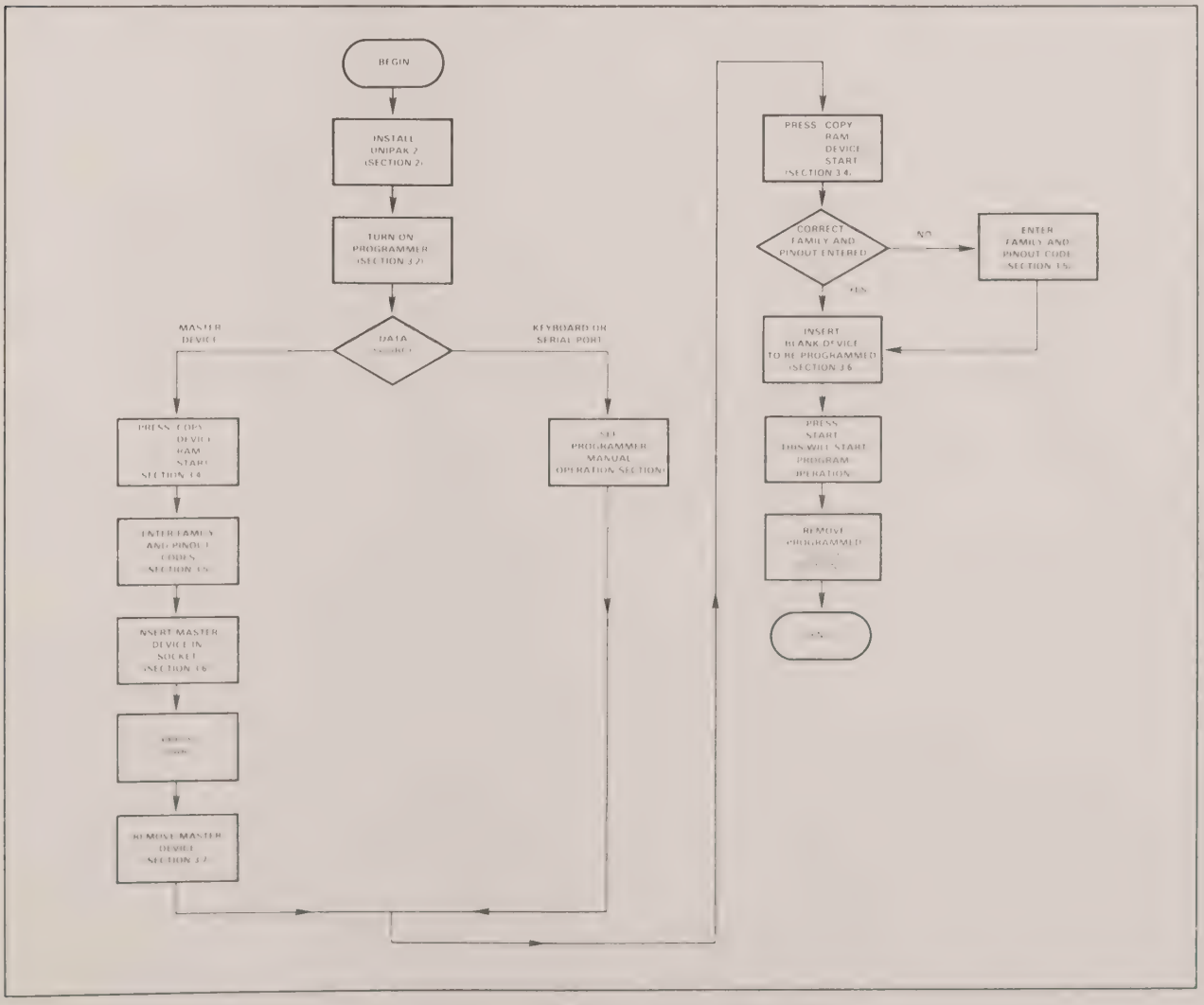


Figure 3-1. Typical 29A Programmer Operation

3.2 POWER UP

NOTE

If the UniPak 2™ is not installed in the programmer before power is turned on, you will hear a beep until the UniPak 2™ is installed.

When turned on, the programmer will perform an automatic self-test routine. When the self-test routine is complete, the programmer will signal its readiness.

To turn the programmer on, do the following:

1. Check to make sure a device is not in a socket. If a device is in a socket, lift up the lever (located on the upper left of the socket; see section 3.8), then gently lift the device out of the socket.
2. Plug the AC power cord into the power outlet.
3. Flip the power switch up to the "ON" position (see figure 3-2).

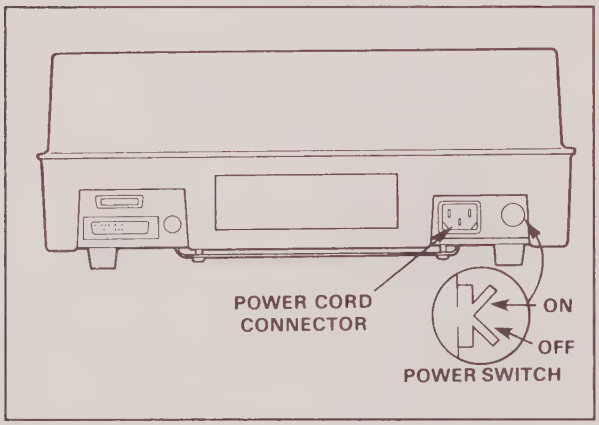


Figure 3-2. Programmer Power Switch Location

3.3 POWER DOWN

CAUTION

Do not turn the power off while the programmer is doing an operation or when a device is in a socket; voltage transients may damage the device.

To turn the programmer power off, do the following procedure:

1. Check to make sure that the programmer is not in the middle of an operation. If it is, wait until that operation is through.
2. Check to make sure a device is not in a socket. If a device is in a socket, remove it as described in section 3.8.
3. Flip the power switch down to the "OFF" position (figure 3-2).

3.4 BASIC OPERATION

All data transfer or verification operations take place between the programmer's internal RAM and the device or between the RAM and serial port in your programmer. Because the procedure to transfer data via a serial port varies from programmer to programmer, this manual describes only data transfer with the 29A. For other programmers, refer to your programmer operation manual.

The basic data transfer operations that can be performed with the UniPak 2™ and the 29A Universal Programmer are:

- Load RAM with data from a master device (described in section 3.4.1).
- Verify RAM data against the device data (described in section 3.4.2).
- Program a device with RAM data (described in section 3.4.3).

3.4.1 Load RAM With Data From Master Device

To load the 29A RAM with data from a master device, follow the steps listed below.

1. Press COPY; 29A displays COPY DATA FROM
2. Press DEVICE; 29A displays DEV ∧ ADDR/SIZE TO

NOTE
The device is the source of data.

3. Press RAM; 29A displays CO DEV > RAM ∧ ADDR

NOTE
The RAM is the destination of the data from the master device.

4. Press START; 29A displays FAM ∧ ØØ PIN ØØ
5. Enter the family code and pinout code (see section 3.6).
6. Insert the master device into the UniPak 2™ (see section 3.7).
7. Press START; 29A displays LOADING DEVICE
   LOAD DONE XXXX

NOTE
XXXX is the sumcheck of the device.

8. Remove the master device from the UniPak 2™ (see section 3.8).

During source destination operations (copy and verify), ADDR and SIZE appear in the 29A prompts. These correspond to starting address and block size, respectively. For more detail on these parameters, see your programmer operation manual. When reading a device, the UniPak 2™ applies a nominal V_{CC} level. To simulate loading on device outputs, each output is driven by a 1.6 mA current source.

3.4.2 Verify RAM Data Against Master Device Data

The two-pass verify consists of comparing the device data to RAM data and is performed at two V_{CC} levels; these levels, plus the output-sink currents and the output-level-sense voltages, vary according to each manufacturer's requirements.

To verify that data entered in the 29A RAM duplicate the master device data, follow these steps:

1. Press VERIFY; 29A displays VERIFY DATA FROM
2. Press DEVICE; 29A displays DEV ∧ ADDR/SIZE TO

NOTE
The device is the source of data.

3. Press RAM; 29A displays VE DEV > RAM ∧ ADDR

NOTE
The RAM is the destination of the data from the master device.

4. Press START; 29A displays FAM ØØ PIN ØØ
5. Enter the family code and pinout code (see section 3.6).
6. Insert the master device into the UniPak 2™ (see section 3.7).
7. Press START; 29A displays VERIFY DEVICE
   VE DEV DONE XXXX

NOTE
XXXX is the sumcheck of the device.

8. Remove the master device from the UniPak 2™ (see section 3-8).

3.4.3 Program Device With RAM Data

When programming a device, the system performs illegal-bit tests and blank checks at nominal V_{CC} and with nominal output loading.

To program a blank device with the data in the 29A RAM, follow these steps:

1. Press COPY; 29A displays COPY DATA FROM
2. Press RAM; 29A displays RAM ∧ ADDR/SIZE TO
3. Press DEVICE; 29A displays CO RAM > DEV ∧ ADDR
4. Press START; 29A displays FAM ∧ ØØ PIN ØØ
5. Enter the family code and pinout code (see section 3-6).
6. Insert the blank device into the UniPak 2™ (see section 3-7).
7. Press START; 29A displays TEST DEVICE
   PROGRAM DEVICE
   VERIFY DEVICE
   PRG DONE Ø1 XXXX
8. Remove the device from the UniPak 2™ (see section 3.8).

NOTE
XXXX represents the sumcheck of the device.

3.4.4 Extended Select Functions

In addition to the three basic source-destination functions (copy, verify and edit) and the select functions described in the Operation section of your programmer manual, the UniPak 2™ offers eight extended select functions (BC, BD, C3, CC, CD, CE, CF and EF). These functions are not required for normal operation of the UniPak 2™.

Functions BC and BD are used to disable and enable the electronic identifier function for device families listed in section 3.5, with the exception of family FF.

To disable the electronic identifier test (BC), follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press BC START; 29A displays SELECT CODE **

To enable the electronic identifier test (BD), follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2 Press BD START; 29A displays SELECT CODE **

Function C3 gives access to options for specific family/pinout code combinations. If the UniPak 2™ is being used in a Model 19, this select code will work only from terminal remote.

To enter the options, follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press C3 START; 29A displays FXX PYY OPTIONS
3. Press START; 29A displays "NAME OF FIRST OPTION"

To select different options, press the REVIEW key. To execute an option, press START (in terminal remote, the RETURN key is used for the START key, and the space bar is used for the REVIEW key). If the option has subheadings under it, once the START key has been pressed, the REVIEW key can select the desired subheading. The START key is then pressed to execute the subheading. Once an option has been completely executed, an asterisk will be displayed after the option name. Complete execution may require doing a number of subheadings. Pressing the START key a second time after an option is completely executed will exit the options file, and the 29A will display OPTIONS DONE **.

NOTE

For the 8751H, the option "PROG SECTY ONLY" will program the security fuse as soon as the option is selected and executed.

Functions CC and CD are used in conjunction with electronic identifiers and may be used from the keyboard or from remote control.

Function CC displays the family and pinout codes of the last algorithm moved to RAM, usually the algorithm for the last device programmed or read. This function helps determine the family and pinout codes used by the programmer when in the automatic electronic identifier mode.

Function CD displays in hexadecimal 16 bytes of the device's electronic identifier. Byte Ø identifies the manufacturer; byte 1 identifies the device. For information on the purpose of the remaining bytes, consult the device data sheets.

To display the family and pinout codes of the last algorithm moved to RAM, follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CC START; 29 A displays XXYY **

NOTE

XX represents the family code; YY represents the pinout code.

To display the electronic identifier, proceed as follows:

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CD START; 29A displays 0000 YY
3. To display additional bytes of electronic identifier, press START; 29A displays 000X YY. To back up through previously displayed identifiers, press REVIEW; 29A displays 000X YY

NOTE

000X represents the byte number of the identifier displayed (i.e., 0001 represents byte 1 of the electronic identifier which is the device code). YY represents the identifier byte in hexadecimal.

Functions CE and CF are used to set the reject count (the number of programming pulses applied to a fuse or cell before it is rejected); CE sets the reject count back to the commercial specification (this is the default value) and CF sets the single-pulse reject count. This feature was accomplished in older UniPak™ models by adding 50 to the family code).

To select the commercial (default) reject count (CE), follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CE START; 29A displays SELECT CODE **

To select the single-pulse reject count (CF), take the following steps:

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CF START; 29A displays SELECT CODE **

Function EF calls up a four-digit hexadecimal configuration number and a two-digit decimal version number that correspond to the revision level and version number of the UniPak 2™ firmware. This function can be useful to identify firmware revision levels when communicating with Data I/O regarding field bulletins and updates.

To display the UniPak 2™ firmware configuration and version number, do the following:

1. Press SELECT; 29A displays SELECT CODE ^
2. Press EF START; 29A displays XXXX YY **

NOTE

XXXX represents the UniPak 2™ firmware configuration number, and YY represents the version number.

3.5 ELECTRONIC IDENTIFIERS

This version of the UniPak 2 ™ can read and use electronic identifiers in two modes.

The first mode occurs when family code 79, 93, 27, A5, BF, C5, AB, AF, C1, DD, or 45 is selected. The identifier is read and used to prohibit programming a device using the wrong family and pinout codes. The new low Vpp devices are protected from the old high Vpp algorithms which might destroy them. Older devices without signatures are permitted to program. An error will occur if you attempt to program using the wrong family or pinout codes.

The second mode is automatic. It is selected by entering family and pinout codes FF/FF. In this mode the operator need not look up any family or pinout codes; the electronic identifier is read and the correct algorithm is used for each device. An error will occur if you attempt to program on older devices without electronic identifiers or on newer devices whose identifiers are not yet supported.

3.6 FAMILY CODE AND PINOUT CODE SELECTION

Any device that can be programmed with the UniPak 2™ is specified by a unique combination of a two-digit family code and a two-digit pinout code (table A-1). Once the codes for a particular device are entered, the UniPak 2™ remains set up for any operation with that device until new codes are entered.

Your programmer manual will tell you where in the key sequence the family and pinout codes should be entered. If invalid family and pinout codes are entered, a beep will sound as either START or ENTER is pressed, or Err 30 (error 30) will be displayed and the operation will be aborted.

To select the family and pinout codes, do the following procedure:

1. Locate the manufacturer name and part number stamped on the device.
2. Turn to table A-1, Family and Pinout Codes, in appendix A, and find the same manufacturer name.
3. Then, in the first column (Device Part Number), find the number which corresponds to the part number stamped on the device.
4. Move to columns two and three, entitled Family and Pinout Codes, to find the numbers on the same line as the particular device number.
5. Enter these selected family and pinout code numbers.
6. Press "START."

NOTE

An LED (light-emitting diode) will light under one of the sockets.

Valid family and pinout codes must be in effect to use the System 19 DEVICE DATA key. When you press the DEVICE DATA key, either nominal, first-pass, or second-pass verify level is applied to the device. The level applied depends on the System 19's position in executing the selected mode. If the KEYBD light is on, the nominal verify level is applied.

3.7 DEVICE INSERTION

Once you have chosen the appropriate family and pinout codes, the UniPak 2™ is ready to accept a device in the socket located above the lighted LED.

NOTE

In the automatic electronic identifier mode, no LED is lighted unless UniPak 2™ is performing an operation on a device. An empty socket will always be unlighted. In this mode, disregard any reference to lighted LEDs; use the socket with the correct number of pins.

A good electrical connection between the device and the socket is essential. To ensure a good connection, do the following:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift up the lever on the upper left side of the socket above the lighted LED; see figure 3-3. (The lever will stay locked into the upright position.)
3. Gently insert the device in the socket above the lighted LED. Make sure pin 1 of the device is aligned with pin 1 of the socket, as shown in figure 3-3.
4. Push the lever down to lock the device in the socket.

Once the family and pinout codes have been entered, the UniPak 2™ is ready for device-related operations. The key sequence to load, program, and verify are described in the Operation section of your programmer manual.

3.8 DEVICE REMOVAL

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift up the lever on the left side of the socket; see figure 3-3. (The lever will lock into the upright position.)
3. Lift the device out of the socket; the LED will remain illuminated.

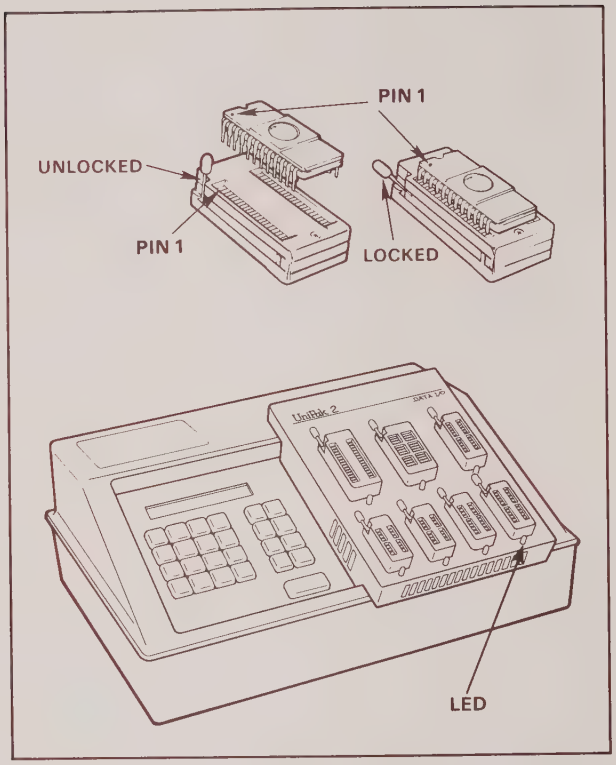


Figure 3-3. UniPak 2™ Sockets and Device Installation

APPENDIX A
FAMILY AND PINOUT CODES
ERROR CODES

Table A-1. UniPak 2™ Family and Pinout Codes

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Advanced Micro Devices					
2708	21	27	003	-	A
27128	AF	51	V04	-	A
27128A	C1	51	V05	-	A
2716	19	23	003	-	A
27256	C1	32	VO5	-	S
2732	19	24	003	-	A
2732A	27	24	003	-	A
27512	DD	A4	VO5	-	A
2764	AF	33	V04	-	A
2764A	C1	33	VO5	-	A
27LS18	16	02	003	-	A
27LS185	16	06	003	-	A
27LS19	16	02	003	-	A
27PS181	16	37	003	-	A
27PS184	16	06	003	-	A
27PS185	16	06	003	-	A
27PS191	16	68	003	-	A
27PS281	16	37	003	-	A
27PS291	16	68	003	-	A
27PS41	16	53	003	-	A
27PS43	16	63	V03	-	A
27PS49	16	67	003	-	A
27S08	15	02	003	-	O
27S09	15	02	003	-	O
27S10	15	01	003	-	O
27S12	16	03	V03	-	A
27S13	16	03	V03	-	A
27S15	16	79	V04	351A-068	A
27S18	16	02	V03	-	A
27S180	16	37	V03	-	A
27S181	16	37	V03	-	A
27S184	16	06	V03	-	A
27S185	16	06	V03	-	A
27S19	16	02	V03	-	A
27S190	16	68	V03	-	A
27S191	16	68	V03	-	A
27S20	16	01	V03	-	A
27S21	16	01	V03	-	A
27S24	16	65	V03	-	A
27S25	16	65	V03	-	A
27S26	16	85	V04	351A-067	A
27S27	16	85	V04	351A-067	A
27S28	16	09	V03	-	A
27S280	16	37	V03	-	A
27S281	16	37	V03	-	A
27S29	16	09	V03	-	A
27S290	16	68	V03	-	A
27S291	16	68	V03	-	A
27S30	16	36	V03	-	A
27S31	16	36	V03	-	A
27S32	16	38	V03	-	A
27S33	16	38	V03	-	A
27S35	16	66	V03	-	A
27S37	16	66	V03	-	A
27S40	16	53	V03	-	A
27S41	16	53	V03	-	A
27S43	16	63	V03	-	A
27S45	16	77	V04	351A-066	A
27S47	16	77	V04	351A-066	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Advanced Micro Devices (Continued)					
27S49	16	67	003	-	A
27S65	16	93	V05	351A-073	A
27S75	16	94	V05	351A-073	A
27S85	16	95	VO5	351A-073	A
2864	C9	A6	VO5	-	A
29750A	16	02	003	-	A
29751A	16	02	V03	-	O
29760A	16	01	V03	-	A
29761A	16	01	V03	-	O
29770	16	03	V03	-	O
29771	16	03	V03	-	O
29774	16	85	V04	351A-067	S
29775	16	85	V04	351A-067	S
AM9708	21	27	003	-	A
AM9716	19	23	003	-	A
AM9732	19	24	003	-	A
AM9764	AF	33	V04	-	A
Electronic Arrays					
2708	21	27	003	-	S
2716	19	23	003	-	S
Eurotechnique					
ET2716	19	23	V04	-	A
ET2732	19	24	V04	-	A
ETC2716	19	23	V04	-	A
ET2764	35	33	V05	-	S
Fairchild					
2708	21	27	003	-	A
93417	01	01	003	-	A
93427	01	01	003	-	A
93436	01	03	003	-	A
93438	01	15	003	-	A
93446	01	03	003	-	A
93448	01	15	003	-	A
93450	01	16	003	-	A
93451	01	16	003	-	A
93452	01	05	003	-	A
93453	01	05	003	-	A
93460	01	16	003	-	A
93461	01	16	003	-	A
93510	01	21	003	-	A
93511	01	21	003	-	A
93514	01	06	003	-	A
93515	01	06	003	-	A
93L450	01	16	003	-	A
93L451	01	16	003	-	A
93Z450	A4	16	VO4	-	A
93Z451	A4	16	VO4	-	A
93Z510	A4	21	VO4	-	A
93Z511	A4	21	VO4	-	A
93Z564	A4	67	VO5	-	S
93Z565	A4	67	VO5	-	S
Fujitsu					
27128	45	51	V04	-	S
2732A	27	24	003	-	S
2732A-35	27	24	003	-	S
2764	45	33	V04	-	S
27C128	45	51	V04	-	S
27C256	45	32	VO5	-	S

Table A-1. UniPak 2™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Fujitsu (Continued)					
27C32A	27	24	003	-	S
27C64	45	33	V04	-	S
7051	78	02	003	-	A
7052	78	01	003	-	A
7053	78	03	003	-	A
7054	78	05	003	-	A
7055	78	69	003	-	A
7056	78	02	003	-	A
7057	78	01	003	-	A
7058	78	03	003	-	A
7059	78	05	003	-	A
7060	78	69	003	-	A
7111	68	02	003	-	A
7112	68	02	003	-	A
7113	68	01	003	-	A
7114	68	01	003	-	A
7115	68	03	003	-	A
7116	68	03	003	-	A
7117	68	08	003	-	A
7118	68	08	003	-	A
7119	68	14	003	-	A
7120	68	14	003	-	A
7121	68	05	003	-	A
7122	68	05	003	-	A
7123	68	09	003	-	A
7124	68	09	003	-	A
7125	68	15	003	-	A
7126	68	15	003	-	A
7127	68	06	003	-	A
7128	68	06	003	-	A
7131	68	16	003		A
7132	68	16	003	-	A
7137	68	21	003	-	A
7138	68	21	003	-	A
7141	68	63	003	-	A
7142	68	63	003	-	A
7143	68	67	003	-	A
7144	68	67	003	-	A
7151	68	53	003	-	S
7152	68	53	003		S
7225LA	68	15	VO5	-	S
7226LA	68	15	VO5	-	S
7231LA	68	16	VO5	-	S
7232LA	68	16	VO5	-	S
7237LA	68	21	VO5	-	S
7238LA	68	21	VO5	-	S
7241LA	68	63	VO5	-	S
7242LA	68	63	VO5		S
8516	19	23	003		S
8518	21	27	003		S
8532	19	24	003		S
8742	50	57	004	351A-070	S
8749H	50	57	004	351A-070	S
General Instruments					
5716	83	23	003		A
5816	37	23	003		A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Harris					
6616	88	75	VO5	-	S
6641	40	47	003	-	A
7602	05	02	V04	-	S
7603	05	02	V04	-	S
7608	05	16	003	-	A
7610	05	01	003	-	A
7611	05	01	003	-	A
7616	05	42	003	-	A
76160	05	21	003	-	O
76161	05	21	003	-	A
76165	05	53	003	-	A
7620	05	03	003	-	A
7621	05	03	003	-	A
7629	05	43	003	-	O
76320	05	63	003	-	O
76321	05	63	003	-	A
7640	05	15	003	-	A
7641	05	15	003	-	A
7642	05	05	003	-	A
7642P	05	38	003	-	O
7643	05	05	003	-	A
7643P	05	38	003		O
7644	05	04	003	-	O
7647R	05	79	VO5	351A-068	S
7648	05	09	003	-	A
7649	05	09	003	-	A
76641	05	67	003	-	A
7680	05	16	003		A
7680RP	05	16	003	-	O
7681	05	16	003		A
7681RP	05	16	003		O
7684	05	06	003	-	A
7684P	05	06	003	-	O
7685	05	06	003		A
7685P	05	06	003	-	O
7686	05	10	A		A
7687	05	10	VO1		A
Hitachi					
25044	74	05	003		O
25045	74	05	003		O
25084	74	06	003		O
25084S	66	06	003		O
25085	74	06	003		O
25085S	66	06	003		O
25088	74	16	003		O
25088S	66	16	003		O
25089	74	16	003		O
25089S	66	16	003		O
25168	74	21	003		O
25168S	66	21	003		O
25169	74	21	003		O
25169S	66	21	003		O
27C32	19	24	003		O
27C32A	27	24	003		O
462532	19	25	003		A
462716	19	23	003		A
462732	19	24	003		A
462732P	19	24	003		S

Table A-1. UniPak 2™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Hitachi (Continued)					
48016	33	23	003	-	A
4827128	79	51	003	-	A
482732A	27	24	003	-	A
482764	79	33	003	-	A
Hughes					
3004-1	58	62	V04	-	S
3004-2	58	61	V04	-	S
3008	58	60	V04	-	S
3704-1	58	62	V04	-	S
3704-2	58	61	V04	-	S
3708	58	60	V04	-	S
Intel					
2704	21	26	003	-	A
2708	21	27	003		A
27128	79	51	003	-	A
27128A	93	51	V04	-	A
2716	19	23	003	-	A
27256	93	32	V04	-	A
2732	19	24	003	-	A
2732A	27	24	003	-	A
2758	19	22	003	-	A
2764	79	33	003	-	A
2764A	93	33	V04	-	A
2815	86	23	003	-	A
2816	37	23	003	-	A
2816A	A5	96	VO5	-	S
2817A	BF	A2	VO5	-	S
3628	75	16	003		A
3628A	75	16	003	-	A
3632	75	63	003	-	A
3636	75	21	003	-	A
3636B	75	21	003	-	A
82HS181	75	16	003	-	A
82HS191	75	21	003	-	A
82HS321	75	63	003	-	A
82S181	75	16	003	-	A
82S191	75	21	003	-	A
82S321	75	63	003	-	A
8704	21	26	003	-	A
8708	21	27	003	-	A
8741	56	59	V04	351A-070	S
8741A	56	59	V04	351A-070	S
8742	50	57	V05	351A-070	S
8744	53	58	V05	351A-071	S
8748	52	56	V04	351A-070	A
8748H	50	56	V04	351A-070	A
8749H	50	57	V04	351A-070	A
8751	53	58	V04	351A-071	A
8751H	D5	58	VO5	351A-071	S
8755A	47	55	V04	351A-072	S
Intersil					
5600	D4	02	VO5	-	O
5603A	70	01	003	-	A
5604	70	03	003	-	A
5610	D4	02	VO5	-	O
5623	70	01	003	-	A
5624	70	03	003	-	A
6716	59	64	003	-	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Mitsubishi					
2708	21	27	003	-	A
27128	79	51	003	-	A
2716	19	23	003	-	A
2732	19	24	003	-	A
2732A	27	24	003	-	A
2764	79	33	003	-	A
54700A	B5	01	V05	-	A
54701A	B5	01	V05	-	A
54730A	B5	02	V05	-	A
54731A	B5	02	V05	-	A
54740A	B5	05	V05	-	A
54741A	B5	05	V05	-	A
8748	52	56	VO5	-	S
Monolithic Memories					
5300	11	01	003	-	A
5301	11	01	003	-	A
5305	11	03	003	-	A
5306	11	03	003	-	A
5308	D1	08	003	-	A
5309	D1	08	003	-	A
5330	29	02	003	-	A
5331	29	02	003	-	A
5335	D1	14	003	-	A
5336	D1	14	003	-	A
5340	D1	15	003	-	A
5340JS	D1	15	003	-	A
5341	D1	15	003	-	A
5341JS	D1	15	003	-	A
5348	D1	09	003	-	A
5349	D1	09	003	-	A
5352	D1	05	003	-	A
5353	D1	05	003	-	A
5380	D1	16	003	-	A
5380JS	D1	16	003	-	A
5381	D1	16	003	-	A
5381JS	D1	16	003	-	A
5388	D1	06	003	-	A
5389	D1	06	003	-	A
53LS080	18	02	003	-	O
53LS081	18	02	003	-	O
53S080	18	02	003	-	O
53S081	18	02	003	-	O
6300	11	01	003	-	A
6301	11	01	003	-	A
6305	11	03	003	-	A
6306	11	03	003	-	A
6308	D1	08	003	-	A
6309	D1	08	003	-	A
6330	29	02	003	-	A
6331	29	02	003	-	A
6335	D1	14	003	-	A
6336	D1	14	003	-	A
6340	D1	15	003	-	A
6340JS	D1	15	003	-	A
6341	D1	15	003	-	A
6341JS	D1	15	003	-	A
6348	D1	09	003	-	A
6349	D1	09	003	-	A

Table A-1. UniPak 2™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Monolithic Memories (Continued)					
6352	D1	05	003	-	A
6353	D1	05	003	-	A
6380	D1	16	003		A
6380JS	D1	16	003	-	A
6381	D1	16	003	-	A
6381JS	D1	16	003	-	A
6388	D1	06	003	-	A
6389	D1	06	003	-	A
63D1641	B2	80	VO5	351A-073	A
63D1642	B2	80	VO5	351A-073	A
63DA1643	AA	87	VO5	351A-073	A
63DA441	AA	AC	VO5	351A-073	A
63DA841	AA	AD	VO5	351A-073	A
63DS1643	AA	87	VO5	351A-073	A
63LS080	18	02	003	-	A
63LS081	18	02	003		A
63LS140	18	01	003	-	A
63LS141	18	01	003	-	A
63LS240	18	03	003	-	A
63LS241	18	03	003	-	A
63LS441	18	05	003	-	A
63PL1681	18	21	VO5		S
63PS1681	18	21	VO5	-	A
63RA1681	18	A3	VO5	-	A
63RA441	18	07	V04	-	A
63RS1681	18	A3	V05	-	A
63RS441	18	07	003	-	A
63RS881	18	86	V04	-	A
63S080	18	02	003		A
63S081	18	02	003		A
63S140	18	01	003	-	A
63S141	18	01	003	-	A
63S1640	18	53	003	-	A
63S1641	18	53	003		A
63S1680	18	21	003	-	A
63S1681	18	21	003	-	A
63S1681J	18	21	003		A
63S240	18	03	003		A
63S241	18	03	003		A
63S3281	18	63	V03	-	A
63S440	18	05	003	-	A
63S441	18	05	003	-	A
63S480	18	09	003	-	A
63S481	18	09	003		A
63S840	18	06	003	-	A
63S841	18	06	003	-	A
Mostek					
2716	19	23	VO3		A
Motorola					
68732-0	25	44	003	-	O
68732-1	25	45	003	-	O
76161	05	21	003		A
76165	05	53	003		S
7620	05	03	003		O
7621	05	03	003		A
7640	05	15	003		O
7641	05	15	003		A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Motorola (Continued					
7642	05	05	003	-	O
7643	05	05	003	-	A
7649	05	09	003	-	S
7680	05	16	003	-	O
7681	05	16	003	-	A
7684	05	06	003	-	O
7685	05	06	003	-	A
MCM2532	19	25	003		A
MCM2708P	21	27	003	-	O
MCM2716	19	23	003	-	A
MCM2808	81	72	003	-	A
MCM2816	43	23	003	-	A
MCM2817	81	71	003	-	A
MCM2832	81	70	003		A
MCM68708	21	27	003	-	A
MCM68764	25	29	003	-	A
MCM68766	25	29	003	-	A
TMS2716	23	28	003	-	A
National Semiconductor					
2532	19	25	003	-	A
25C32	19	25	003	-	A
2708	21	27	003	-	A
2716	19	23	003	-	A
2732	19	24	003	-	A
2758A	19	22	003	-	A
2758B	19	35	VO3	-	A
2764	35	33	003	-	S
2764H	63	33	V05		S
27C16	19	23	003	-	A
27C16H	BD	23	V05	-	S
27C32	19	24	003	-	A
27C32H	BD	24	V05	-	S
2816	37	23	003		A
54LS471	08	08	003		O
54S188	08	02	003	-	O
54S287	08	01	003	-	O
54S288	08	02	003		O
54S387	08	01	003		O
54S471	08	08	003		O
54S472	08	09	003	-	O
54S473	08	09	003	-	O
54S474	08	15	V03		A
54S475	08	15	V03	-	A
54S570	08	03	003		O
54S571	08	03	003		O
54S572	08	05	003		O
54S573	08	05	003		O
74LS471	08	08	003		A
74S188	08	02	003		A
74S287	08	01	003		A
74S288	08	02	003		A
74S387	08	01	003	-	A
74S471	08	08	003		A
74S472	08	09	003		A
74S473	08	09	003		A
74S474	08	15	003		A
74S475	08	15	VO3		A
74S570	08	03	003		A

Table A-1. UniPak 2™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
National Semiconductor (Continued)					
74S571	08	03	003	-	A
74S572	08	05	003	-	A
74S573	08	05	003	-	A
74S574	08	34	003	-	A
77LS181	08	16	V03	-	A
77S180	08	16	V03	-	A
77S184	08	06	V03	-	A
77S185	08	06	V03	-	A
87LS181	08	16	003	-	A
87S180	08	16	003	-	A
87S181	08	16	003	-	A
87S184	08	06	003	-	A
87S185	08	06	003	-	A
87S190	08	21	003	-	A
87S191	08	21	003	-	A
87S195	08	53	003	-	A
87S280	08	16	003	-	A
87S281	08	16	003	-	A
87S290	08	21	003	-	A
87S291	08	21	003	-	A
87S295	08	15	003	-	A
87S296	08	15	003	-	A
87S321	08	63	003	-	A
87SR181	08	66	VO5	-	A
87SR25	08	81	V04	-	A
87SR474	08	81	VO5	-	A
9716	B3	23	V04	-	A
Nippon Electric Company, Ltd.					
27128	79	51	VO5	-	A
2716	19	23	003	-	A
2732	19	24	003	-	A
2732A	27	24	003	-	A
2764	79	33	003	-	A
8741AD	56	59	V04	351A-070	S
8748AD	52	56	V04	351A-070	S
8755A	47	55	V04	351A-072	S
B403	72	01	003	-	A
B405	72	15	003	-	A
B406	72	05	003	-	A
B408	72	16	003	-	A
B409	72	21	003	-	A
B417	72	16	003	-	A
B419	72	42	003	-	A
B423	72	01	003	-	A
B425	72	15	003	-	A
B426	72	05	003	-	A
B428	72	16	003	-	A
B429	72	21	003	-	A
Oki					
2532	19	25	003	-	S
2708	21	27	003	-	A
27128	79	51	003	-	S
2716	19	23	003	-	A
2732	19	24	003	-	S
2732A	27	24	003	-	S
2758	19	22	003	-	A
2764	79	33	003	-	A
8755A	47	55	004	351A-072	S

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Raytheon					
29600	11	08	003	-	A
29601	11	08	003	-	A
29602	11	08	003	-	A
29603	11	08	003	-	A
29610	11	03	003	-	A
29611	11	03	003	-	A
29612	11	03	003	-	A
29613	11	03	003	-	A
29620	11	09	003	-	A
29621	11	09	003	-	A
29622	11	09	003	-	A
29623	11	09	003	-	A
29624	11	15	003	-	A
29625	11	15	003	-	A
29626	11	15	003	-	A
29627	11	15	003	-	A
29630	11	16	003	-	A
29630SM	11	16	003	-	A
29631	11	16	003	-	A
29631SM	11	16	003	-	A
29632	11	16	003	-	A
29632SM	11	16	003	-	A
29633	11	16	003	-	A
29633SM	11	16	003	-	A
29634	11	16	003	-	A
29635	11	16	003	-	A
29636	11	16	003	-	A
29637	11	16	003	-	A
29640	11	53	003	-	A
29641	11	53	003	-	A
29642	11	53	003	-	A
29643	11	53	003	-	A
29650	11	06	003	-	A
29651	11	06	003	-	A
29652	11	06	003	-	A
29653	11	06	003	-	A
29660	11	01	003	-	A
29661	11	01	003	-	A
29662	11	01	003	-	A
29663	11	01	003	-	A
29671	11	63	003	-	A
29673	11	63	003	-	A
29680	11	21	003	-	A
29680SM	11	21	003	-	A
29681	11	21	003	-	A
29681SM	11	21	003	-	A
29682	11	21	003	-	A
29682SM	11	21	003	-	A
29683	11	21	003	-	A
29683SM	11	21	003	-	A
Ricoh					
RD5H32	27	24	003	-	S
Rockwell					
R87C32	27	24	V05	-	S
Seeq					
27C256	93	32	V05	-	S
5133	79	33	VO4	-	A

Table A-1. UniPak 2™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Seeq (Continued)					
5133H	79	33	VO4	-	A
5143	79	51	VO4	-	A
5213	A5	96	V04	-	A
5213H	B9	96	V05	-	A
52B13	A5	96	004	-	A
52B13H	B9	96	V05	-	A
52B23	AB	97	VO5	-	A
52B23H	AB	97	VO5	-	A
52B33	AB	98	VO5	-	A
52B33H	AB	98	VO5	-	A
SGS Technology					
2532	19	25	002	-	A
2716	19	23	003	-	A
2764	35	33	V05	-	A
Signetics					
2708	21	27	003	-	A
82123	10	02	003	-	A
82LS135	10	08	003	-	A
82LS137	10	05	003	-	A
82LS180	10	16	003	-	A
82LS181	10	16	003	-	A
82PS180	10	16	003	-	A
82PS181	10	16	003	-	A
82S123	10	02	003	-	A
82S126	10	01	003	-	A
82S129	10	01	003	-	A
82S130	10	03	003	-	A
82S131	10	03	003	-	A
82S135	10	08	003	-	A
82S136	10	05	003	-	A
82S137	10	05	003	-	A
82S140	10	15	003	-	A
82S141	10	15	003	-	A
82S146	10	09	003	-	A
82S147	10	09	003	-	A
82S180	10	16	003	-	A
82S181	10	16	003	-	A
82S182	10	16	003	-	A
82S183	10	16	003	-	A
82S184	10	06	003	-	A
82S185	10	06	003	-	A
82S190	10	21	003	-	A
82S191	10	21	003	-	A
82S195	10	53	003	-	A
82S23	10	02	003	-	A
82S2708	10	16	003	-	A
82S321	10	63	003	-	A
Synertek					
2716	19	23	003	-	A
Thompson					
71190	92	21	003	-	S
71191	92	21	003	-	S
Texas Instruments					
24S10	13	01	003	-	A
24S166	13	53	003	-	A
24S41	13	38	003	-	A
24S81	13	06	003	-	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Texas Instruments (Continued)					
24SA10	13	01	003	-	A
24SA166	13	53	003	-	A
24SA41	13	38	003	-	A
24SA81	13	06	003	-	A
2508	19	22	003	-	A
2516	BD	23	V05	-	A
2532	BD	25	V05	-	A
2564	BD	30	V05	-	A
25L32	19	25	003	-	A
2708	21	27	003	-	A
27128	79	51	V03	-	S
2732	BD	24	V05	-	A
2732A	63	24	V05	-	A
2764	79	33	003	-	A
27L08	21	27	003	-	A
28L166	13	21	003	-	A
28L22	13	46	003	-	A
28L42	13	09	003	-	A
28L45	13	15	003	-	A
28L85	13	16	003	-	A
28L86	13	16	003	-	A
28LA22	13	46	003	-	A
28P166	13	21	003	-	A
28P42	13	09	003	-	A
28P45	13	15	003	-	A
28P85	13	16	003	-	A
28S166	13	21	003	-	A
28S2708	13	16	003	-	A
28S42	13	09	003	-	A
28S45	13	15	003	-	S
28S46	13	15	003	-	A
28S85	13	16	003	-	A
28S86	13	16	003	-	A
28SA166	13	21	003	-	A
28SA42	13	09	003	-	A
28SA46	13	15	003	-	A
28SA86	13	16	003	-	A
54LS478	13	16	003	-	O
54S476	13	38	003	-	O
54S477	13	38	003	-	O
54S478	13	16	003	-	O
54S479	13	16	003	-	O
74LS478	13	16	003	-	O
74S2708	13	16	003	-	O
74S454	13	06	003	-	O
74S455	13	06	003	-	O
74S476	13	38	003	-	O
74S477	13	38	003	-	O
74S478	13	16	003	-	O
74S479	13	16	003	-	O
TMS2716	23	28	VO3	-	A
Toshiba					
27128	79	51	003	-	S
2732	19	24	003	-	S
2732A	27	24	003	-	S
2732D	19	24	003	-	S
2764	79	33	003	-	S
321	21	26	003	-	S

Table A-1. UniPak 2™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Toshiba (Continued)					
322	21	27	003	-	S
323	19	23	003	-	S
8755AC	47	55	V04	351A-072	S

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Xicor					
2804A	B7	82	V05	-	S
2816A	B7	23	V05	-	S
2864A	C3	98	V05	-	S

ERROR CODES

NOTE

In the case of an error condition, be sure that the family and pinout codes are correct for the PROM installed; refer to table A-1 in appendix A to cross check family and pinout codes.

CODE	NAME	DESCRIPTION
21	Illegal-Bit Error	The device cannot be programmed due to already programmed locations of incorrect polarity.
23	First-Pass Verify Error	The device data was incorrect on the first pass of the automatic verify sequence during device programming.
24	Second-Pass Verify Error	The device data was incorrect on the second pass of the automatic verify sequence during device programming.
27	Insufficient RAM	Due to the value of the Begin RAM Address, there is insufficient RAM to program the device, or the total allotment of RAM resident is less than the word limit of the device.
30	No Programming Algorithm	Valid family and pinout codes are not selected, or family code selection not followed by pinout code selection.
31	Excesive Current Drain	The operation aborted due to excessive current drain by a device.
32	Backward Device	The operation aborted due to V_{CC} level test indicating a backward device.
35	Faulty Chip Select	The operation aborted due to data being present while a device is disabled.
37	Socketing Error	Operation aborted due to a low V_{CC} level indication on sockets presumed to be empty. A device may be in the wrong socket, or two or more devices may be socketed simultaneously.
38	Illegal Operation During Calibration	An illegal or invalid operation was attempted during calibration.
39	Failure to Lock Security Fuse	The security bit did not program and the device is not locked.
70	Faulty Bit Supply	The operation aborted due to a faulty bit supply. Do not use UniPak 2™ until repaired.
71	Faulty CS Supply	The operation aborted due to a faulty CS supply. Do not use UniPak 2™ until repaired.
72	Faulty V_{CC} Supply	The operation aborted due to a faulty V_{CC}. Do not use UniPak 2™ until repaired.
A1	No Identifier Found	The device does not have an electronic identifier. The electronic identifier mode cannot be used.
A2	Invalid Identifier	The electronic identifier of the device has been read and it indicates that the device cannot be programmed using the selected family and pinout codes. Consult table A-1 for the correct family and pinout codes. Try again using these codes.
BØ	Byte Erase Error	The device does not have a byte erase mode. Block limits must be removed and a chip erase performed. The entire chip may then be reprogrammed.
B1	Chip Erase Error	The device does not have a chip erase mode.

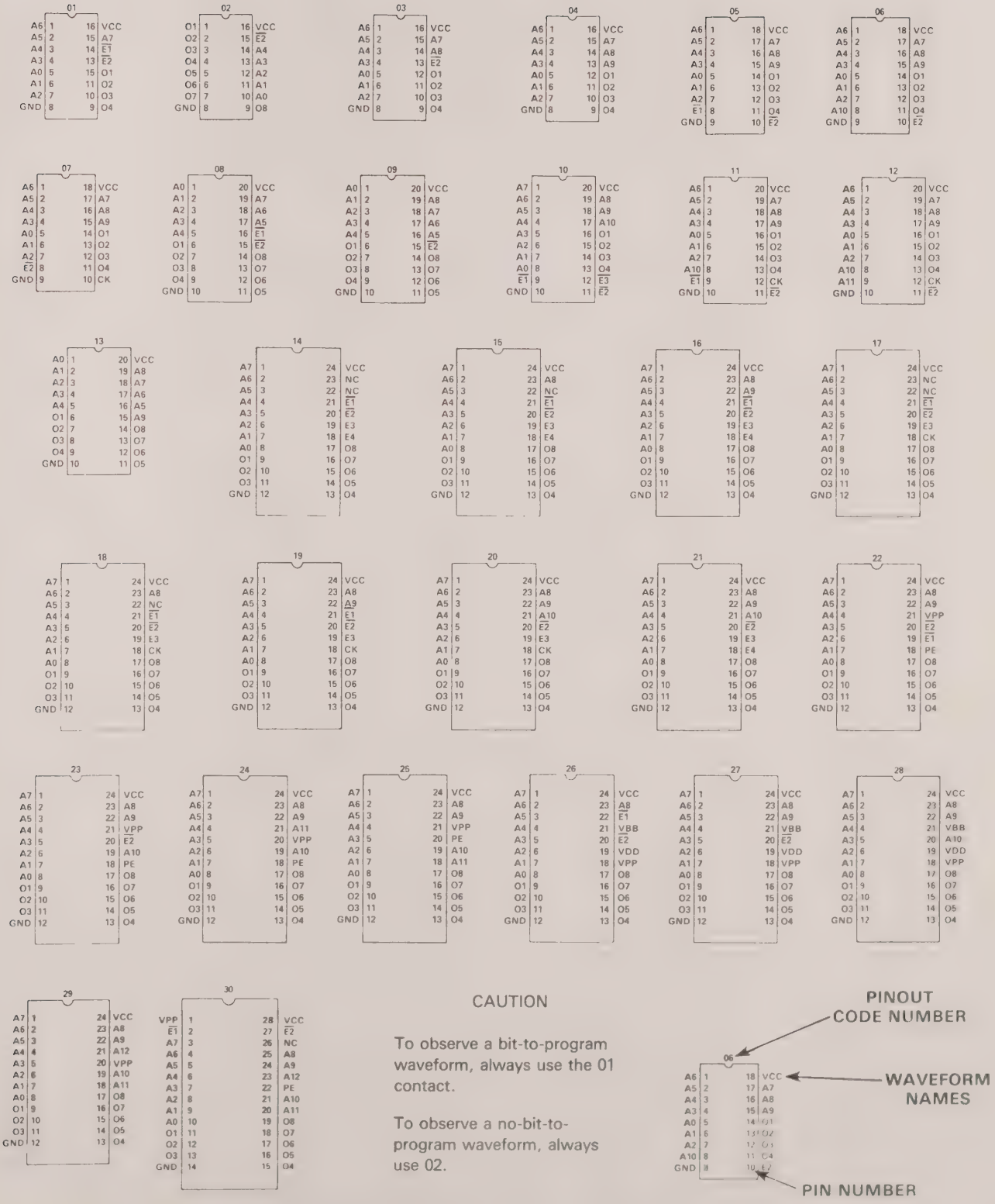


Figure 4-12. Pin Names by Pinout Code Numbers

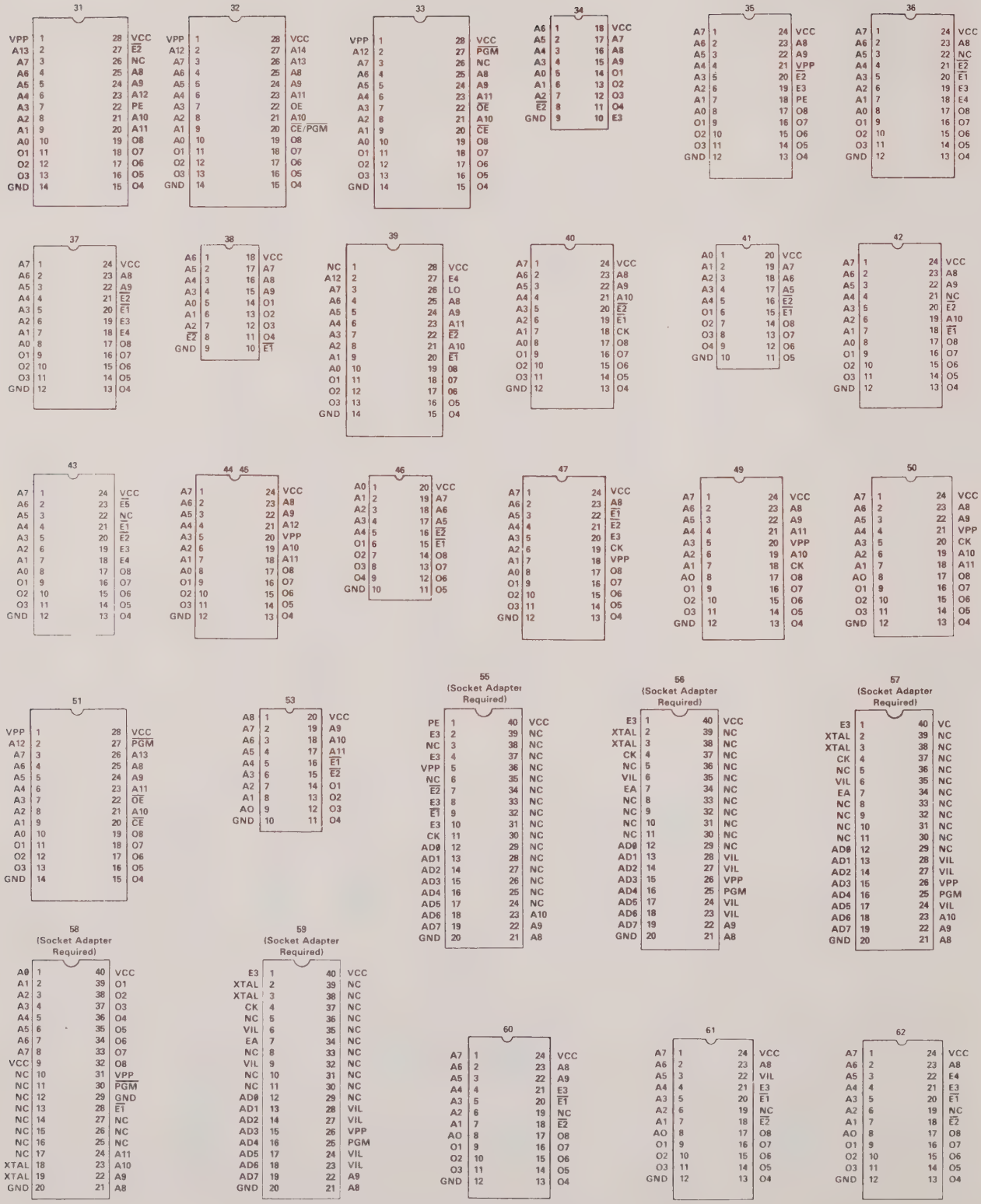


Figure 4-12. Pin Names by Pinout Code Numbers (Continued)

Figure 4-12. Pin Names by Pinout Code Numbers (Continued)

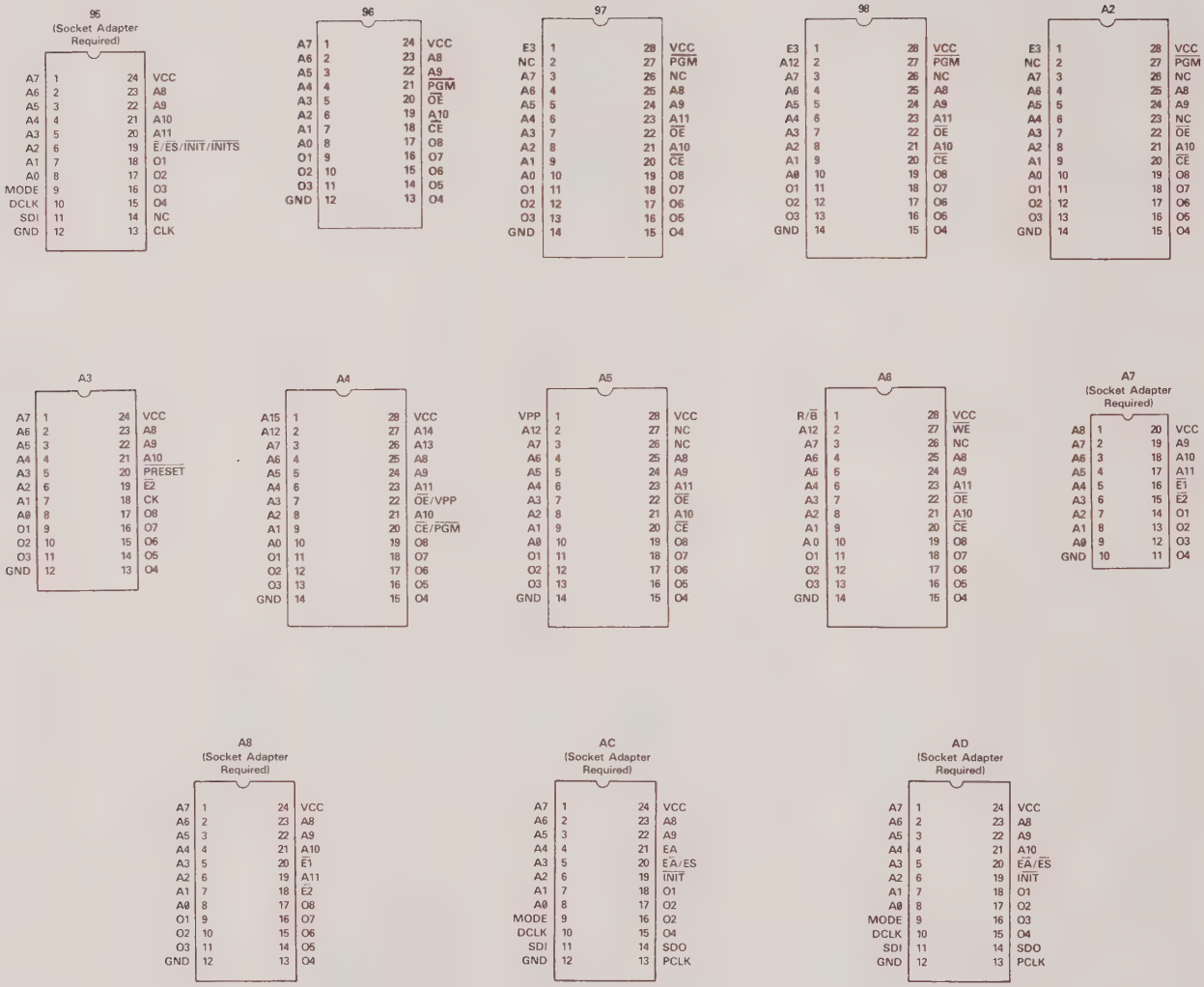


Figure 4-12. Pin Names by Pinout Code Numbers (Continued)

SECTION 4
MAINTENANCE/TROUBLESHOOTING/CALIBRATION

4.1 OVERVIEW

The support material in this section has been provided to help you keep your UniPak 2™ in good operating condition. General maintenance practices are discussed in section 4.2, while the basic troubleshooting steps are listed in section 4.3. For those UniPak 2™ users who prefer to do their own calibration, detailed procedures, including measurement charts and timing diagrams, are provided in section 4.4.

4.2 MAINTENANCE

Before the UniPak 2™ can be cleaned (section 4.2.2) and/or inspected (section 4.2.3), it must be disassembled as described below.

4.2.1 UniPak 2™ Disassembly

To disassemble the UniPak 2™, refer to figure 4-1 and follow the procedure outlined below.

1. Remove the UniPak 2™ from the programmer; see section 2.3 for details.
2. Place the UniPak 2™ face down on a flat surface.
3. Unscrew the captive fasteners (figure 4-1a) until they hang loosely; the screws will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 4-1b) to unlock the flanges.

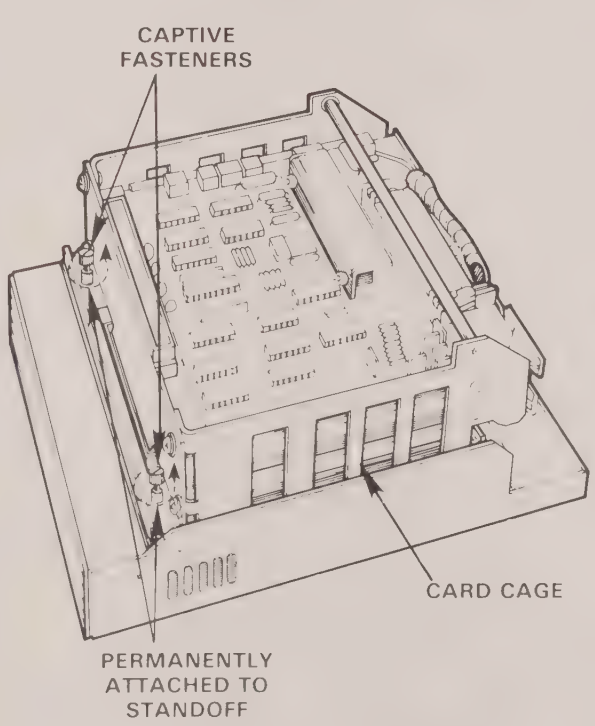


Figure 4-1a) Unscrew captive fasteners.

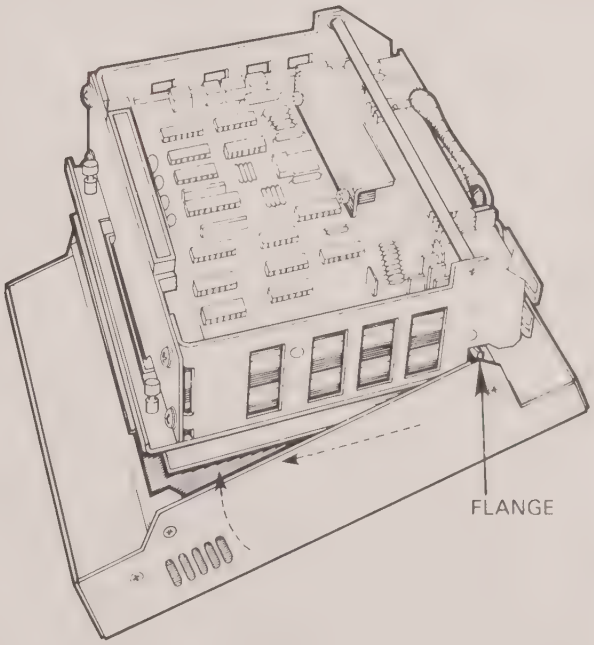


Figure 4-1b) Lift card cage up and out.

Figure 4-1. UniPak 2™ Disassembly

5. Lift the card cage up until you can see the socketboard interconnect cable and its connector (figure 4-2).
6. Flip the extraction tabs out on each side of the connector (figure 4-2).
7. Pull the cable out of the connector.
8. Disconnect the ground wire from the socketboard (see figure 4-2).
9. Flip the extraction tabs out on the top card (waveform generator card) and unplug the interconnect cable from its connector (figure 4-3).
10. Flip the extraction tabs out on the top card (waveform generator card).
11. Pull the waveform generator card out along the guides (figure 4-3).
12. Repeat steps 9, 10, and 11 for the extraction tabs on the address card.
13. Remove the two screws and the shield, and pull the memory card down to unplug it from the edge connector (as shown in figure 4-4).

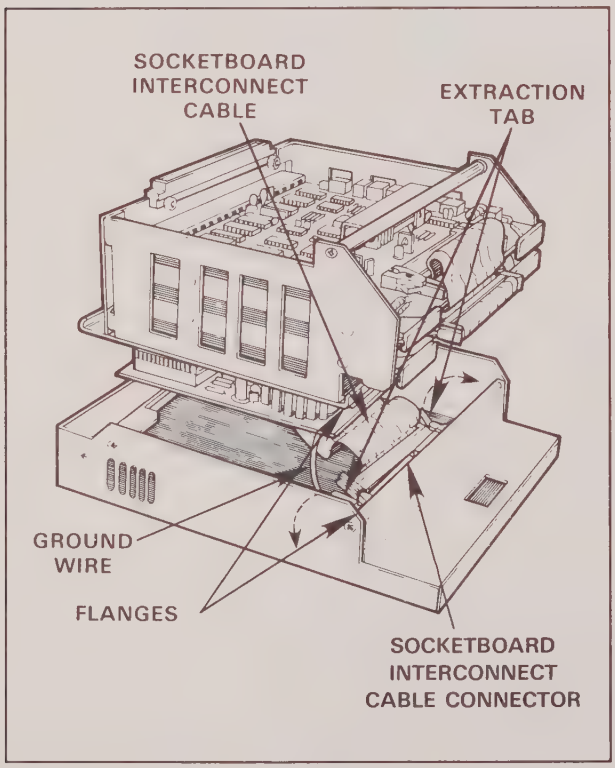


Figure 4-2. Socketboard Interconnect Cable Disconnect

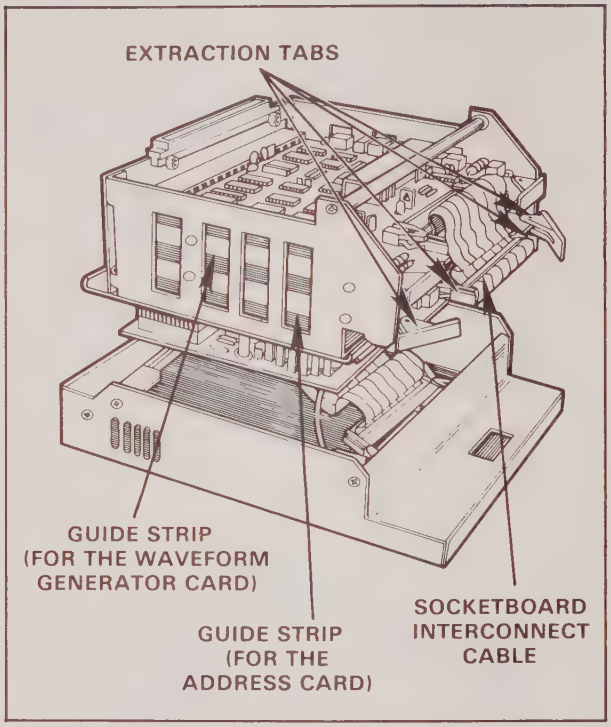


Figure 4-3. Circuit Board Removal

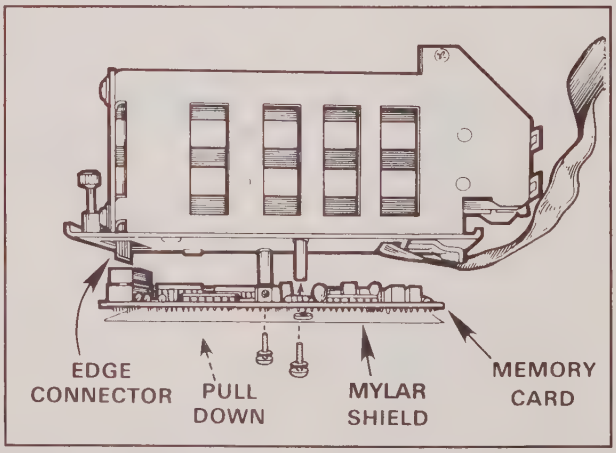


Figure 4-4. Memory Card Removal

4.2.2 Cleaning

Inspect the UniPak 2™ inside and out for accumulated dirt or dust. To clean the UniPak 2™, follow the procedure below.

1. Wipe any dust and/or dirt off the outside of the UniPak 2™ with a clean, damp cloth.

   NOTE

   Do not use abrasive cleaners or solvents. They will etch the paint.

2. Remove dust from the circuit boards with a blast of dry, compressed air or a clean, soft-bristled brush.

4.2.3 Inspection

You can help prevent malfunctions by periodically inspecting your UniPak 2™. Check cable connections, card seating, mounting of socketed components, etc., for shorts, opens or unstable continuity.

If you find heat-damaged components, be particularly careful to find and correct the cause of the overheating. This will prevent further damage.

4.2.4 UniPak 2™ Assembly

1. Plug the memory card onto its edge connector, as shown in figure 4-4.
2. Replace the shield, washers, and the two screws.
3. Flip the two extraction tabs down on the address card.
4. Using the flat surfaces of the extraction tabs, gently push the address card along the guides into its connector.
5. Make sure the extraction tabs on the interconnect cable connector are flipped open.
6. Firmly, but gently, push the socketboard interconnect cable into the connector. Notice that the extraction tabs will move back to their locked positions when the cable is locked into the connector.
7. Repeat steps 3 through 6 to replace the waveform generator card.
8. Reconnect the ground wire to the socketboard.
9. Plug the socketboard interconnect cable into its connector on the socketboard (figure 4-2).
10. Replace the card cage by tilting it up to lock the flanges, as shown in figure 4-1, then gently setting it down. Make sure the captive fasteners line up with the fastener holes on the UniPak 2™ frame.
11. Tighten the captive fasteners finger tight.

4.3 TROUBLESHOOTING

This section will help you interpret and isolate failures in the UniPak 2™. Use it in conjunction with section 5 (Circuit Description) and the schematics provided in the back of this manual.

There are three major classes of failures that can occur in a system comprised of a programmer and a UniPak 2™. The first is no system operation, the second is poor yields, and the third is UniPak 2™ failure.

After successfully troubleshooting the UniPak 2™, you must calibrate it according to the instructions in section 4.4. It is very important that the programmer be calibrated before the UniPak 2™ is calibrated.

4.3.1 No System Operation

You should perform the following steps if the system will not initialize with the UniPak 2™ installed. After completing each step, determine whether the problem still exists.

1. Check to be sure the UniPak 2™ is properly installed in your programmer.
2. Check the UniPak 2™ programmer mating connector (J1) for bent or broken pins. (Pin HH is intentionally shorter.)
3. Check the UniPak 2™ cards to be sure they are correctly installed in their connectors (section 4.2).
4. Check the ribbon cable to be sure it is properly inserted in the connectors (section 4.2).
5. Check the programmer power supplies for proper voltage output levels (see programmer manual).
6. If steps 1 through 5 fail to isolate the problem, contact your local Data I/O Service Center.

4.3.2 Poor Yields

Perform the following steps if the yield rate begins to decrease. After completing each step, determine whether the problem still exists.

1. Do a complete calibration; be sure that the programmer has been calibrated first.
2. Perform waveform observations (section 4.4) for the family of the device being programmed, being careful to note any discrepancies. You may find the circuit description (section 5) and the schematics at the end of this manual useful in isolating the problem.
3. Perform calibration steps 27 and 28 on the measurement chart for the device family that is giving problems. The circuit description (section 5), schematics, and suspected components in tests 1 through 4 of table 4-1 may be helpful in isolating the problem.
4. If steps 1 through 3 fail to resolve the problem, contact your local Data I/O Service Center.

4.3.3 UniPak 2™ Failure

Perform the following steps if a device will not program at all or if error messages are displayed. After completing each step, determine whether the problem still exists.

1. Check that the family and pinout codes are correct for the device, and that the device is being inserted in the correct socket.
2. If possible, try a known-good device to determine whether there is a hardware problem.
3. Check to be sure the UniPak 2™ is properly installed.
4. Check the UniPak 2™ programmer mating (J1) connector for bent or broken pins. (Pin HH is intentionally shorter.)
5. Check the UniPak 2™ cards to be sure they are correctly installed in their connectors (section 4.2).
6. Check to be sure the ribbon cable is correctly oriented and properly inserted in the connectors.
7. Perform a complete calibration, noting any measurements falling outside the indicated limits. Refer to the corresponding test number in table 4-1 for suspected boards and components, as well as the circuit description (section 5) and the schematics, to attempt to isolate the problem.
8. Perform waveform observations and note any discrepancies. Referring to the circuit description and the schematics may be helpful in isolating the problem.
9. If steps 1 through 8 fail to resolve the problem, contact your local Data I/O Service Center.

Table 4-1. Troubleshooting Chart

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
1	701-1655	VR1, U17, U25
2	701-1655	VR1, U16, U25, Q2, Q3
3	701-1655	VR1, U16, U25, Q2
4	701-1690	U15, U7, U12, Q21, R52, CR15, CR16, VR1, Q15
	702-1659	CR18, U10
5	701-1690	U14, U7, U3, Q3, R15, CR4, CR3, U10, U9, U11, Q24, Q25, Q19, CR14, Q16, U18, U17, VR1, Q15
	702-1659	C5, R11, CR9
6	701-1690	U13, U7, U6, Q9, R31, CR10, CR11, Q2, CR19, VR1, Q15
	701-1655	U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, U24, U11, CR6
7	702-1650	U23, U22, VR2, CR3, Q2, R28
	702-1659	CR24, Q10, U20
	701-1655	U4, U14
8	701-1655	VR1, U17, U25
9	701-1655	VR1, U16, U25, Q2
10	701-1655	VR1, U17, U25
11	702-1650	U17, Q3, R3, VR1, U2, Q1, CR1, CR2
	701-1655	U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, CR6, U24, U11
12	702-1650	U17, Q3, R3, VR1, U2, Q1, CR1, CR2, VR3, U5, U22, U11
	701-1655	U23, R1, Q15, Q17, RP8, RP3, RP4, RP2, Q4, U24, U11, CR6
13	701-1690	U17, U18, U11, Q22, Q25, Q2, CR19
	701-1655	U23, R1, RP8, Q16, RP3, Q14, RP4, RP2, Q12, U19, U24, CR9
14	701-1690	U15, U7, U12, Q21, U16
	702-1659	CR18, U10
15	701-1690	U16, U13, U7, U6, Q9
16	701-1690	U16, U14, U7, U3, Q3
17	701-1655	U26, U17, U25, VR1
18	701-1655	U26, U16, U25, VR1, Q2
19	702-1650	U5, U22, U17, U11, Q3, U2, CR1, CR2, Q1
	701-1655	U23, R1, RP8, Q15, RP3, Q17, RP4, RP2, Q4, CR6, U11, U24
20	701-1690, 701-1655, 702-1659	
21	702-1659	U4, DS2
	701-1655	U18
22	701-1690	U15, U7, U12, Q21, CR15, CR14, U16
	702-1659	CR18, U10
23	702-1659	CR26, Q6, Q7, Q5
	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	702-1650	U16, U3, U10, U12, U11, U7
24	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, Q19, CR14, Q16, CR4, CR3
	702-1659	C5, R11

Table 4-1. Troubleshooting Chart (Continued)

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
25	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, U5, Q6, Q8, CR8, CR4, CR3
	702-1659	C5, R11
26	701-1690	U16, U14, U7, U3, Q3, U9, U10, U11, Q24, Q25, U5, Q13, CR9, Q4, Q10, Q12, Q5, Q7, CR4, CR3
	702-1659	C5, R11
27	701-1690	U16, U13, U7, U6, Q9, CR10, CR11, Q2, CR19
	701-1655	U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9, U19, U24
28	701-1690	U16, U13, U7, U6, Q9, Q2, Q18, U17, Q11, CR2, Q14, U5
29	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR18, U10
30	701-1690	U16, U14, U7, U3, Q3, CR4, CR3, U9, U10, U11, Q24, Q25, U5, Q6, Q8, CR8
	702-1659	C5, R11
31	702-1650	U23, U22, VR2, CR3, Q2, R28
	702-1659	CR24, Q10, U20
	701-1655	U4, U14
32	701-1690	U18, U10, U5, U7, Q20, Q7, Q5, Q12, U9, CR9, Q13, U11, Q24
	702-1659	CR8, C5, R11
33	701-1690	U11, CR17, VR2, U18, Q19, Q16, U9, Q24, U10
	702-1659	CR9, R11, C5
34	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	702-1659	CR4, CR3, CR2, U22, CR5, Q1, CR32, CR31, CR28, C3, C13
	702-1650	U5, VR3, U22, U17, U11, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U19, U24, U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9
35	702-1650	U5, VR3, U22, U17, U11, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U19, U24, U23, R1, Q16, RP3, Q17, RP4, RP2, Q8, CR9
36	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR18, U10
37	701-1690	U16, U14, U7, U3, Q3, CR4, CR3, U9, U10, U11, Q24, Q25, U5, Q13, CR9, Q7, Q5, Q12, Q20, U7
	702-1659	C5, R11
38	701-1690	U16, U13, U7, U6, Q9, CR10, CR11
	702-1659	CR4, CR3, CR2, U22, CR5, Q1, CR32, CR31, CR28, C3, C13
	702-1650	U5, VR3, U22, U17, U11, Q3, U2, Q1, CR1, CR2, VR1
	701-1655	U24, U11, U23, R1, RP8, Q15, RP3, Q17, RP4, RP2, Q4, CR9
39	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR18, U10
40	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, CR6, U24, U11, U19, CR4, CR7
	702-1659	Q2, CR29, R30, CR28, CR31, CR32
41	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, U24, U11, U19, CR4
	702-1659	Q2, CR29, R30, CR28, CR31, CR32
42	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, U24, U11, U19, CR4
	702-1659	Q2, CR29, R30, CR28, CR31, CR32
43	701-1655	VR1, U16, U25, Q2, RP5, U28, U22, CR9, CR6, U24, U11, U19, CR4, CR7
	702-1659	Q2, CR29, R30, CR28, CR31, CR32

Table 4-1. Troubleshooting Chart (Continued)

TEST NUMBER	SUSPECT CARDS	SUSPECT COMPONENTS
44	702-1659	DS1, U4
	701-1655	U18
45	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR7, U10
46	701-1655	U2, U3, U4, U14
	702-1650	U23, U22, VR2, CR3, Q2
	702-1659	CR24, Q10, U20, U21, U13
47	701-1655	U2, U3, U4, U14
	702-1650	U23, U22, VR2, CR3, Q2
	702-1659	CR24, Q10, U20, U21, U13
48	701-1655	U2, U3, U4, U14
	702-1650	U23, U22, VR2, CR3, Q2
	702-1659	CR24, Q10, U20, U21, U13
49	701-1655	U2, U3, U4, U14
	702-1650	U23, U22, VR2, CR3, Q2
	702-1659	CR24, Q10, U20, U21, U13
50	701-1655	Q4, Q8, Q12, Q5, Q14-17, U23
51	701-1655	Q6, Q11, Q9, Q7, Q14-Q17, U23
52	701-1655	Q4, Q8, Q12, Q5, Q14-17, U23
53	701-1655	Q6, Q11, Q9, Q7, Q14-17, U23
54	702-1659	DS3, U4
	701-1655	U18
55	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	CR22, U10
56	702-1659	DS4, U4
	701-1655	U18
57	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	U10, CR1
58	702-1659	DS5, U4
	701-1655	U18
59	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	U10, CR11
60	702-1659	DS6, U4
	701-1655	U18
61	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	U10, CR19
62	702-1659	DS7, U4
	701-1655	U18
63	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	702-1659	U10, CR23
64	702-1659	Q3, CR14, RP1, R10, CR17, U10
	701-1655	U18, U22
65	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-1655	VR1, U16, U17, U25, Q2, Q3, Q1
	702-1659	CR17, CR1, CR11, CR19, CR23, CR22, CR7, CR18, U10
66	701-1690	U16, U15, U7, U12, Q21, CR15, CR16
	701-1655	VR1, U16, U17, U25, Q2, Q3, Q1
	702-1659	CR17, CR1, CR11, CR19, CR23, CR22, CR7, CR18, U10

4.4 CALIBRATION

The need for calibration varies with the amount of use your UniPak 2™ receives. Generally, we suggest calibration whenever: 1) programming yields fall below the manufacturer's recommended minimums, or 2) troubleshooting has been completed, or 3) the user's company policy requires periodic calibration certification.

NOTE

If calibration or repair is required but you lack the facilities to accomplish it, contact the nearest Data I/O Service Center.

Because of differences in programmer mainframes, this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the UniPak 2™.

Calibration of the UniPak 2™ consists of three parts:

1. Power Supply Calibration—measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part of the calibration procedure must be done first. Refer to your programmer manual.
2. DC Calibration—consists of measuring and adjusting critical DC voltage levels generated by the UniPak 2™.
3. Waveform Observation—enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturers' critical voltage and timing specifications.

The first part of the calibration procedure (power supply calibration) varies with the type of programmer you have. Therefore, this manual refers you to your programmer manual for details on power supply calibration. DC calibration is discussed in section 4.4.1, the optional verify voltage checks are described in 4.4.2, and waveform observation is detailed in section 4.4.3. For information on how to carry out these steps on various programmers, consult your programmer manual.

The following equipment is necessary to calibrate the UniPak 2™:

- Data I/O calibration extender (part number 910-1521)
- Three and a half-digit digital voltmeter (DVM)
- Dual-trace oscilloscope (Tektronix 465 or equivalent)

Check the appropriate programmer manual for any additional equipment that you may need to calibrate the programmer.

To prepare your UniPak 2™ for calibration, follow the procedures outlined below.

1. Turn the programmer power off; see section 3.3 for details.
2. Remove the UniPak 2™ from the programmer; see section 2.3 for details.
3. Insert the calibration extender into the programmer the same way you insert the UniPak 2™ (section 2.2).
4. Unscrew the two thumb screws (captive fasteners) located on the underside of the top cover of the UniPak 2™ (figure 4-1); they connect the card cage to the socket assembly. Separate the two parts of the assembly.

CAUTION

Do not let the fasteners short to the motherboard.

5. Insert the 64-pin connector of the card cage into the mating connector on the calibration extender (figure 4-5, detail B).
6. Lean the top portion of the UniPak 2™ against its bottom portion at a 45-degree angle; see figure 4-5.

NOTE

Be sure the socket assembly flange locks into the card cage flange (see figure 4-5, detail A).

Do not allow the frame of the socket assembly to short to the memory board.

Be careful not to strain the cable or scratch the top of the programmer.

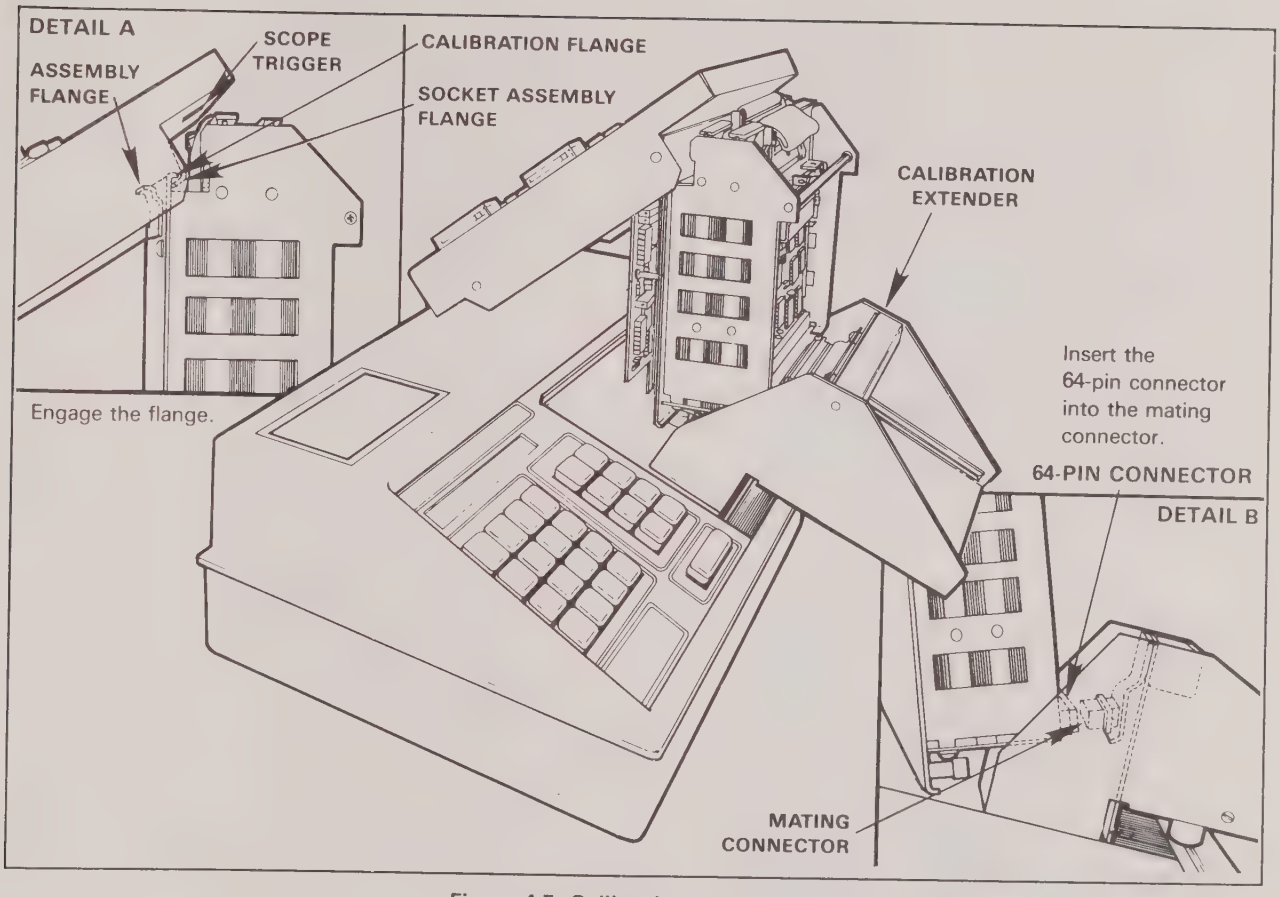


Figure 4-5. Calibration Setup

4.4.1 DC Calibration

The DC calibration procedure described in this section enables you to adjust critical DC voltage levels generated by the UniPak 2™. To follow this procedure, use the measurement chart at the end of this section. This measurement chart contains the information needed for all DC calibration tests. This information is included on the measurement chart in columns with the following headings:

- Step No.—tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- Test No.—identifies individual tests.
- Test Description—identifies the functions being tested.
- Measurement Test Location—tells which socket pins, circuit boards, or test points to probe for measuring voltages.
- Measurement—specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the UniPak 2™ until the problem is corrected.
- Adjustment Location—tells which potentiometer to adjust if a measurement is out of range.
- Comments—gives special instructions for particular tests.

The DC calibration procedure is as follows:

CAUTION

Remove all devices from the sockets before entering the calibration mode (see section 3.8 for details). Waveform generation may damage any device in the UniPak 2™ sockets.

1. Turn the programmer power on (section 3.2).
2. Put the programmer into the calibration mode by following the key sequences in table 4-2.
3. Perform the general calibration steps (steps 1 through 24) on the measurement chart. For steps 5, 6, and 7, refer to the figures at the end of the measurement chart to observe the bit switch rise waveform the DAC step waveforms, and the current DAC step waveform.

Table 4-2. Key Sequence To Access the Calibration Mode

Programmer System	Key Sequence To Enter Calibration Mode	To Increment Step No.	To Decrement Step No.
19	Press SELECT Press C2 Press ENTER Enter Step Number* Press START	Press ENTER	Press REVIEW
29A/ 29B	Press SELECT Press C1 Press START Enter Step Number* Press START	Press START	Press REVIEW
100A	Press SELECT Press 12 Enter Step Number* Press START	Press START	Press BACK-SPACE

*Optional

For each general calibration step on the measurement chart do the following:

- Take measurement readings at the device sockets or test points indicated on the measurement chart; figure 4-6 shows the pin numbers for the sockets; figure 4-7 shows test points.
- Ground the digital voltmeter to socket 7, pin 10 on the front panel of UniPak 2™.
- The adjustment pots on the waveform generator, memory board, and the address card enable you to make adjustments when your measurements do not match the measurement chart; figure 4-7 shows the location of these adjustment points.

- Access each new step by pressing the START (or ENTER) key. The new step number will appear in the display when the UniPak 2™ is ready for the next step. To go back to a previous test, press the REVIEW (or BACKSPACE) key.

NOTE

The remaining steps on the measurement chart (steps 25 through 28) are family specific. These steps are optional and have been included for your convenience.

4. For each family-specific calibration step on the measurement chart, do the following to enter the family and pinout codes:

   - Perform a **load operation**; refer to your programmer manual for details.
   - Enter the family and pinout codes when prompted by the programmer; refer to your programmer manual for further information.
   - Fill RAM with data specified on the timing diagram.
   - Put the programmer back into the calibration mode; see figures 4-8, 4-9, and 4-10 for the key sequence.
   - Enter the step number from the measurement chart.
   - Press START.

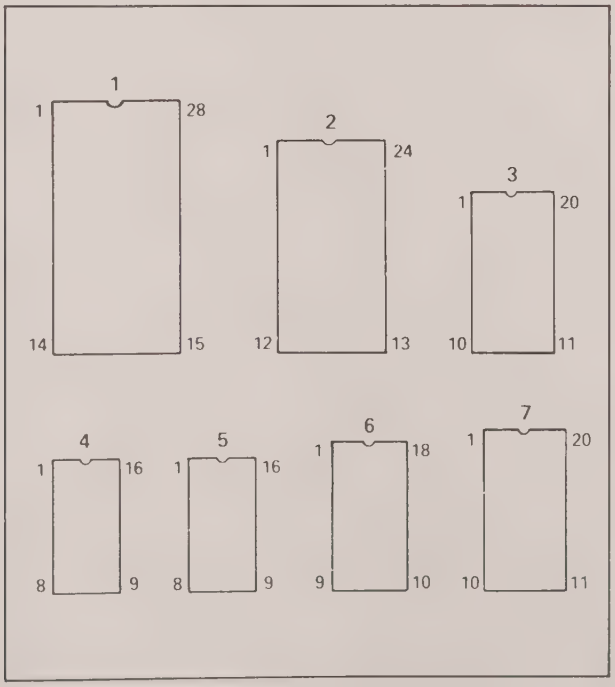


Figure 4-6. Pin Numbers of Device Sockets

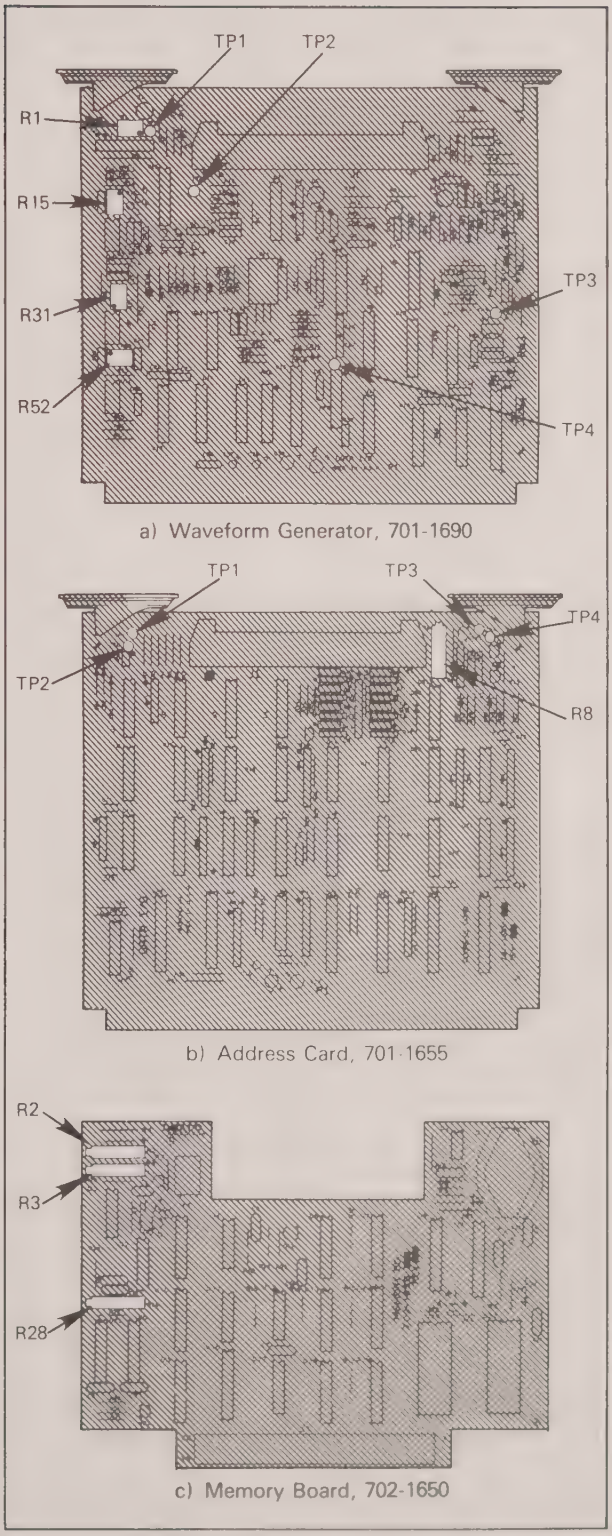


Figure 4-7. Adjustment Locations

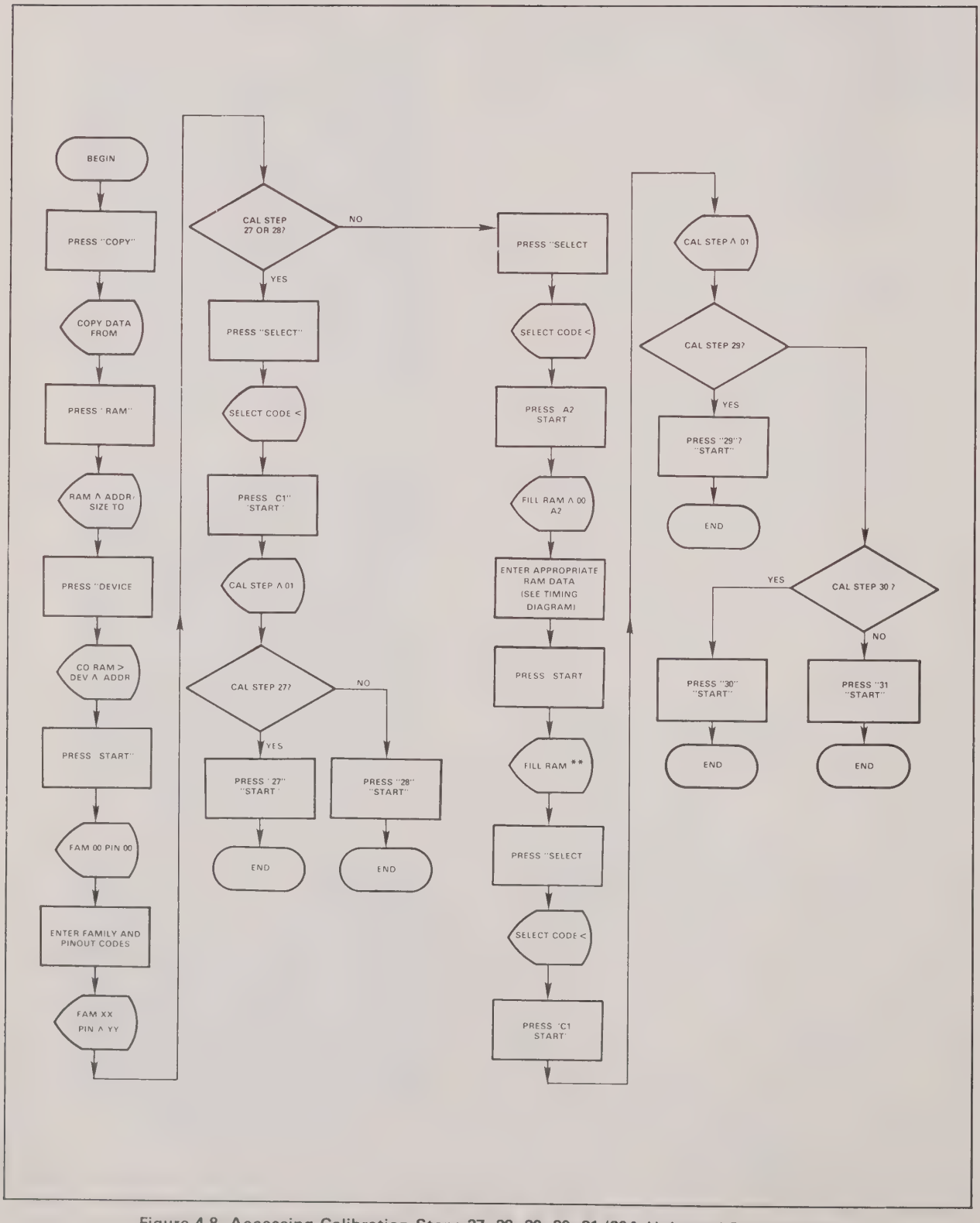


Figure 4-8. Accessing Calibration Steps 27, 28, 29, 30, 31 (29A Universal Programmer)

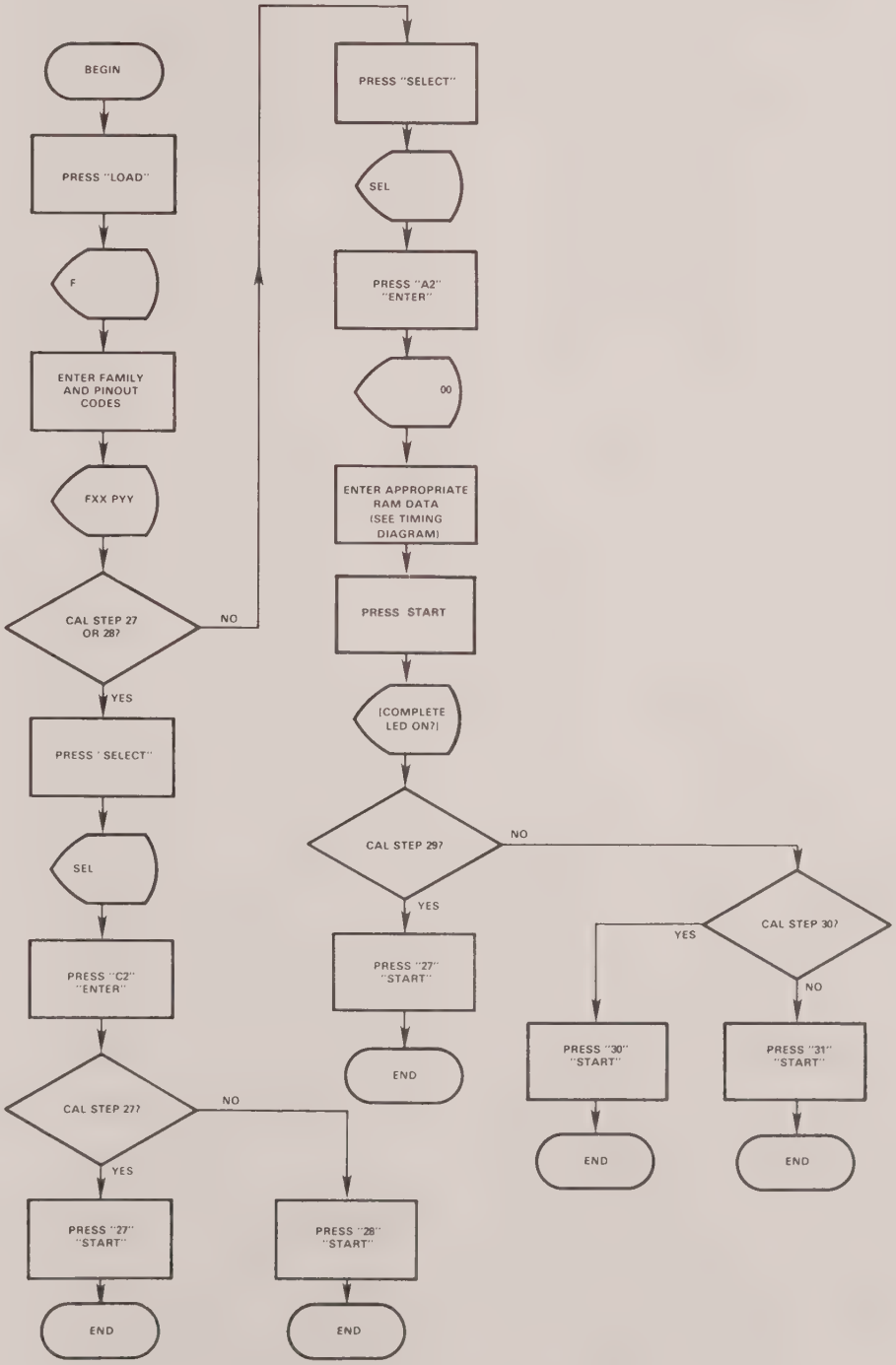


Figure 4-9. Accessing Calibration Steps 27, 28, 29, 30, and 31 (System 19)

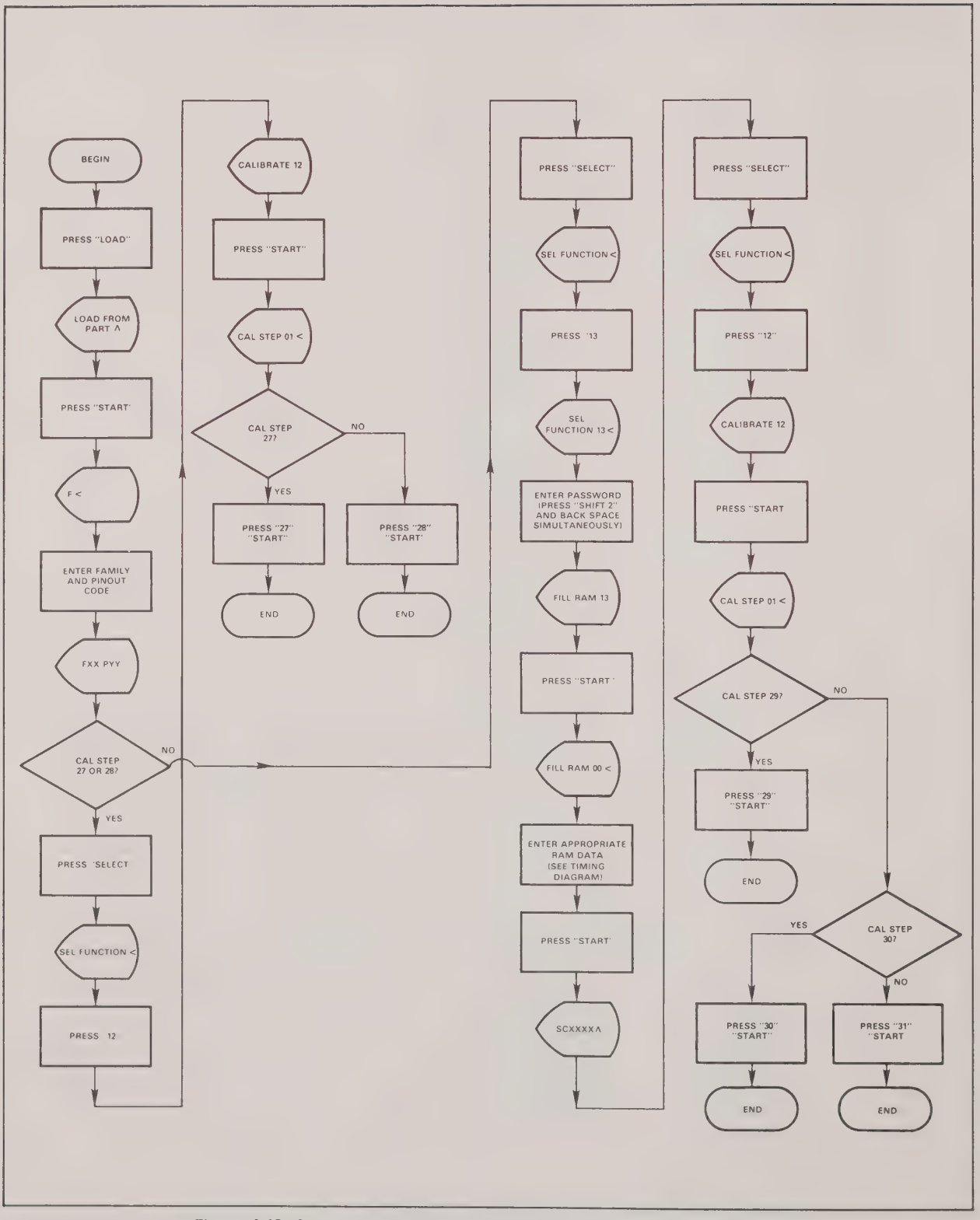


Figure 4-10. Accessing Calibration Steps 27, 28, 29, 30, 31 (Model 100A)

4.4.2 Optional Verify-Voltage Checks

Two calibration steps (27 and 28) have been provided for the measurement of first- and second-pass verify voltages. The family characteristics table in the applicable family timing diagram defines the levels for first- and second-pass verifications for each family. These are provided for the investigation of yield problems; no adjustments are available. Under normal circumstances, these steps can be eliminated from a routine calibration.

4.4.3 Waveform Observation

Programming waveforms of your UniPak 2™ can be observed with an oscilloscope and compared with the timing diagrams that are provided in appendix B. In this way, timing and magnitude relationships can be measured against known specifications to confirm that the UniPak 2™ is performing to the device manufacturer's specifications. Since the UniPak 2™ generates a large number of waveforms and all calibration adjustments are accomplished in DC calibration, it is necessary only to observe waveforms for commonly used devices or those that are presenting yield problems.

During the waveform observation phase of the calibration procedure, your UniPak 2™ uses a firmware routine that generates programming waveforms for the data stored in system RAM. An oscilloscope trigger pulse is generated for every address increment. This occurs after the reject pulse count has been reached for all the bits being programmed in the previous data word. The address is automatically reset to Ø when the maximum PROM address is reached, and incrementing continues. Waveform observation can be done with the UniPak 2™ either on the calibration extender or plugged into the programmer.

The waveform observation procedure described below calls for filling RAM with data so that it is possible to observe bit-to-program waveforms. The procedure takes into account the device type (VOL or VOH) so that for either type of PROM a bit-to-program will appear on the same socket contact.

When used with a timing diagram, this procedure allows you to compare waveforms on the oscilloscope with the waveform photographs on the timing diagram for any type of device; a detailed explanation of the timing diagrams is provided in section 4.4.4. The waveform observation procedure is as follows:

1. Refer to table A-1 to determine the family and pinout codes, polarity, and technology of the selected device.

   NOTE
   Polarity is indicated in the family code. Odd-numbered families are VOL and even-numbered families are VOH.

2. Initiate a load operation; refer to section 3.4 for details.
3. Key in the family and pinout codes when prompted by the programmer; see section 3.5.
4. Fill your programmer's RAM with programming data listed in the timing diagram for the family code entered: the correct data depends on the polarity and technology of the device. Refer to table 4-3 for the "Fill RAM" key sequence.

   CAUTION
   Remove all devices before entering the calibration mode. Waveform generation may damage any device in the UniPak 2™ sockets.

Table 4-3. Key Sequence To Fill RAM With Data

System	Key Sequence
19	Press SELECT A 2 Press ENTER Enter data Press START
29A/29B	Press SELECT A2 Press START Enter data Press START
100A	Press SELECT 1 3 Enter Password (SHIFT 2/ BACKSPACE Enter data Press START

5. Enter the waveform generation mode at step 27 on the measurement chart by following the key sequences listed in figure 4-8, 4-9, or 4-10, depending on your programmer.
6. Erase waveforms for EEPROMs are observable at step 30 or 31 of the measurement chart by following the key sequences listed in figure 4-8, 4-9 or 4-10, depending on your programmer.
7. Trigger your oscilloscope by connecting to the test point under the top edge of the socket assembly (see figure 4-11).
8. Ground the scope to the GND contact of the socket with its LED illuminated; the GND contacts are shown in figure 4-12.
9. To observe individual waveforms, refer to figure 4-13 under the pinout code number entered in step 3. The individual socket illustrations give the numbers of the socket contacts to probe when observing the waveforms on the timing diagram.

   NOTE
   Considerations helpful in setting up and interpreting the waveform displays are explained in section 4.4.4.

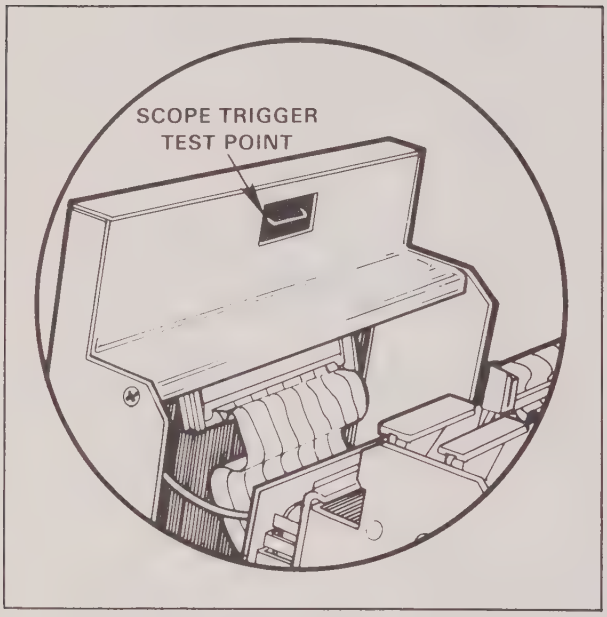


Figure 4-11. UniPak 2™ Scope Trigger Test Point

4.4.4 Detailed Explanation of the Timing Diagrams

This manual contains a timing diagram for each device family that can be programmed by the UniPak 2™. Each timing diagram contains a set of waveform photographs that show critical programming parameters. To use these diagrams and photographs, read the information provided below and refer to the sample timing diagram (figure 4-13).

1. FAMILY CODE NUMBER—corresponds to the family code number of the device (refer to table A-1).
2. FAMILY CHARACTERISTICS TABLE—lists the minimum and maximum parameter values; voltage and timing parameters other than those listed in this table are to be considered noncritical with a ±10% tolerance.
3. NOTES—important information pertaining to a timing diagram.
4. WAVEFORM NAMES—correspond to the pin names on the pinout chart (figure 4-12); the pinout chart tells you which socket pins to probe when you are observing the waveforms for a particular device pinout within a family. (The pinout is indicated by the number above each socket on figure 4-12 which corresponds to the pinout code on table A-1.)

   We recommend that you use the oscilloscope's single-sweep mode for address observation, since one trigger pulse is generated for each address change.

   - BIT NO PROG—Always use the 02 (bit 2) contact (shown in figure 4-12).
   - BIT TO PROG—always use the 01 (bit 1) contact (shown in figure 4-12).

5. LAYOUT SEQUENCE NUMBER—used as a reference point within each diagram.
6. DELAY TIME POSITION—indicates the time from the start of the main sweep to the start of the delay time.
7. OSCILLOSCOPE GROUND REFERENCE—ground contact on the socket with its LED illuminated.
8. TIME-BASE AND VOLTS-PER-DIVISION SETTINGS—Horizontal positioning of the waveforms is not critical and may vary slightly from the photographs. The important observation is the timing relationship between the waveforms in the photographs. You can adjust this timing relationship on your oscilloscope to set convenient reference points. By taking into account any time-base variance, you can also make time comparisons between photographs. The time base is always the same for different waveforms in the same photograph.
9. EXPANDED PHOTOGRAPH NUMBER—corresponds to the photograph number. These detailed photographs are included to magnify rapid voltage changes or particular pulses in a pulse train.
10. VOLTAGE—indicates volts per division. The one in the upper left corner is for the top trace, and that in the lower left corner is for the bottom trace.

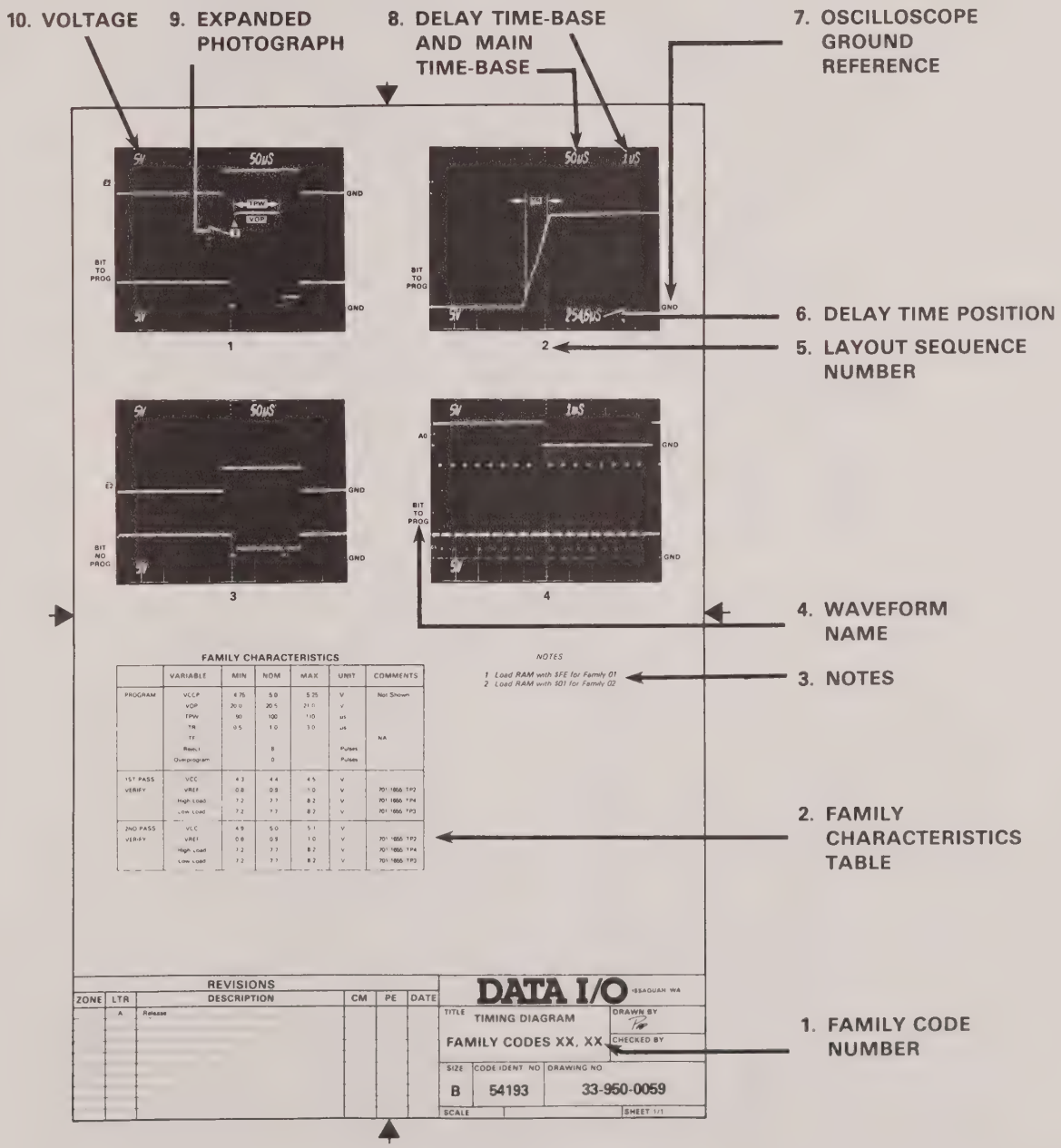


Figure 4-13. Sample Timing Diagram

Table 4-4. Measurement Chart

REVISIONS

LTR	DESCRIPTION	P E	DATE
A			10/82
C	ECN 4831		5/83
D	ECN 5023		2/84

UniPak 2™ Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
			The following tests are performed					
			with the UniPak 2™ on the calibration					
			extender.					
1	1	V reference supply	701-1655/TP2	14.4V	14.5V	14.6V	R8,701-1655	
	2	Load supply (high range)	701-1655/TP4	25.0V		26.0V		
	3	Load supply (low range)	701-1655/TP3	25.0V		26.0V		
	4	V_{CC} supply	2 24	11.9V	12.0V	12.1V	R52,701-1690	
	5	CE supply	2 20	32.7V	33.0V	33.2V	R15,701-1690	
	6	Bit supply	2 9	25.7V	26.0V	26.2V	R31,701-1690	
	7	Address supply	2 8	14.8V	15.0V	15.2V	R28,702-1650	
2	8	V reference supply	701-1655/TP2	6.70V		6.90V		
	9	Load supply	701-1655/TP3	10.3V		11.7V		
3	10	V reference supply	701-1655/TP2	3.30V		3.50V		
	11	Current source 20 mA	2 9	19.5 mA	20.0 mA	20.5 mA	R3,702-1650	Use a 100-ohm, 2W carbon comp resistor in series with the current meter.
4	12	Current source supply	2 9	118 mA	120 mA	122 mA	R2,702-1650	Use a 100-ohm, 2W carbon comp resistor in series with the current meter.

Table 4-4. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A			10/82
C	ECN 4831		5/83
D	ECN 5023		2/84

UniPak 2™ Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
5	13	Bit switch rise waveform	2 14				R17, 701-7997	See waveform photograph (page 27).
6		DAC step waveforms						
	14	V_{CC}	2 24					See waveform photograph (page 28).
	15	Bit supply	701-1690/TP2					
	16	CE supply	701-1690/TP1					
	17	V_{REF} supply	701-1655/TP2					
	18	Load supply	701-1655/TP3					
			The following tests are performed					
			with the UniPak 2™ installed in its					
			normal operating position.					
7	19	Current DAC step waveform	2 9					Place a 200-ohm, 5W resistor
								between pins 9 and 12,
								socket 2 (page 26).
8	20	All voltages off	all all	-0.1V		0.4V		
9	21	Socket 2 LED						Confirm that socket 2 LED is on.
	22	V_{CC} supply load	2 24	11.8V		12.1V		Place a 20-ohm, 2W resistor
								between pins 24 and 12,socket 2.
10	23	Fast V_{CC} supply load	2 24	12.0V		13.0V		Same as above.

Sheet 2 of 6

Table 4-4. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A			10/82
C	ECN 4831		5/83
D	ECN 5023	CJ	2/84

UniPak 2™ Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
11	24	CE supply load	2 20	32.3V		33.2V		Ground DMM to socket 7, pin 10
								Place a 100-ohm, 10W resistor
	25	Pin 18 voltage switch	2 18	32.7V		33.2V		between pins 20 and 12,socket 2.
	26	Pin 21 voltage switch	2 21	32.7V		33.2V		
12	27	Bit supply load	2 11	25.2V		26.0V		Place a 100-ohm, 5W resistor
								between pins 11 and 12,socket 2.
	28	Pin 19 voltage switch	2 19	25.6V		26.2V		
13	29	V_{CC} voltage linearity	2 24	3.90V		4.10V		
	30	CE supply linearity	2 18	23.0V		23.5V		Place a 2.2K-ohm, 1/2W resistor
								between pin 12 and 18,
								socket 2.
	31	Address supply	2 8	4.70V		5.30V		
	32	-5V supply	2 21	-5.2V		-4.8V		
	33	12-volt supply	2 20	11.4V		12.6V		
	34	Clamp supply	2 11	20.5V		21.5V		
	35	Current source linearity	2 11	88 mA		92 mA		Use a 100-ohm, 2W carbon
								comp resistor in series with
								the current meter.
14	36	V_{CC} voltage linearity	2 24	4.90V		5.10V		

Table 4-4. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P E	DATE
A			10/83
C	ECN 4831		5/83
D	ECN 5023		2/84

UniPak 2™ Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION		MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
									Ground DMM to socket 7, pin 10
	37	CE supply linearity	2	21	11.4V		12.0V		
	38	Clamp supply linearity	2	9	6.7V		7.3V		
15	39	V_{CC} voltage linearity	2	24	5.90V		6.10V		
	40	I source and pulldowns	2	9,11,14,16	2.0V		2.6V		
	41	I source and pulldowns	2	10,13,15,17	0.0V		1.0V		
16	42	I source and pulldowns	2	10,13,15,17	2.0V		2.6V		
	43	I source and pulldowns	2	9, 11, 14, 16	0.0V		1.0V		
17	44	Socket 1 LED							Confirm that socket 1 LED is on.
	45	V_{CC} voltage supply	1	28	4.90V		5.10V		
	46	Odd address and data	1	2,3,5,7,9,11,13,16,18,	3.5V		6.0V		
		high		20,22,24,26					
	47	Even address and data	1	1,4,6,8,10,12,15,17,19,21,	-0.1V		0.4V		
		low		23,25,27					
18	48	Odd address and data	1	2,3,5,7,9,11,13,16,18,	-0.1V		0.4V		
		low		20,22,24,26					
	49	Even address and data	1	1,4,6,8,10,12,15,17,19,21,	3.5V		6.0V		
		high		23,25,27					
19	50	Odd data lines high	1	11,13,16,18	25.5V		26.5V		
	51	Even data lines pullups	1	12,15,17,19	4.5V		5.5V		

Table 4-4. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A			10/82
C	ECN 4831		5/83
D	ECN 5023		2/84

UniPak 2™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS
								Ground DMM to socket 7, pin 10
20	52	Odd data lines pullups	1 11,13,16,18	4.5V		5.5V		
	53	Even data lines high	1 12,15,17,19	25.5V		26.5V		
21	54	Socket 3 LED						Confirm that socket 3 LED is on.
	55	V_{CC} voltage supply	3 20	4.90V		5.10V		
22	56	Socket 4 LED						Confirm that socket 4 LED is on.
	57	V_{CC} voltage supply	4 16	4.90V		5.10V		
23	58	Socket 5 LED						Confirm that socket 5 LED is on.
	59	V_{CC} voltage supply	5 16	4.90V		5.10V		
24	60	Socket 6 LED						Confirm that socket 6 LED is on.
	61	V_{CC} voltage supply	6 18	4.90V		5.10V		
25	62	Socket 7 LED						Confirm that socket 7 LED is on.
	63	V_{CC} voltage supply	7 20	4.90V		5.10V		
26	64	V_{CC} pullup 1 on	1 28	4.0V		5.2V		
		V_{CC} pullup 2 on	2 24	4.0V		5.2V		
		V_{CC} pullup 3 on	3 20	4.0V		5.2V		
		V_{CC} pullup 4 on	4 16	4.0V		5.2V		
		V_{CC} pullup 5 on	5 16	4.0V		5.2V		
		V_{CC} pullup 6 on	6 18	4.0V		5.2V		
		V_{CC} pullup 7 on	7 20	4.0V		5.2V		

Sheet 5 of 6

Table 4-4. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A			10/82
C	ECN 4831		5/83
D	ECN 5023	CS	2/84

UniPak 2™ Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT			ADJUSTMENT LOCATION	COMMENTS
				MIN	NOM	MAX		Ground DMM to socket 7, pin 10
			Steps 27 through 31 are optional.					
27	65	Static 1st-pass verify						See family characteristics table
		levels						in the applicable timing
								diagram.
28	66	Static 2nd-pass verify						See applicable timing diagram.
		levels						
29	67	Programming waveforms						See applicable timing diagram.
30	68	Chip erase waveforms						See applicable timing diagram.
								For electrically erasable
								devices only.
31	69	Byte erase waveforms						See applicable timing diagram.
								For electrically erasable
								devices only.

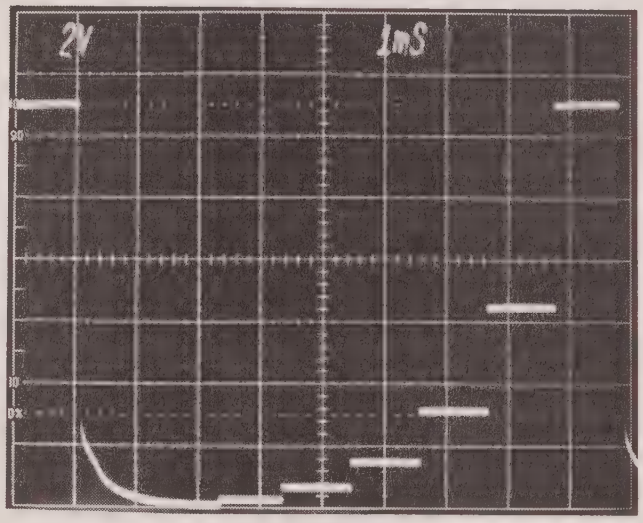
Sheet 6 of 6

Measurement Chart Photographs

Measurement Chart

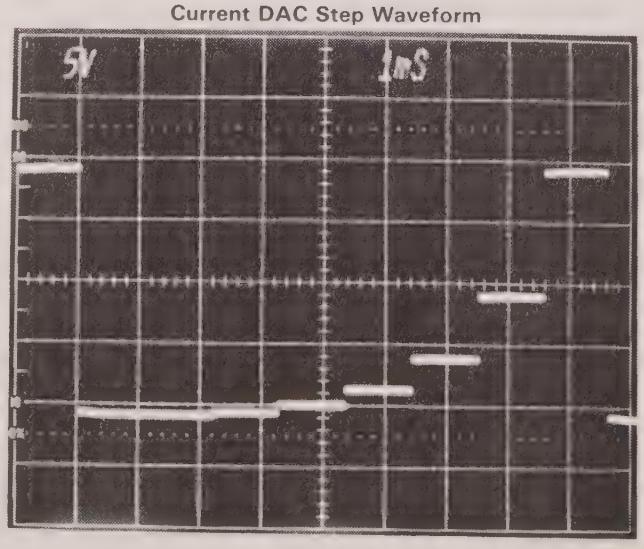
PROGRAM ELECTRONICS UNIPAK 2™

DAC Step Waveform



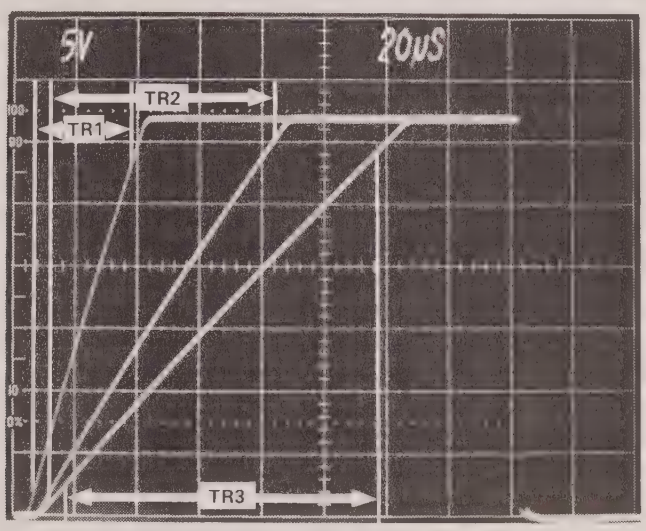
LOAD SUPPLY DAC

Current DAC Step Waveform



DATE	REV	REVISION RECORD	DR	CK
10-82				C.J.S.
3-84				C.J.S.

Bit Switch Rise Waveform



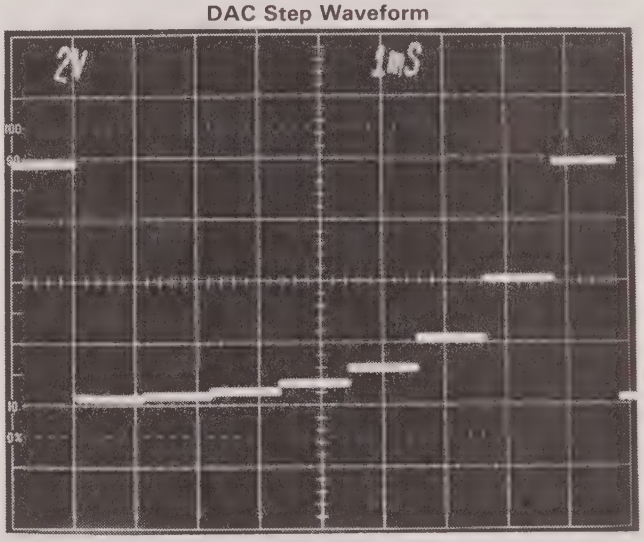
	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	TR1	29	33	37	μs	
	TR2	65	66	67	μs	Adjust R1, 701-1690.
	TR3	90	100	110	μs	

NOTE: All TR's are measured from 10% to 90%.

Measurement Chart

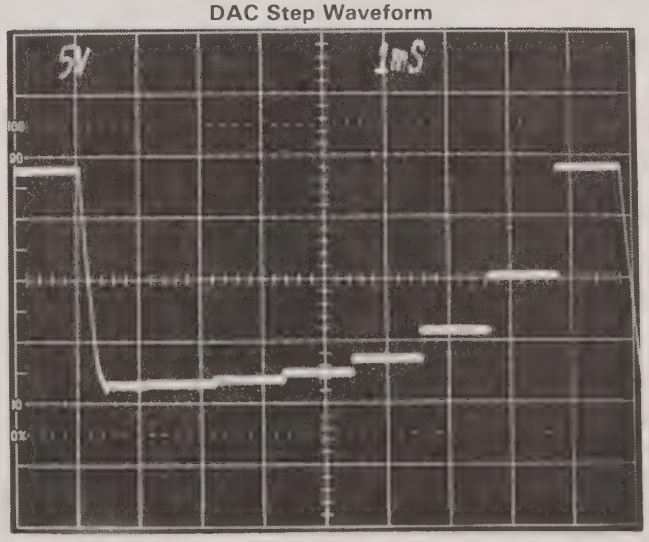
PROGRAM ELECTRONICS UNIPAK 2™

DAC Step Waveform



V_{CC} DAC

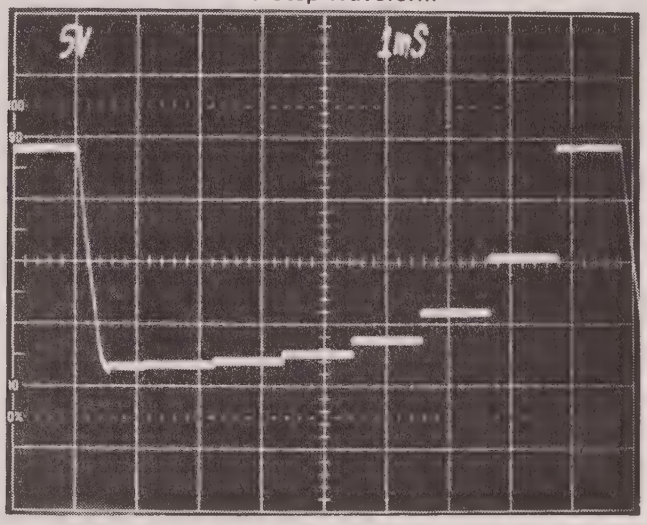
DAC Step Waveform



$\overline{CE}$ SUPPLY DAC

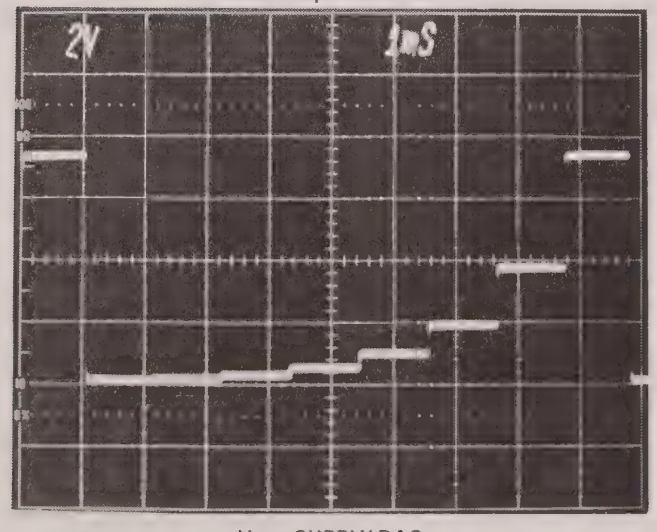
DATE	REV	REVISION RECORD	DR	CK
10-82				
3-84				C73

DAC Step Waveform



BIT SUPPLY DAC

DAC Step Waveform



V_{REF} SUPPLY DAC

SECTION 5
CIRCUIT DESCRIPTION

5.1 OVERVIEW

This section defines the functions of UniPak 2™ principal hardware components. Each circuit-card assembly is depicted by a block diagram accompanied by a written description.

5.2 GENERAL ARCHITECTURE

5.2.1 The Link Between the UniPak 2™ and the Programmer

The UniPak 2™ is controlled by the programmer's extended processor bus through the UniPak 2™ mating connector (J1). The control software for the UniPak 2™ is located in EPROM on the memory card (702-1650).

5.2.2 The Buses

The programmer's address bus, data bus, R/$\overline{W}$ line and $\overline{V \bullet \emptyset_2}$ line access the software on the memory card and control the gates and registers on the waveform generator (701-1690) and address cards (701-1655). The UniPak 2™'s device bus gathers the programming waveforms produced by these cards and transmits them to the socket card (702-1659). Figure 5-1 shows the relationships between the buses.

5.3 COMPONENT LAYOUT

The principal components of the UniPak 2™ are the motherboard, the waveform generator, the address card, the socket card, and the memory card. The component layout of the UniPak 2™ is shown in figure 5-2 and described in the following subsections.

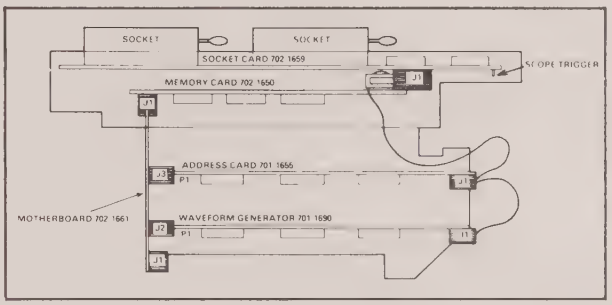


Figure 5-2. Principal Components

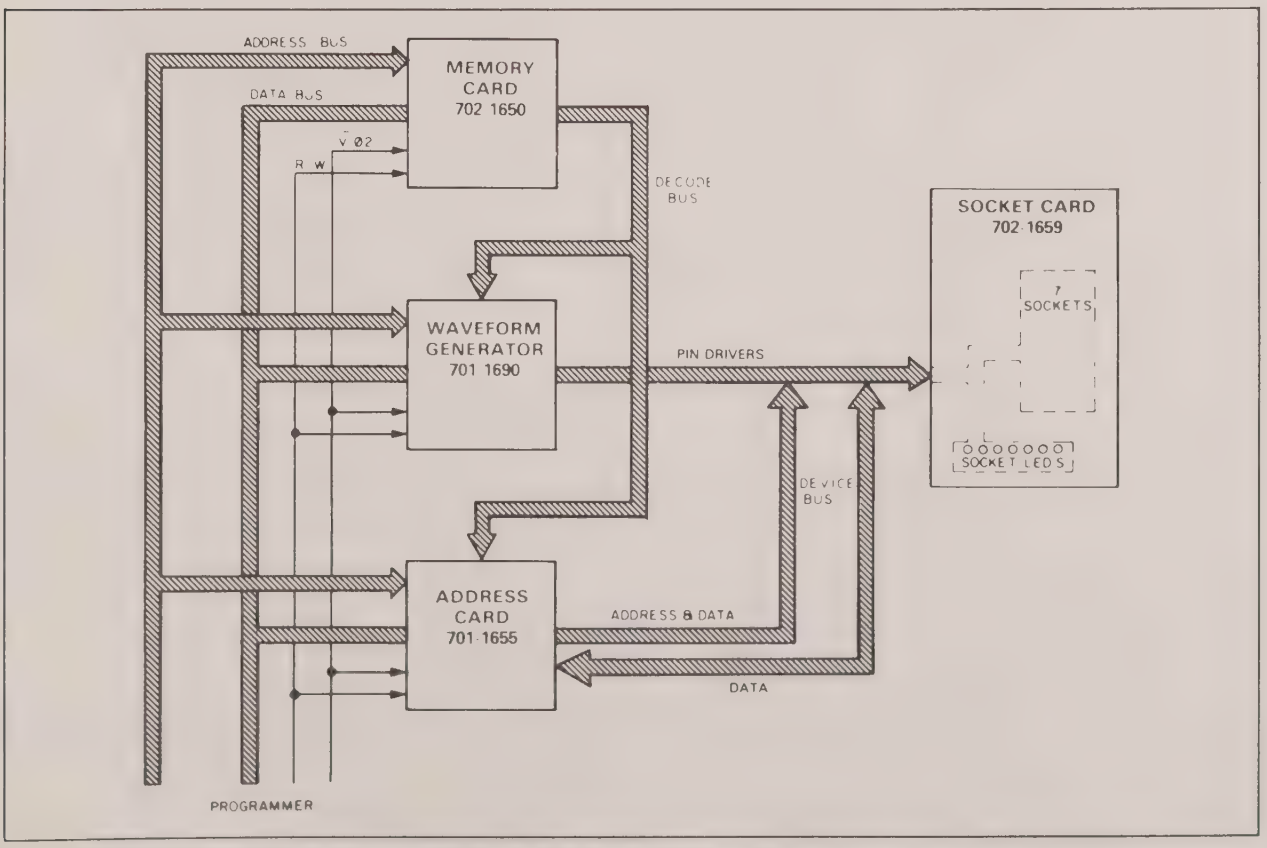


Figure 5-1. Block Diagram, UniPak 2™ Electronics

5.3.1 Motherboard

The motherboard accepts the signals and power supplies from the J6 of the programmer and transmits them to two identical 72-pin edge connectors and a 50-pin edge connector (see figure 5-3 and schematic 30-702-1661).

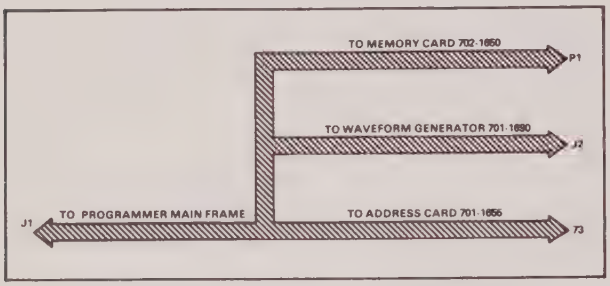


Figure 5-3. Block Diagram, Motherboard

5.3.2 Waveform Generator

The waveform generator provides signals required for programming devices. These signals are generated by the blocks shown in figure 5-4.

Three major supplies are the V_{CC} supply, the $\overline{CE}$ supply and the bit supply, which are used to generate the respective signals. Each supply is software-controlled via a D/A converter. All DACs obtain their reference voltage from the DAC reference.

The V_{CC} waveforms are generated by writing appropriate DAC values from the firmware. The rise and fall times are fixed by the slewing rate of the op amp. Two overcurrent detectors are included, one for low currents and one for high currents (above 1 amp). If a detector is activated, the control latch is reset; the DAC-reference kill output then causes the DAC reference to go to zero, in turn causing all supplies to return to zero.

The V_{CC} supply senses the V_{CC} voltage at the PROM socket via the V_{CC} sense line. This remote sensing compensates for all cable drops between the supply and the socket.

The $\overline{CE}$ waveforms are generated by using the $\overline{CE}$ supply in conjunction with one of the pin switches. The voltage level is selected by writing the appropriate value to the $\overline{CE}$ DAC. One of two rise times is selected by the control latch and rise-time control circuitry. Either the pin 18, 20 or 21 switch can be enabled by the switch-control latch to output the high-level $\overline{CS}$ voltage. Switches that are not enabled can output TTL levels.

Each pin switch consists of an emitter follower with the collector tied to the $\overline{CE}$ supply. A current source is provided for the base of each switch to charge the common rise-time capacitor. When the base is released, a linear ramp is generated which is truncated at the $\overline{CE}$ supply level. An NPN-transistor pulldown is included in the switch to provide a 20V/μs controlled fall time. Logic circuitry prevents the pulldown and pullup circuits from being active simultaneously.

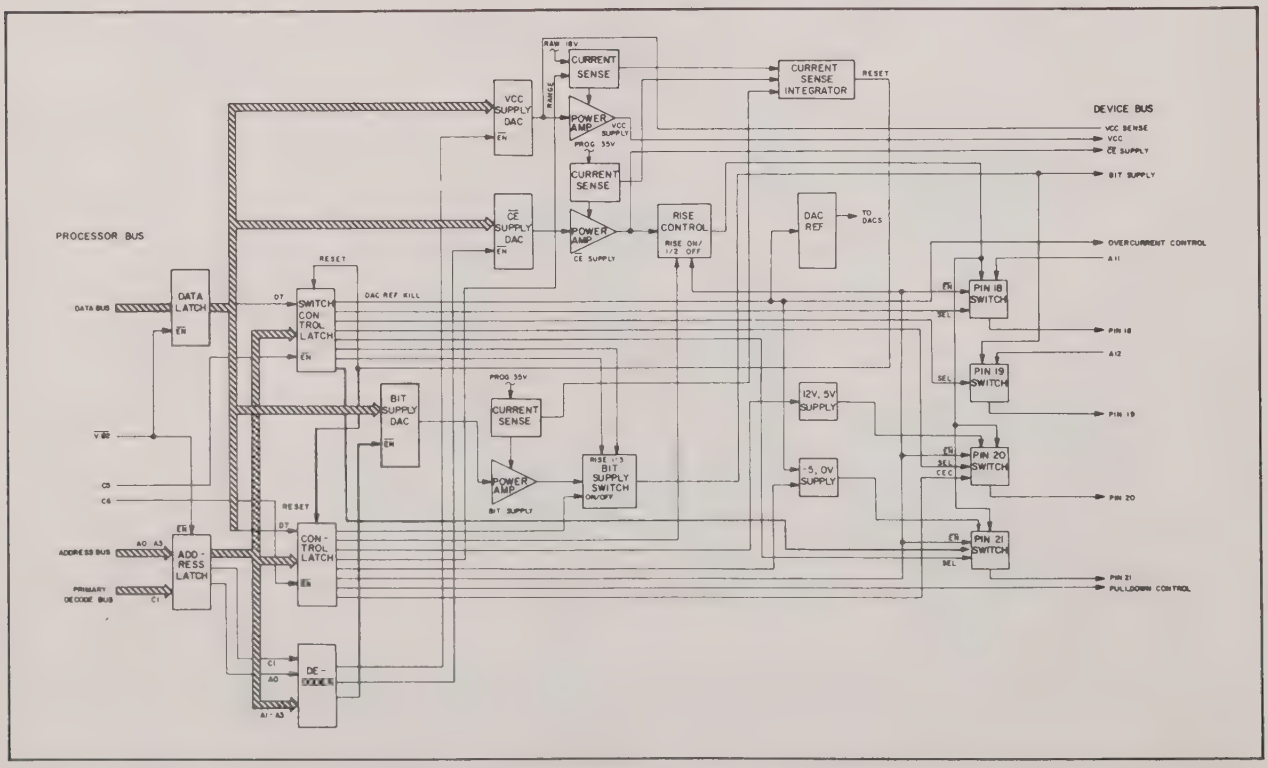


Figure 5-4. Block Diagram, Waveform Generator

The pin 21 switch uses the same principles as the pin 18 and pin 20 switches. However, a power amplifier output (0/-5V supply) provides the ground reference for the switch. For certain programming algorithms this amplifier output is brought to -5V.

The pin 20 switch includes a pullup that is connected to the +12/+5V supply, thus allowing the switch in the TTL mode to switch from 0 to 12V as well as from 0 to 5V. The +12/+5V supply consists of a monolithic regulator and a 5.1V zener diode controlled by the switch-control latch.

Signals to be applied to the data lines of a device are generated with the bit-supply signals and controlled by the bit-supply switch. The bit supply is nearly identical to the $\overline{CE}$ supply, but has one less diode in the feedback path, compensating for one less drop in the switch paths. The bit-supply switch consists of an emitter follower, a current source, and three rise-time control capacitors. The collector of the emitter follower is connected to the bit supply; the base is connected to the current source and timing capacitor. The control latch can select the timing capacitor and also control the base of the switch. When the base is released, the output ramps linearly to the bit-supply level. The output on the bit-supply switch is sent to the address card and to the pin 19 switch; unlike the pin 20, 21 and 18 switches, the pin 19 switch consists of a simple PNP-saturating switch controlled by the switch-control latch.

The current-sense integrator smoothes the transient overcurrent pulses occurring from charging supply capacitors. When an overcurrent condition from the V_{CC}, $\overline{CE}$, bit or (0/-5V) supply exists for sufficient time, the control latch is reset, in turn causing the DAC reference and the supplies to go to zero. The state of the overcurrent-control line can be read by the address card and used by the programmer to detect shorted devices.

Table 5-1 lists the functions of the device-bus pins. The data latch buffers the data bus and holds data to satisfy the long DAC data-hold requirement. The address latch buffers the lower-order address lines and the primary decode bus. These buffered lines are then sent to the decoder and the address latches. The decoder provides decode signals to the DACs for the V_{CC}, $\overline{CE}$ and bit supplies. The switch-control latch and the control latch receive their clocks from a decoder on the address card.

Table 5-1. Pin Functions, Device Bus (at J1)

Pin	Function	Pin	Function
1	PA_8	26	PA_7
2	PA_9	27	PA_6
3	PA_{10}	28	PA_5
4	PA_{11}	29	PA_4
5	PA_{12}	30	PA_3
6	PA_{13}	31	PA_2
7	PA_{14}	32	PA_1
8	PA_{15}	33	PA_0
9	GND	34	V_{CC}
10	V_{CC} Sense	35	GND
11	$\overline{CE}$ Supply	36	GND
12	Bit Switch	37	Bit Supply
13	Pin 20	38	Pin 18
14	Pin 21	39	Pin 19
15	Scope Trigger	40	PD_1
16	9V	41	PD_2
17	+24V	42	PD_4
18	$\overline{\text{Overcurrent}}$	43	PD_4
19	$\overline{\text{Pull-Down Control}}$	44	S1
20	$\overline{V_{CC}\text{ Pull-Up Control}}$	45	S2
21	Address Supply +5V Select	46	$\overline{S3}$
22	PD_8	47	$\overline{V_{CC}\text{ Pulse}}$
23	PD_7	48	Address DAC
24	PD_6	49	+5V
25	PD_5	50	Bit Switch Control

5.3.3 Address Card

The address card, illustrated in figure 5-5, provides the device address, device data, data loads and supply measurement capability of the UniPak 2™.

The address drivers consist of addressable latches driving the device address bus. The addressable latches receive data from the most-significant-bit line of the data bus.

The data switch register drives PNP data switches which direct the output of the bit switch to the appropriate device-data line. The PNP switches are driven by current sources to provide a constant-base drive at all bit-switch voltages.

The data sink register is used to shunt programming currents to ground. Device data is read via the data comparators and strobed to the processor bus via the data gate. The comparators receive their reference voltage from the V_{REF} amplifier, which is controlled by the V_{REF} DAC. Loading the device data bus is controlled by the load DAC, the load amplifier and the high/low-range load switch. This supply develops a voltage that is applied to either the low-range or high- and low-range load resistor banks. These resistors are fed through isolation diodes, which are connected to the device data pins. The load sink register enables the UniPak 2™ to select which device data pins will have loads applied to them. The diode clamps limit the voltage applied by the load resistors to the data bus to approximately 5V when the load clamp switch is closed.

The supply comparators read the V_{CC}-sense line, the $\overline{CE}$ supply and the bit-switch line. The comparator gate/multiplexer strobes the data from the supply comparators and the overcurrent-read line to the most significant-bit line of the data bus.

The socket-select latch provides a control line for the high-/low-range switch and control lines for the socket card.

The data latch buffers the data bus and holds data to satisfy the DAC requirements.

The current source latch will supply a 4-mA current to a device provided there is a 15V zener diode inside the device on pin 18, 19 or 20. The address supply 5V select determines whether the address supply DAC or a fixed 5V will be applied to PA0-PA3.

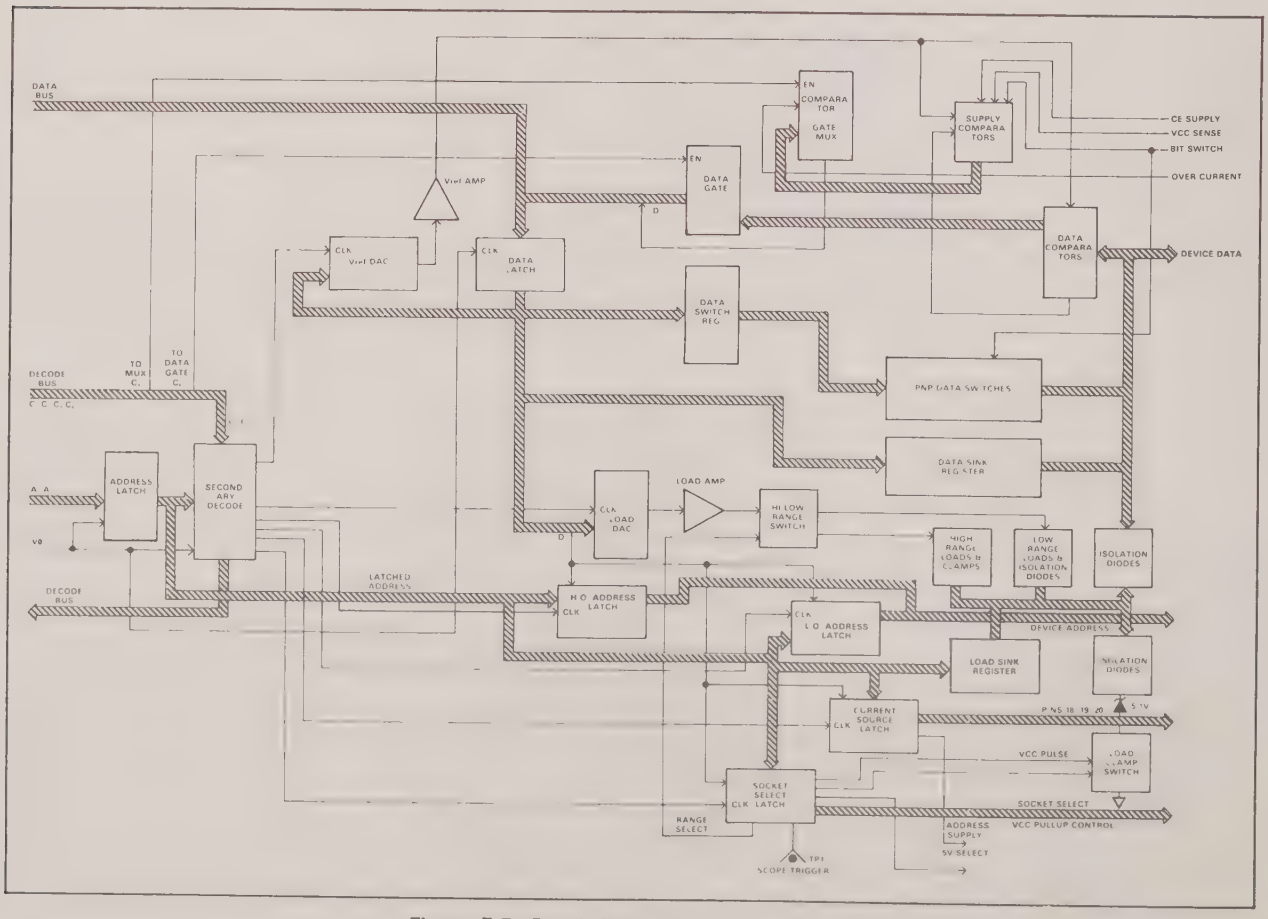


Figure 5-5. Block Diagram, Address Card

The address latch buffers low-order addresses for the secondary decoder. The secondary decoder provides the appropriate signals for the DACs and registers, as well as the latches on this card and on the waveform generator. The $\overline{V \bullet \emptyset_2}$ signal controls the timing of the various clock signals developed by the decoder.

5.3.4 UniPak 2™ Socket Card

The socket card distributes to the device sockets the signals developed on the address card and the waveform generator (refer to figure 5-6).

The device address bus (PA0-PA15) is generated on the address card and fed to the socket card via the ribbon cable. On the socket card, the bus is fed into CMOS buffers. The address supply DAC connects to the V_{DD} supply on these buffers. This allows the VOH level to be under DAC control. The address supply 5V select line allows PA0-PA3 to switch at TTL levels while all other address lines switch between "0" and the address supply level. The address clamps provide overvoltage protection and are connected to a comparator that senses overvoltage, shutting down all the supplies when excessive voltage is detected.

The device-data bus connects directly to all sockets. Four-bit devices are connected to PD1-PD4. The data pulldowns consist of 1K-ohm resistors and a diode network. The data clamp has two modes of operation controlled by the bit switch control line.

When voltage pulses are being applied to a device, the pass element of the data clamp is switched out of the circuit. The op amp and 2.2K-ohm resistor precharge the 0.1 μF capacitors to the level set by the bit supply so that the network does not absorb energy from the actual data-line programming pulses.

When current pulses are being applied to a device, the pass element is switched into the circuit. The data clamp will be set to a voltage level by the bit supply and will sink all unnecessary current.

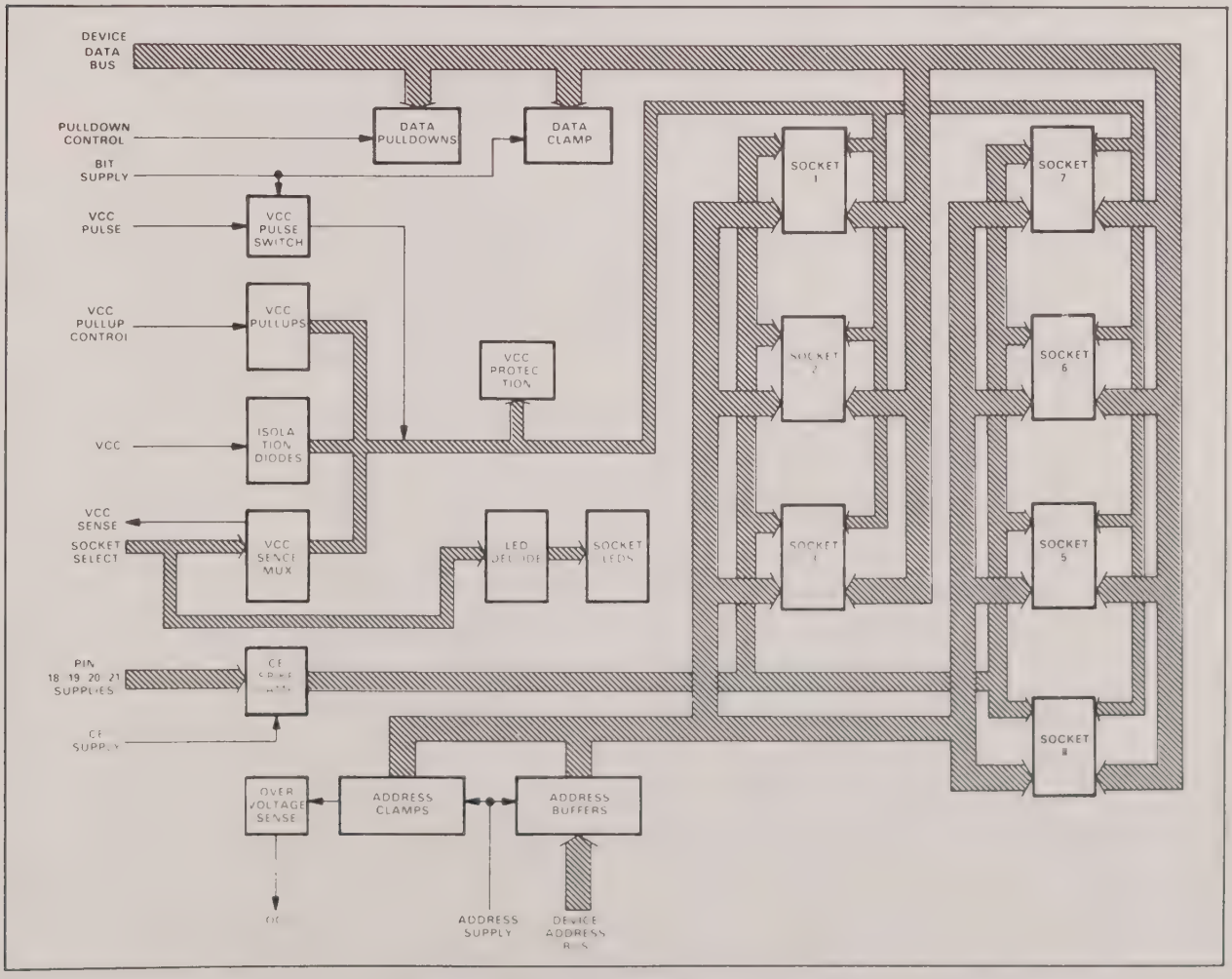


Figure 5-6. Block Diagram, Socket Card

Pins 18, 19, 20 and 21 of the 24-pin device socket receive signals directly from the waveform generator via the corresponding pin switches. A spike-suppression network is provided where the $\overline{CE}$ supply charges the RC network. V_{CC} is applied to all sockets through seven diodes. Remote sensing of the voltage at the selected socket is provided by the analog switch of the V_{CC}-sense multiplexer. When V_{CC} is brought to zero, the device's V_{CC} lines can be pulled up by the V_{CC} pullups. The V_{CC} sense-multiplexer and a comparator on the address card are then used to read the V_{CC} voltage. If a device is properly inserted in a socket, the V_{CC} voltage will be above 2V. If it is in backwards it will be below 1V, and if no device is in the socket, the voltage will approach 4V.

The V_{CC} pulse switch is used to switch from a level set by the V_{CC} supply to a level set by the bit supply. The switch uses a HEX JFET with an RC network to control the rise and fall times. When the HEX FET is switched on, the V_{CC} isolation diode is reversed biased and the V_{CC} sense line sees a dummy load. The V_{CC} pulse switch is applied only to the 24-pin socket. When the switch is on, the .01 μF decoupling capacitor for the 24-pin socket is switched off.

The LED decoder is used to light the LEDs below the selected socket.

5.3.5 Memory Card

The UniPak 2™ memory card is shown in figure 5-7. EPROMs which store the UniPak 2™ firmware are contained on the memory card. These EPROMs connect to the address bus directly and to the data bus through data buffers.

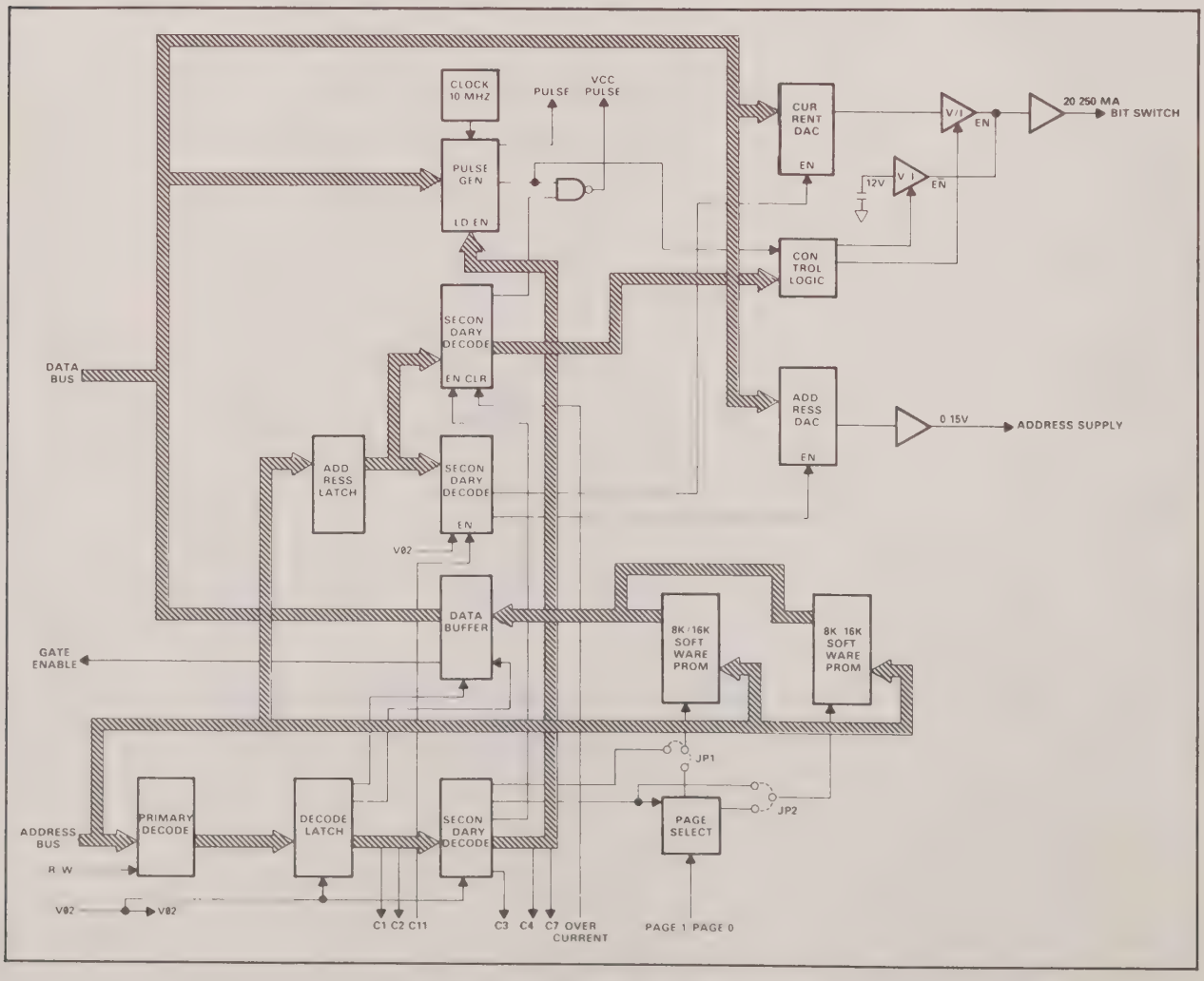


Figure 5-7. Block Diagram, Memory Card

Paging is used when the 16K x 8 PROMs are installed. Two EPROMs and a latch comprise the primary decoding for the entire UniPak 2™. The EPROMs connect to the 12 high-order address lines and the R/$\overline{W}$ line. Outputs from the primary-decoder latch connect to the secondary decoder and also to secondary decoders on the address card and the waveform generator. A 1-of-8 decoder, timed with $\overline{V \bullet \emptyset_2}$, provides the secondary decoding for the software EPROMs. Two additional lines from this decoder connect to the address card to provide the decode signals for the data gate and comparator gate/multiplexer. Additional outputs from the binary decoder enable the data buffer during all software-read operations and lower the data gate enable line during any access of the UniPak 2™.

The pulse generator consists of a count-up ripple counter, an 8-bit latch, and a 10-mHz crystal-controlled clock. The latch is connected to the data bus and is used to load the counter, allowing the pulse generator to be programmable between 0.1 and 25.5 μs.

The current source consists of a fixed 20-mA current source and a programmable current source. The control logic selects which current source is active. The pulse generator can be selected to control the programmable current source.

The address supply generates the voltage necessary to drive the CMOS buffers located on the socket card. The voltage is generated from the 24V power supply using an NPN transistor driven by an op amp. The input of the op amp is a DAC, which allows the voltage to be software selectable.

APPENDIX A
FAMILY AND PINOUT CODES
ERROR CODES

KEY TO HEADINGS AND FOOTNOTES

- **Device Part Number.** The number assigned by the device manufacturer.
- **Family Code.** A 2-digit number that designates the programming algorithm.
- **Pinout Code.** A 2-digit number used to differentiate device types based on pin assignment and array size.
- **Software Version.** A number in this column specifies the earliest software version of the 22A that will program the device to the manufacturer's latest specifications.
- **Approval Status.** The following is an explanation of the symbols used in this column.

  A - Written approval obtained.

  O - Device is obsolete and no longer in production. No approval can be obtained. Algorithm has been used and approved in previous Data I/O equipment.

  S - This algorithm is in the process of submission for manufacturer approval. The algorithm has been tested by Data I/O or the manufacturer, but no representation as to yield level is made or implied.

CAUTION

Entry of an invalid family/pinout code, other than those listed in this table can cause unpredictable results at the device socket, which may damage a device. A valid family code and a valid pinout code may be combined to produce an invalid (illegal) combination. The correct combination for your device is published in this table. All family/pinout combinations not contained in this table are considered "illegal". Data I/O assumes no responsibility or liability for results produced by entry of "illegal" family/pinout combinations.

Table A-1. UniPak™ Family and Pinout Codes

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Advanced Micro Devices					
2708	21	27	A	-	A
27128	AF	51	005	-	A
27128A	C1	51	V07	-	A
2716	19	23	A	-	A
27256	C1	32	V07	-	S
2732	19	24	A	-	A
2732A	27	24	005	-	A
27512	DD	A4	V07	-	A
2764	AF	33	005	-	A
2764A	C1	33	V07	-	A
27LS18	16	02	A	-	A
27LS185	16	08	E	-	A
27LS19	16	02	A	-	A
27PS181	16	37	A	-	A
27PS184	16	06	A	-	A
27PS185	16	06	E	-	A
27PS191	16	68	H	-	A
27PS281	16	37	003	-	A
27PS291	16	68	003	-	A
27PS41	16	53	005	351A-065	A
27PS43	16	63	004	-	A
27PS49	16	67	003	-	A
27S08	15	02	A	-	O
27S09	15	02	A	-	O
27S10	15	01	A	-	O
27S11	15	01	A	-	O
27S12	16	03	A	-	A
27S13	16	03	A	-	A
27S15	16	79	005	351A-068	A
27S18	16	02	A	-	A
27S180	16	37	A	-	A
27S181	16	37	A	-	A
27S184	16	06	E	-	A
27S185	16	06	E	-	A
27S19	16	02	A	-	A
27S190	16	68	H	-	A
27S191	16	68	H	-	A
27S20	16	01	A	-	A
27S21	16	01	A	-	A
27S24	16	65	003	-	A
27S25	16	65	003	-	A
27S26	16	85	005	351A-067	A
27S27	16	85	005	351A-067	A
27S28	16	09	E	-	A
27S280	16	37	003	-	A
27S281	16	37	003	-	A
27S29	16	09	A	-	A
27S290	16	68	003	-	A
27S291	16	68	003	-	A
27S30	16	36	A	-	A
27S31	16	36	A	-	A
27S32	16	38	E	-	A
27S33	16	38	E	-	A
27S35	16	66	004	-	A
27S37	16	66	004	-	A
27S40	16	53	004	351A-065	A
27S41	16	53	004	351A-065	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Advanced Micro Devices (Continued)					
27S43	16	63	004	-	A
27S45	16	77	004	351A-066	A
27S47	16	77	004	351A-066	A
27S49	16	67	003	-	A
27S65	16	93	V07	351A-073	A
27S75	16	94	V07	351A-073	A
27S85	16	95	V07	351A-073	A
9864	C9	A6	V07	-	A
9864-3	C9	A6	V07	-	S
29750A	16	02	A	-	A
29751A	16	02	A	-	A
29760A	16	01	A	-	A
29761A	16	01	A	-	A
29770	16	03	A	-	A
29771	16	03	A	-	A
29774	16	85	005	351A 067	S
29775	16	85	005	351A 067	S
AM9708	21	27	A	-	A
AM9716	19	23	A	-	A
AM9732	19	24	A	-	A
AM9764	AF	33	005	-	A
Electronic Arrays					
2708	21	27	A	-	A
2716	19	23	A	-	A
Eurotechnique					
ET2716	19	23	005	-	A
ET2732	19	24	005	-	A
ETC2716	19	23	005	-	A
ET2764	35	33	V07	-	S
Exel					
2816A	B7	23	V07	-	S
Fairchild					
2708	21	27	A	-	A
93417	01	01	A	-	A
93427	01	01	A	-	A
93436	01	03	A		A
93438	01	15	A	-	A
93446	01	03	A	-	A
93448	01	15	A		A
93450	01	16	A		A
93451	01	16	A		A
93452	01	05	A	-	A
93453	01	05	A	-	A
93460	01	16	A	-	A
93461	01	16	A		A
93510	01	21	004	-	A
93511	01	21	004	-	A
93514	01	06	A	-	A
93515	01	06	A		A
93L450	01	16	A		A
93L451	01	16	A		A
Fujitsu					
27128	45	51	005		S
2732A	27	24	F		A
2732A-35	27	24	C		A
2764	45	33	005		A

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Fujitsu (Continued)					
27C128	45	51	005	-	S
27C256	45	32	V07	-	S
27C32A	27	24	A	-	A
27C64	45	33	005	-	A
8516	19	23	E	-	A
8518	21	27	E	-	A
8532	19	24	F	-	A
8742	50	57	005	351A-070	S
8749H	50	57	005	351A-070	S
General Instruments					
5716	83	23	003	-	A
5816	37	23	003	-	A
Harris					
6641	40	47	F	-	A
7602	05	02	A	-	A
7603	05	02	A	-	A
7608	05	16	A	-	A
7610	05	01	A	-	A
7611	05	01	A	-	A
7616	05	42	A	-	A
76160	05	21	A	-	O
76161	05	21	A	-	A
76165	05	53	004	351A-065	A
7620	05	03	A	-	A
7621	05	03	A	-	A
7629	05	43	A	-	O
76320	05	63	H	-	O
76321	05	63	H	-	A
7640	05	15	A	-	A
7641	05	15	A	-	A
7642	05	05	A	-	A
7642P	05	38	H	-	O
7643	05	05	A	-	A
7643P	05	38	H	-	O
7644	05	04	A	-	O
7647R	05	79	V07	351A-068	S
7648	05	09	A	-	A
7649	05	09	A	-	A
76641	05	67	H	-	A
7680	05	16	A	-	A
7680RP	05	16	H	-	O
7681	05	16	A	-	A
7681RP	05	16	H	-	O
7684	05	06	A	-	A
7684P	05	06	H	-	O
7685	05	06	A	-	A
7685P	05	06	H	-	O
7686	05	10	A	-	A
7687	05	10	V01	-	A
Hitachi					
27C32	19	24	A	-	O
27C32A	27	24	A	-	O
462532	19	25	E	-	A
462716	19	23	F	-	A
462732	19	24	F	-	A
462732P	19	24	A	-	A
48016	33	23	E	-	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Hitachi (Continued)					
4827128	79	51	004	-	A
482732A	27	24	A	-	A
482764	79	33	004	-	A
Hughes					
3004-1	58	62	004	-	A
3004-2	58	61	004	-	A
3008	58	60	004	-	A
3104-1	58	62	004		A
3104-2	58	61	004	-	A
3108	58	60	004	-	A
Intel					
2704	21	26	A	-	O
2708	21	27	A	-	O
27128	79	51	004	-	A
27128A	93	51	005	-	A
2716	19	23	A	-	A
27256	93	32	005	-	A
2732	19	24	A	-	A
2732A	27	24	A	-	A
27512	4B	A4	V09	-	S
2758	19	22	A	-	A
2764	79	33	004	-	A
2764A	93	33	005	-	A
2815	85	23	005	-	A
27C64	93	33	V05	-	S
2816	37	23	H	-	A
2816A	A5	96	V07	-	A
2817A	BF	A2	V07	-	A
8704	21	26	A	-	A
8708	21	27	A	-	A
8741	56	59	005	351A-070	S
8741A	56	59	005	351A-070	S
8742	50	57	V07	351A-070	S
8744	53	58	V04	351A-071	S
8748	52	56	005	351A-070	S
8748H	50	56	005	351A-070	S
8749H	50	57	005	351A-070	S
8751	53	58	005	351A-071	S
8751H	D5	58	V07	351A-071	S
8755A	47	55	005	351A-072	S
Intersil					
6716	59	64	004	-	A
Mitsubishi					
2708	21	27	A		A
27128	79	51	004		S
2716	19	23	A		A
2732	19	24	A	-	A
2732A	27	24	A		A
2764	79	33	004		A
8748	52	56	V07	351A-070	S
Monolithic Memories					
5300	11	01	D		A
	E5	01	V09		S

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Monolithic Memories (Continued)					
5301	11	01	D	-	A
	E5	01	V09	-	S
5305	11	03	D	-	A
	E5	03	V09	-	S
5306	11	03	D	-	A
	E5	03	V09	-	S
5308	11	08	D	-	A
	D1	08	V07	-	A
5309	11	08	D	-	A
	D1	08	V07	-	A
5330	29	02	D	-	A
	E7	02	V09	-	S
5331	29	02	D	-	A
	E7	02	V09	-	S
5335	11	14	D	-	A
	D1	14	V07	-	A
5336	11	14	D	-	A
	D1	14	V07	-	A
5340	11	15	D	-	A
	D1	15	V07	-	A
5340JS	11	15	D	-	A
	D1	15	V07	-	A
5341	11	15	D	-	A
	D1	15	V07	-	A
5341JS	11	15	D	-	A
	D1	15	V07	-	A
5348	11	09	D	-	A
	D1	09	V07	-	A
5349	11	09	D	-	A
	D1	09	V07	-	A
5352	11	05	D	-	A
	D1	05	V07	-	A
5353	11	05	D	-	A
	D1	05	V07	-	A
5380	11	16	D	-	A
	D1	16	V07	-	A
5380JS	11	16	D	-	A
	D1	16	V07	-	A
5381	11	16	D	-	A
	D1	16	V07	-	A
5381JS	11	16	D	-	A
	D1	16	V07	-	A
5388	11	06	D	-	A
	D1	06	V07	-	A
5389	11	06	D	-	A
	D1	06	V07	-	A
53LS080	18	02	004	-	O
53LS081	18	02	004	-	O
53S080	18	02	004	-	O
53S081	18	02	004	-	O
6300	11	01	D	-	A
	E5	01	V09	-	S
6301	11	01	D	-	A
	E5	01	V09	-	S
6305	11	03	D	-	A
	E5	03	V09	-	S

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Monolithic Memories (Continued)					
6306	11	03	D	-	A
	E5	03	V09	-	S
6308	11	08	D	-	A
	D1	08	V07	-	A
6309	11	08	D	-	A
	D1	08	V07	-	A
6330	29	02	D	-	A
	E7	02	V09	-	S
6331	29	02	D	-	A
	E7	02	V09	-	S
6335	11	14	D	-	A
	D1	14	V07	-	A
6336	11	14	D	-	A
	D1	14	V07	-	A
6340	11	15	D	-	A
	D1	15	V07	-	A
6340JS	11	15	D	-	A
	D1	15	V07	-	A
6341	11	15	D	-	A
	D1	15	V07	-	A
6341JS	11	15	D	-	A
	D1	15	V07	-	A
6348	11	09	D	-	A
	D1	09	V07	-	A
6349	11	09	D	-	A
	D1	09	V07	-	A
6352	11	05	D	-	A
	D1	05	V07	-	A
6353	11	05	D	-	A
	D1	05	V07	-	A
6380	11	16	D	-	A
	D1	16	V07	-	A
6380JS	11	16	D	-	A
	D1	16	V07	-	A
6381	11	16	D	-	A
	D1	16	V07	-	A
6381JS	11	16	D	-	A
	D1	16	V07	-	A
6388	11	06	D	-	A
	D1	06	V07	-	A
6389	11	06	D	-	A
	D1	06	V07	-	A
63D1641	B2	80	V07	351A-073	A
63D1642	B2	80	V07	351A-073	A
63DA1643	AA	87	V07	351A-073	A
63DA441	AA	AC	V07	351A-073	A
63DA841	AA	AD	V07	351A-073	A
63DS1643	AA	87	V07	351A-073	A
63LS080	18	02	004	-	A
63LS081	18	02	004	-	A
63LS140	18	01	004	-	A
63LS141	18	01	004	-	A
63LS240	18	03	004	-	A
63LS241	18	03	004	-	A
63PL1681	18	21	V07	-	A
63PS1681	18	21	005	-	A
63RA1681	18	A3	V07	-	A

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Monolithic Memories (Continued)					
63RA441	18	07	004	-	A
63RA481	EC	65	V09	-	S
63RA841	18	11	004	-	A
63RS1681	18	A3	V07	-	A
63RS881	18	86	005	-	A
63S080	18	02	004	-	A
63S081	18	02	004	-	A
63S140	18	01	004	-	A
63S141	18	01	004	-	A
63S1640	18	53	004	351A-065	A
63S1641	18	53	005	351A-065	A
63S1680	18	21	004	-	A
63S1681	18	21	004	-	A
63S1681J	18	21	004	-	A
63S240	18	03	004	-	A
63S241	18	03	004	-	A
63S3281	18	63	005	-	A
63S440	18	05	004	-	A
63S441	18	05	004	-	A
63S480	18	09	004	-	A
63S481	18	09	004	-	A
63S840	18	06	004	-	A
63S841	18	06	004	-	A
63S881	18	16	004	-	A
Mostek					
2716	19	23	A	-	A
Motorola					
68732-0	25	44	A	-	O
68732 1	25	45	A	-	O
76161	05	21	A	-	A
76165	05	53	003	351A-065	S
7620	05	03	A	-	O
7621	05	03	A	-	A
7640	05	15	A	-	O
7641	05	15	A	-	A
7642	05	05	A	-	O
7643	05	05	A	-	A
7649	05	09	A	-	A
7680	05	16	A	-	O
7681	05	16	A	-	A
7684	05	06	A	-	O
7685	05	08	A	-	A
MCM2532	19	25	B	-	A
6836E16	2D	5A	V09	-	S
MCM2708P	21	27	A	-	O
MCM2716	19	23	B	-	A
MCM2808	81	72	003	-	A
MCM2816	43	23	003	-	A
MCM2817	81	71	003	-	A
MCM2832	81	70	003	-	A
MCM68708	21	27	A	-	A
MCM68764	25	29	F	-	A
MCM68766	25	29	F	-	A
TMS2716	23	28	A	-	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
National Semiconductor					
2532	19	25	A	-	A
25C32	19	25	A	-	A
2708	21	27	A	-	A
2716	19	23	A	-	A
2732	19	24	A	-	A
2758A	19	22	A	-	A
2758B	19	35	A	-	A
2764	35	33	F	-	S
2764H	63	33	V07	-	S
27C16	19	23	E	-	A
27C16H	BD	23	V07	-	S
27C32	19	24	A	-	A
2864	C7	A5	V09	-	S
27C32H	BD	24	V07	-	S
2816	37	23	003	-	A
54LS471	08	08	A	-	O
54S188	08	02	A	-	O
54S287	08	01	A	-	O
54S288	08	02	A	-	O
54S387	08	01	A	-	O
54S471	08	08	A	-	O
54S472	08	09	A	-	O
54S473	08	09	A	-	O
54S474	08	15	A	-	A
54S475	08	15	A	-	A
54S570	08	03	A	-	O
54S571	08	03	A	-	O
54S572	08	05	A	-	A
54S573	08	05	A	-	A
74LS471	08	08	A	-	A
74S188	08	02	A	-	A
74S287	08	01	A	-	A
74S288	08	02	A	-	A
74S387	08	01	A	-	A
74S471	08	08	A	-	A
74S472	08	09	A	-	A
74S473	08	09	A	-	A
74S474	08	15	A	-	A
74S475	08	15	A	-	A
74S570	08	03	A	-	A
74S571	08	03	A	-	A
74S572	08	05	A	-	A
74S573	08	05	A	-	A
74S574	08	34	A	-	A
77LS181	08	16	A		A
77S180	08	16	A	-	A
77S184	08	06	A	-	A
77S185	08	06	A	-	A
87LS181	08	16	A	-	A
87S180	08	16	A	-	A
87S181	08	16	A	-	A
87S184	08	06	A	-	A
87S185	08	06	A		A
87S190	08	21	A		A
87S191	08	21	A		A
87S195	08	53	004		A

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
National Semiconductor (Continued)					
87S280	08	16	003	-	A
87S281	08	16	003	-	A
87S290	08	21	003	-	A
87S291	08	21	003	-	A
87S295	08	15	A	-	A
87S296	08	15	A	-	A
87S321	08	63	004	-	A
87SR181	08	66	V07	-	A
87SR25	08	81	005	-	A
87SR191	08	77	V09	351A-066	S
87SR474	08	81	V07	-	A
9716	B3	23	005	-	A
87SR27	08	85	V09	351A-067	S
Nippon Electric Company, Ltd.					
27128	79	51	004	-	S
2716	19	23	F	-	A
2732	19	24	F	-	A
2732A	27	24	A	-	A
2764	79	33	004	-	S
8741AD	56	59	005	351A-070	S
8748AD	52	56	005	351A-070	S
8755A	47	55	005	351A-072	S
Oki					
2532	19	25	A	-	A
2708	21	27	A	-	A
27128	79	51	004	-	S
2716	19	23	A	-	A
2732	19	24	A	-	A
2732A	27	24	A	-	A
2758	19	22	A	-	A
2764	79	33	004		S
8755A	47	55	005	351A-072	S
Raytheon					
29600	11	08	D	-	A
29601	11	08	D	-	A
29602	11	08	D	-	A
29603	11	08	D	-	A
29610	11	03	D	-	A
29611	11	03	D	-	A
29612	11	03	D	-	A
29613	11	03	D	-	A
29620	11	09	D	-	A
29621	11	09	D	-	A
29622	11	09	D	-	A
29623	11	09	D	-	A
29624	11	15	D	-	A
29625	11	15	D	-	A
29626	11	15	D	-	A
29627	11	15	D		A
29630	11	16	D	-	A
29630SM	11	16	003	-	A
29631	11	16	D	-	A
29631SM	11	16	003	-	A
29632	11	16	D	-	A
29632SM	11	16	003		A
29633	11	16	D		A
29633SM	11	16	003	-	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Raytheon (Continued)					
29634	11	16	D	-	A
29635	11	16	D	-	A
29636	11	16	D	-	A
29637	11	16	D	-	A
29640	11	53	004	351A-065	A
29641	11	53	004	351A-065	A
29642	11	53	004	351A-065	A
29643	11	53	004	351A-065	A
29650	11	06	D	-	A
29651	11	06	D	-	A
29652	11	06	D	-	A
29653	11	06	D	-	A
29660	11	01	D	-	A
29661	11	01	D	-	A
29662	11	01	D	-	A
29663	11	01	D	-	A
29671	11	63	H	-	A
29673	11	63	H	-	A
29680	11	21	D	-	A
29680SM	11	21	003	-	A
29681	11	21	D	-	A
29681SM	11	21	003	-	A
29682	11	21	D	-	A
29682SM	11	21	003	-	A
29683	11	21	D	-	A
29683SM	11	21	003	-	A
Ricoh					
RD5H32	27	24	F	-	A
Rockwell					
R87C32	27	24	V07	-	S
87C64	93	33	V07	-	S
Seeq					
27C256	93	32	V07	-	S
5133	79	33	005	-	A
5133H	79	33	005	-	A
5143	79	51	005	-	S
2816A	B7	23	V07	-	S
2816AH	DF	23	V09	-	S
5516A	B7	23	V07	-	S
5516AH	DF	23	V09	-	S
2817A	BF	A2	V07	-	S
5517A	BF	A2	V07	-	S
2817AH	BF	A2	V07	-	S
5517AH	BF	A2	V07	-	S
5213	A5	96	V07	-	A
5213H	B9	96	V07	-	A
52B13	A5	96	V07	-	A
52B13H	B9	96	V07	-	A
52B23	AB	97	V07	-	A
52B23H	F1	97	V07	-	A
52B33	AB	98	V07	-	A
52B33H	F1	98	V07	-	A
SGS Technology					
2532	19	25	003	-	A
2716	19	23	V03	-	A
2764	35	33	V07	-	A

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Signetics					
2708	21	27	A	-	A
82123	10	02	A	-	A
82LS135	10	08	A	-	A
82LS137	10	06	A	-	A
82HS195	CF	53	V09	351A-065	S
82LS180	10	16	A	-	A
82LS181	10	16	003	-	A
82PS180	10	16	A	-	A
82PS181	10	16	003	-	A
82HS321	CF	63	V09	-	S
82S123	10	02	A	-	A
82S126	10	01	A	-	A
82S129	10	01	A	-	A
82S130	10	03	A	-	A
82S131	10	03	A	-	A
82S135	10	08	A	-	A
82S136	10	05	A	-	A
82S137	10	05	A	-	A
82S140	10	15	A	-	A
82S141	10	15	A	-	A
82S146	10	09	A	-	A
82S147	10	09	A	-	A
82S180	10	16	A	-	A
82S181	10	16	A	-	A
82S182	10	16	A	-	A
82S183	10	16	A	-	A
82S184	10	06	A	-	A
82S185	10	06	A	-	A
82S190	10	21	A	-	A
82S191	10	21	A	-	A
82S195	10	53	004	351A-065	A
82S23	10	02	A	-	A
82S2708	10	16	A	-	A
82S321	10	63	004	-	A
27C64	35	33	F	-	S
Synertek					
2716	19	23	A	-	A
Texas Instruments					
14S10	03	01	A	-	A
14SA10	03	01	A	-	A
18S030	04	02	A	-	A
18S22	04	08	A	-	A
18S42	04	09	A	-	A
18S46	04	15	A	-	A
18SA030	04	02	A	-	A
18SA22	04	08	A	-	A
18SA42	04	09	A	-	A
18SA46	04	15	A	-	A
24S10	13	01	A	-	A
24S166	13	53	005	351A-065	S
24S41	13	38	A	-	A
24S81	13	06	A	-	A
24SA10	13	01	A	-	A
24SA166	13	53	005	351A-065	S
24SA41	13	38	A	-	A
24SA81	13	06	A	-	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Texas Instruments (Continued)					
2508	19	22	A	-	A
2516	BD	23	V07	-	A
2532	BD	25	V07	-	A
2564	BD	30	V07	-	A
25L32	19	25	A	-	A
2708	21	27	A	-	A
27128	79	51	005	-	S
2732	BD	24	V07	-	A
2732A	63	24	V07	-	A
2764	79	33	F	-	S
27L08	21	27	A	-	A
28L166	13	21	G	-	A
28L22	13	46	G	-	A
28L42	13	09	G	-	A
28L45	13	15	G	-	S
28L85	13	16	G	-	S
28L86	13	16	A	-	A
28LA22	13	46	G	-	A
28P166	13	21	G	-	S
28P42	13	09	G	-	S
28P45	13	15	G	-	S
28P85	13	16	G	-	S
28S166	13	21	G	-	A
28S2708	13	16	A	-	A
28S42	13	09	A	-	A
28S45	13	15	G	-	A
28S46	13	15	G	-	A
28S85	13	16	G	-	S
28S86	13	16	A	-	A
28SA166	13	21	G	-	S
28SA42	13	09	G	-	A
28SA46	13	15	G	-	A
28SA86	13	16	A	-	A
54LS478	13	16	A	-	O
54S476	13	38	A	-	A
54S477	13	38	A	-	A
54S478	13	16	A	-	A
54S479	13	16	A	-	A
74188A	04	02	A	-	O
74S188	04	02	A	-	A
74S2708	13	16	A	-	O
74S287	03	01	A	-	O
74S288	04	02	A		O
74S387	03	01	A		O
74S454	13	06	A		O
74S455	13	06	A		O
74S470	04	08	A	-	O
74S471	04	08	A		O
74S472	04	09	A	-	O
74S473	04	09	A		O
74S474	04	15	A		O
74S475	04	15	A		O
74S476	13	38	A		O
74S477	13	38	A		O
74S478	13	16	A		O
74S479	13	16	A		O
TMS2716	23	28	A		A

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Thompson					
71190	92	21	004	-	A
71191	92	21	004	-	A
Toshiba					
27128	79	51	004	-	S
2732	19	24	A	-	A
2732A	27	24	A	-	A
2732D	19	24	A	-	A

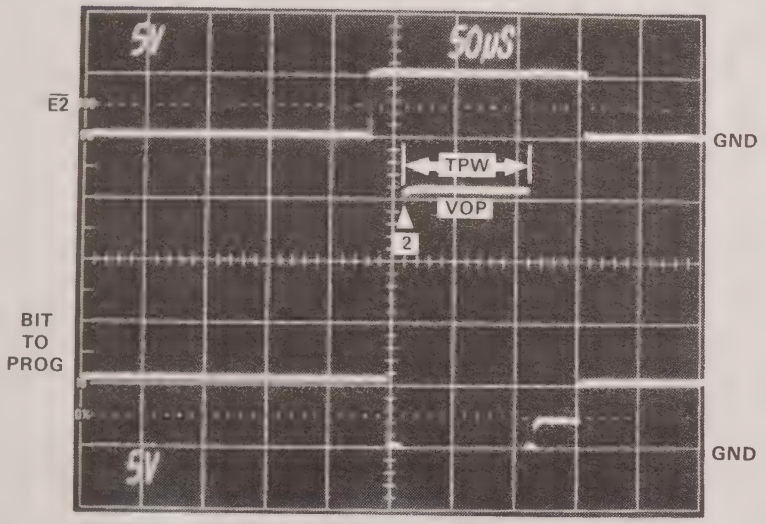
Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Toshiba (Continued)					
2764	79	33	004	-	S
321	21	26	A	-	A
322	21	27	A	-	A
323	19	23	A	-	A
8755AC	47	55	005	351A-072	S
Xicor					
2804A	B7	82	V07	-	S
2816A	B7	23	V07	-	S
2864A	C3	98	V07	-	S

Table A-2. Error Codes*

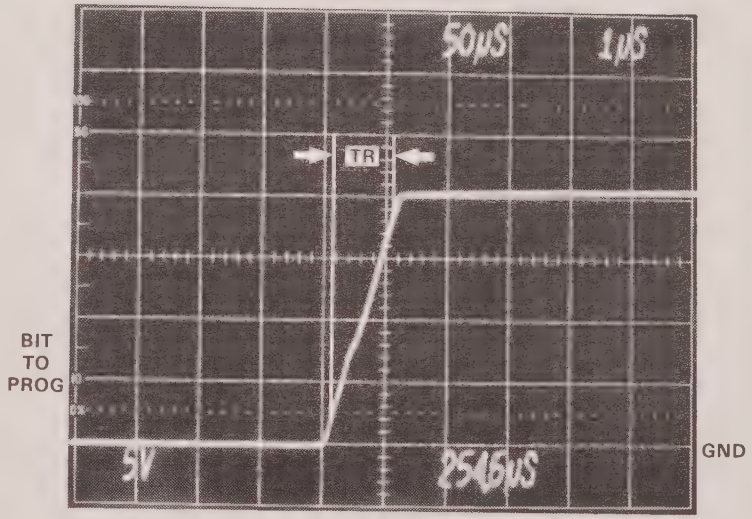
CODE	NAME	DESCRIPTION
21	Illegal-Bit Error	The device cannot be programmed due to already programmed locations of incorrect polarity.
23	First-Pass Verify Error	The device data was incorrect on the first pass of the automatic verify sequence during device programming.
24	Second-Pass Verify Error	The device data was incorrect on the second pass of the automatic verify sequence during device programming.
27	Insufficient RAM	Due to the value of the Begin RAM Address, there is insufficient RAM to program the device, or the total allotment of RAM resident is less than the word limit of the device.
30	No Programming Algorithm	Valid family and pinout codes are not selected, or family code selection is not followed by pinout code selection.
31	Excessive Current Drain	The operation aborted due to excessive current drain by a device.
32	Backward Device	The operation aborted due to V_{CC} level test indicating a backward device.
35	Faulty Chip Select	The operation aborted due to data being present while a device is disabled.
37	Socketing Error	Operation aborted due to a low V_{CC} level indication on sockets presumed to be empty. A device may be in the wrong socket, or two or more devices may be socketed simultaneously.
38	Illegal Operation During Calibration	An illegal or invalid operation was attempted during calibration.
39	Failure to Lock Security Fuse	The security bit did not program and the device is not locked.
70	Faulty Bit Supply	The operation aborted due to a faulty bit supply. Do not use UniPak™ until repaired.
71	Faulty CS Supply	The operation aborted due to a faulty CS supply. Do not use UniPak™ until repaired.
72	Faulty V_{CC} Supply	The operation aborted due to a faulty V_{CC}. Do not use UniPak™ until repaired.
B0	Byte Erase Error	The device does not have a byte erase mode. Block limits must be removed and a chip erase performed. The entire chip may then be reprogrammed.
B1	Chip Erase Error	The device does not have a chip erase mode.

*In the case of an error condition, be sure that the family and pinout codes are correct for the PROM installed; refer to table A-1 in this appendix to cross check family and pinout codes.

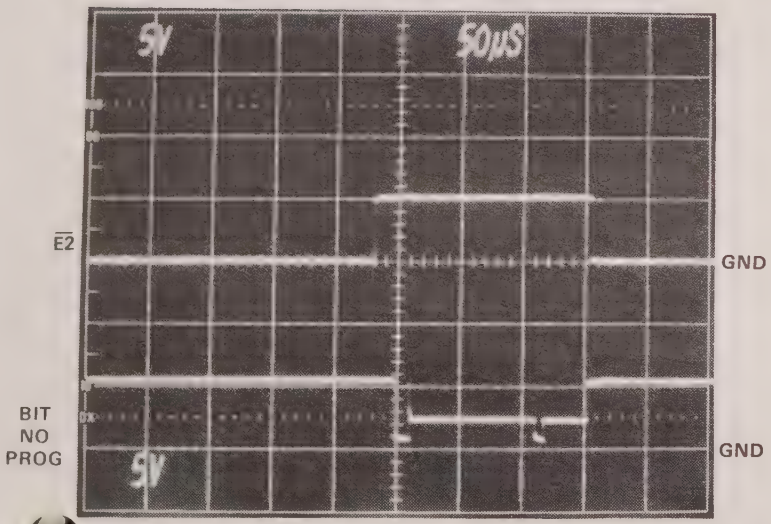
APPENDIX B
TIMING DIAGRAMS


5V
50µS
$\overline{E2}$
GND
TPW
VOP
2
BIT
TO
PROG
GND
5V

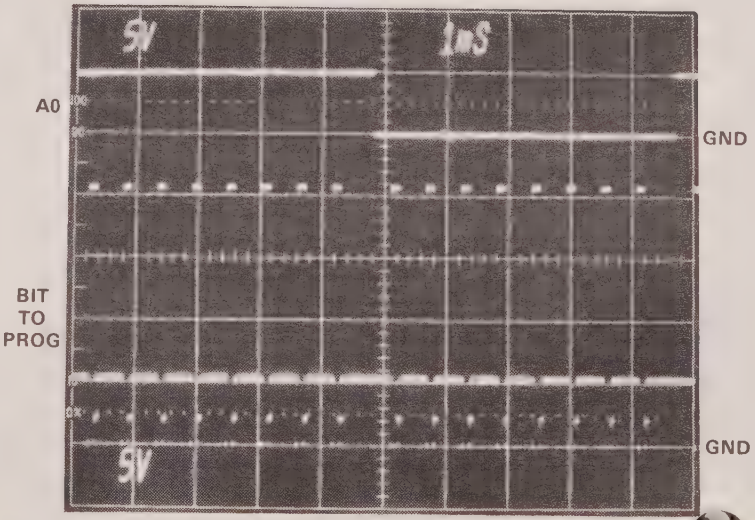
1


50µS
1µS
TR
BIT
TO
PROG
5V
GND
254µS

2


5V
50µS
$\overline{E2}$
GND
BIT
NO
PROG
GND
5V

3


5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4 75	5.0	5.25	V	Not Shown
	VOP	20 0	20.5	21.0	V	
	TPW	90	100	110	µs	
	TR	0.5	1.0	3.0	µs	
	TF					NA
	Reject		8		Pulses	
	Overprogram		0		Pulses	
1ST PASS	VCC	4.3	4.4	4.5	V	
VERIFY	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3
2ND PASS	VCC	4.9	5.0	5.1	V	
VERIFY	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 01.*
2. *Load RAM with hex 01 for Family 02.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJJ	11/82
		ECN #4831		KH	5/83
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 01, 02

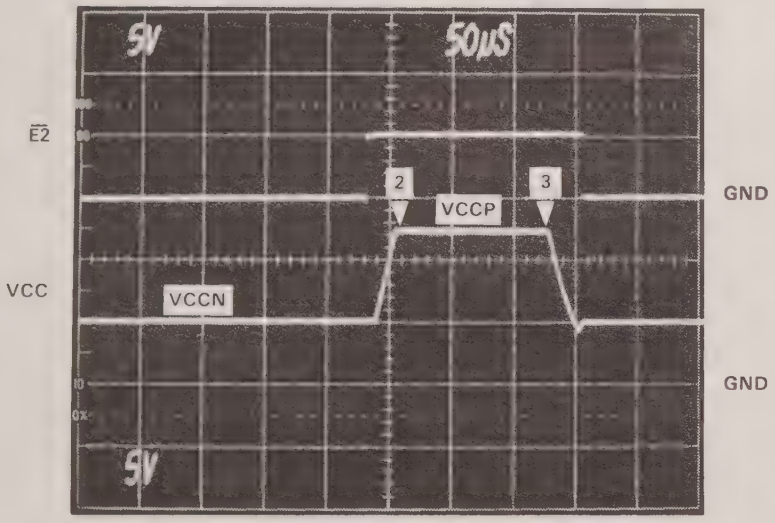
DRAWN BY: KAP

CHECKED BY:

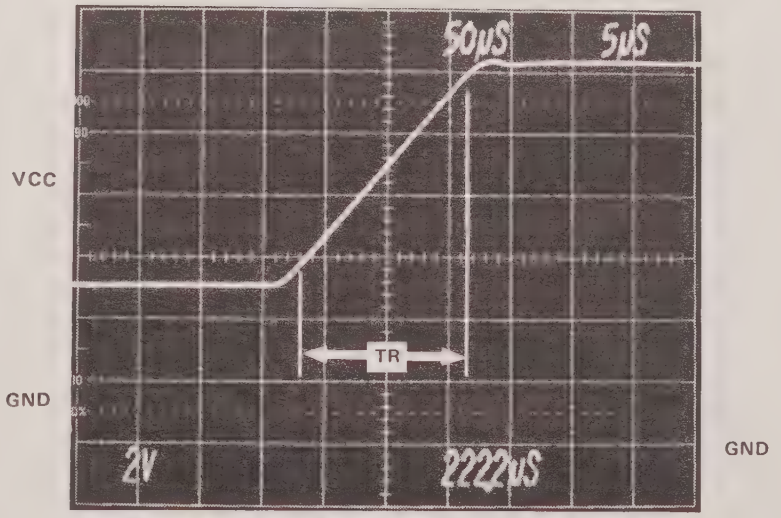
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

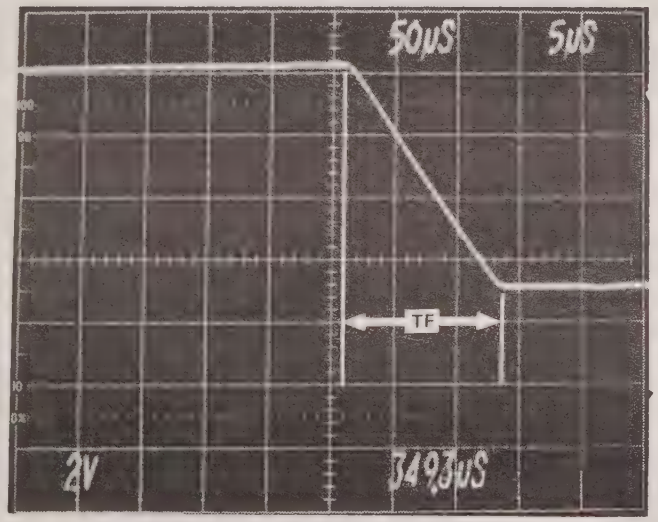
SHEET 1/1


5V
50µS
E2
2
VCCP
3
GND
VCC
VCCN
GND
5V

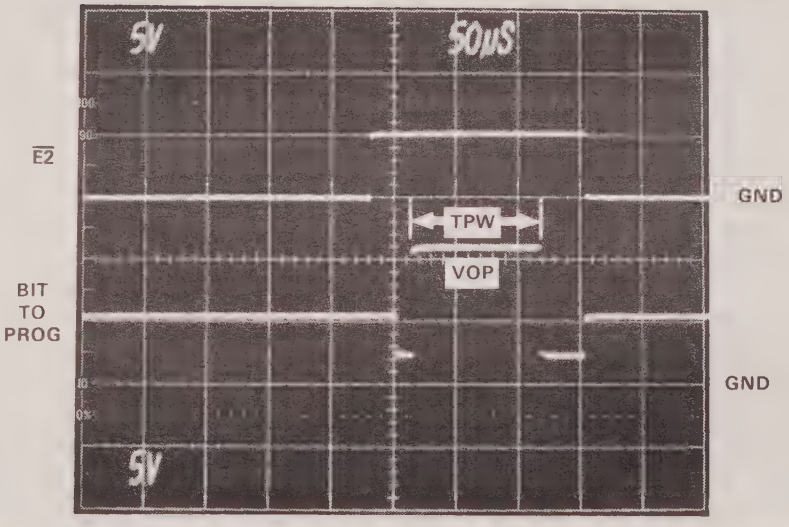
1


50µS
5µS
VCC
TR
GND
2V
2222µS
GND

2


50µS
5µS
VCC
TF
2V
3493µS

3


5V
50µS
E2
GND
TPW
VOP
BIT
TO
PROG
GND
5V

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	12 0	12 0	12 5	V	
	VCCN	4 75	5 0	5 25	V	
	VOP	10 5	10.5	11 0	V	
	TPW	90	100	110	µs	
	T_R	1 0		25	µs	See note 3
	T_F	1.0		25	µs	See note 3
	Reject		8		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	15.5	16.5	17.5	V	701-1655/TP4
	Low Load	15.5	16.5	17.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	1.6	1.7	1.8	V	701-1655/TP2
	High Load	12.5	13.5	14.5		701-1655/TP4
	Low Load	12.5	13.5	14.5		701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 05.*
2. *Load RAM with hex 01 for Family 06.*
3. *Load V_{CC} with a 330 Ω ½-watt resistor.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		KH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 05, 06

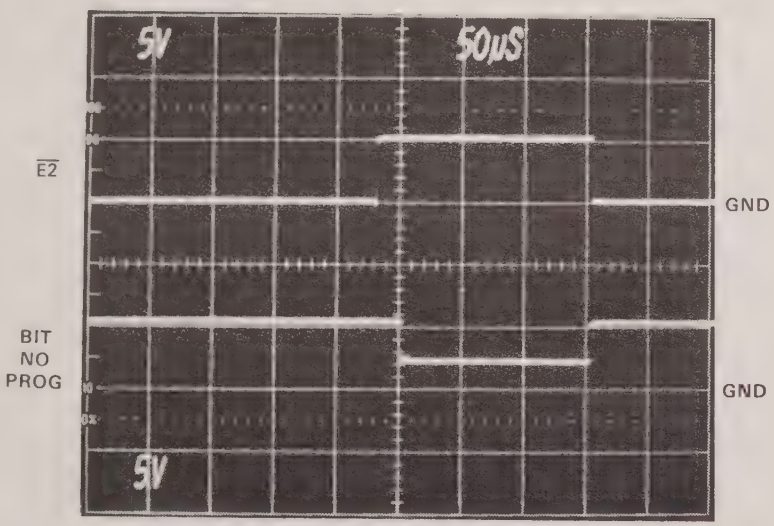
DRAWN BY:

CHECKED BY:

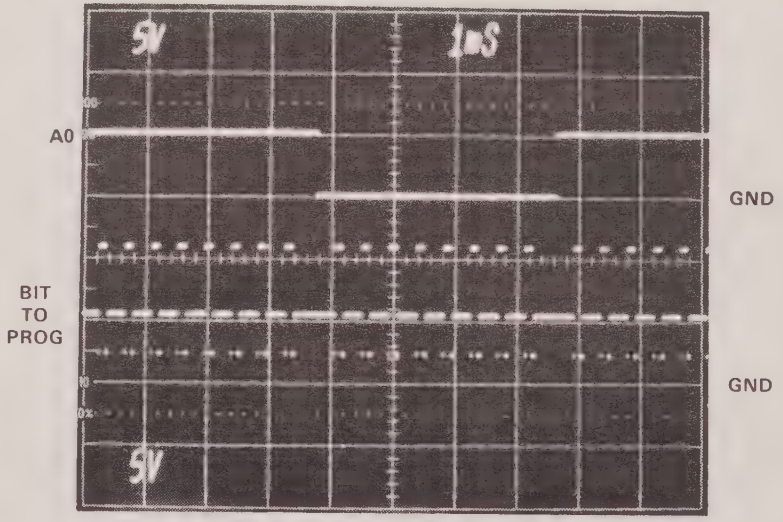
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


5V
50µS
$\overline{E2}$
GND
BIT
NO
PROG
GND
5V

5

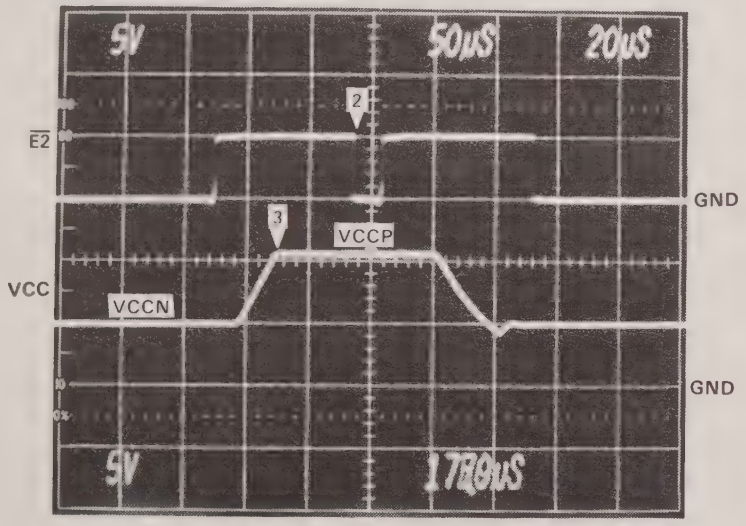

5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

6

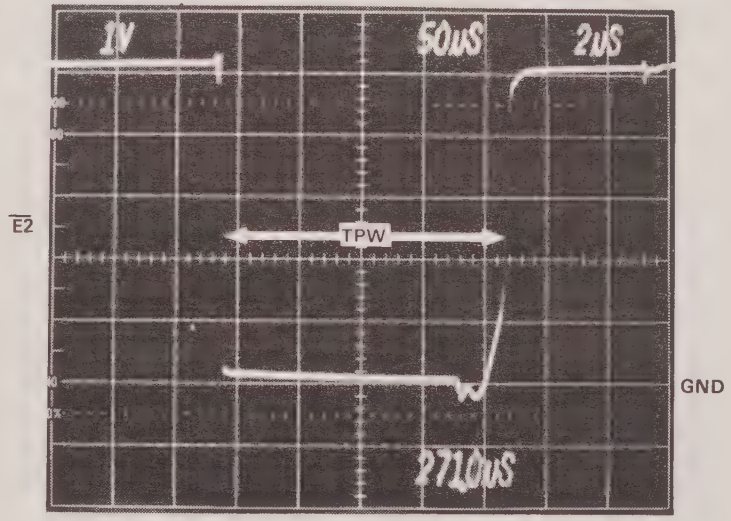
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C TJ.	11/82
		ECN #4831		KK	5/83
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

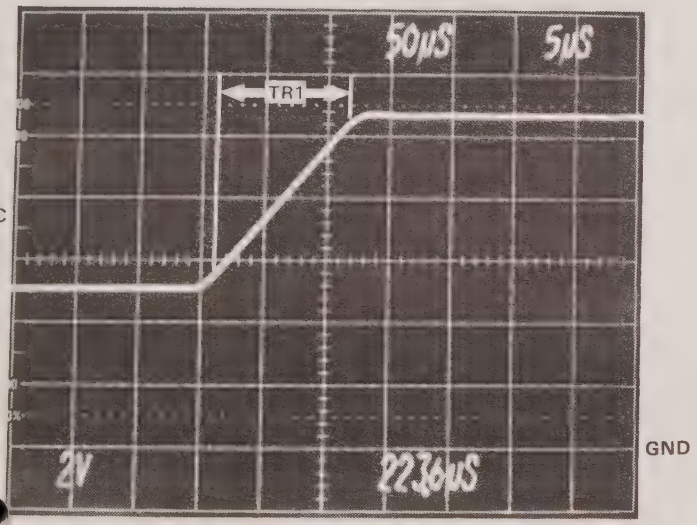
TITLE: TIMING DIAGRAM FAMILY CODES 05, 06			DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2


5V
50µS
20µS
2
E2
GND
3
VCCP
VCC
VCCN
GND
5V
1780µS

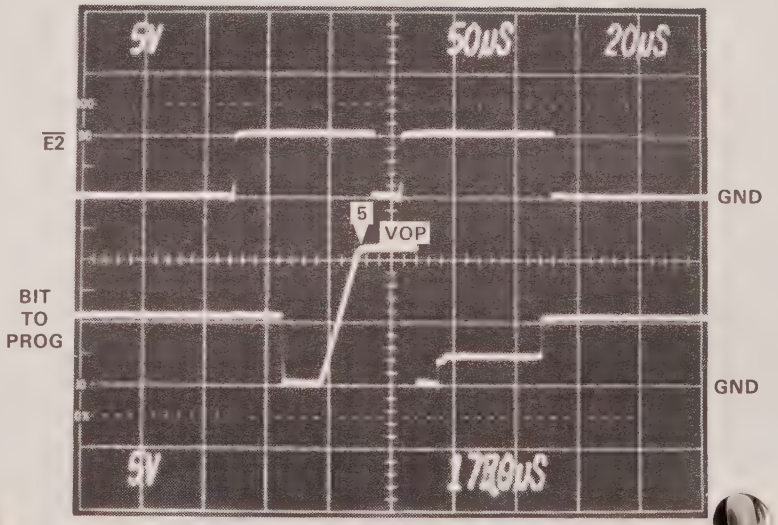
1


1V
50µS
2µS
E2
TPW
GND
2710µS

2


50µS
5µS
TR1
VCC
GND
2V
2236µS

3


5V
50µS
20µS
E2
GND
5
VOP
BIT
TO
PROG
GND
5V
1780µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	10.0	10.5	11.0	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	10.0	10.5	11.0	V	
	TPW	9.0	10.0	11.0	µs	
	TR1	1		25	µs	See note 3
	TR2	1		15	µs	
	TF					NA
	Reject		14		Pulses	
	Overprogram		5		Pulses	
1ST PASS VERIFY	VCC	3.9	4.0	4.1	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	6.9	7.9	8.9	V	701-1655/TP4
	Low Load	6.9	7.9	8.9	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	1.6	1.7	1.8	V	701-1655/TP2
	High Load	6.0	7.0	8.0	V	701-1655/TP4
	Low Load	6.0	7.0	8.0	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 07.*
2. *Load RAM with hex 01 for Family 08.*
3. *Load V_{CC} with a 330 Ω ½-watt resistor.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		XH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 07, 08

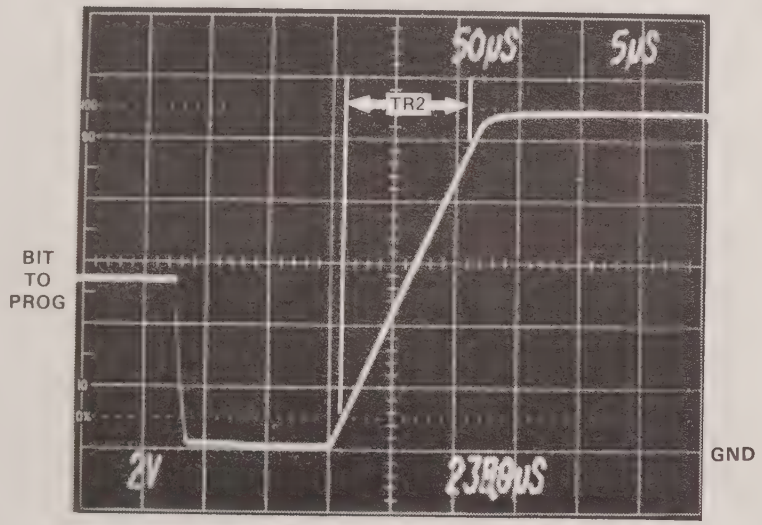
DRAWN BY: ES

CHECKED BY:

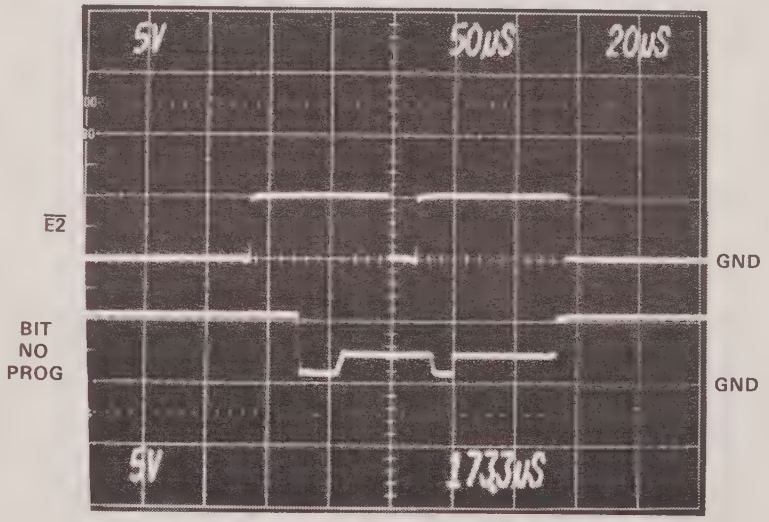
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

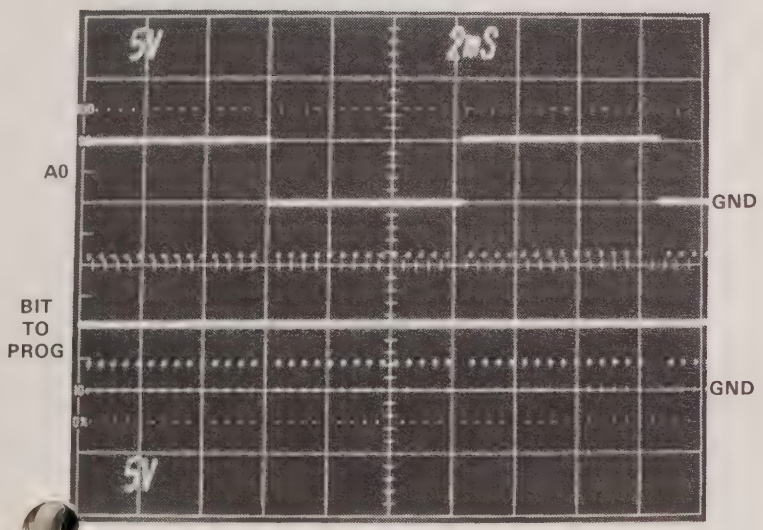
SHEET 1/2


50µS
5µS
TR2
BIT
TO
PROG
2V
GND

5


5V
50µS
20µS
E2
GND
BIT
NO
PROG
GND
5V

6

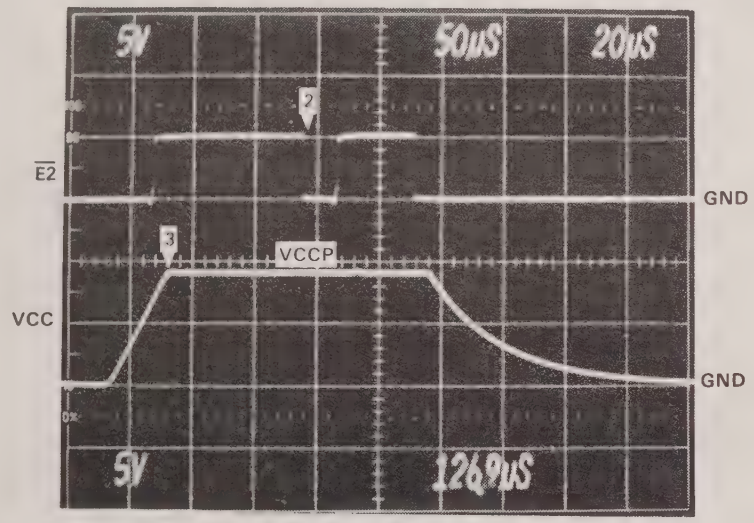

5V
2mS
A0
GND
BIT
TO
PROG
GND
5V

7

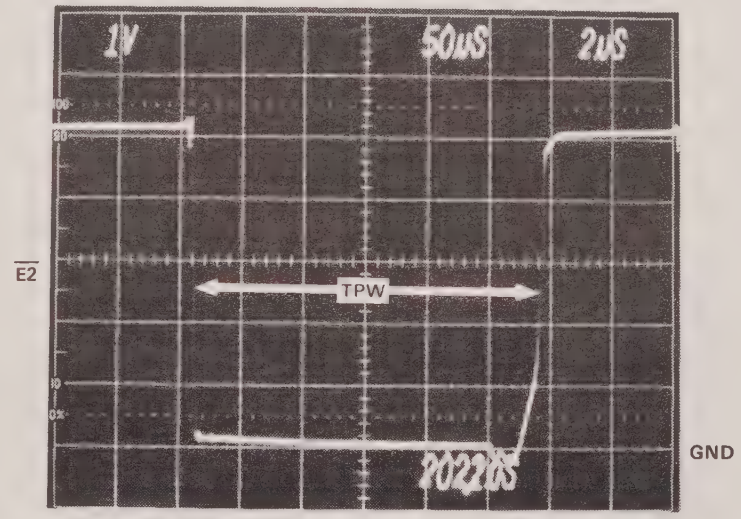
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.S.Z.	11/82
		ECN #4831		ZR	5/83

DATA I/O ISSAQUAH, WA

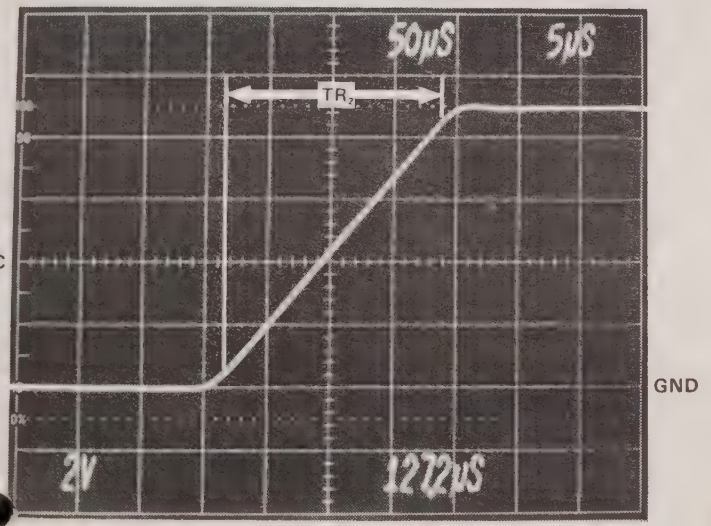
TITLE: TIMING DIAGRAM FAMILY CODES 07, 08		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
50µS
20µS
2
E2
GND
3
VCCP
VCC
GND
5V
126.9µS

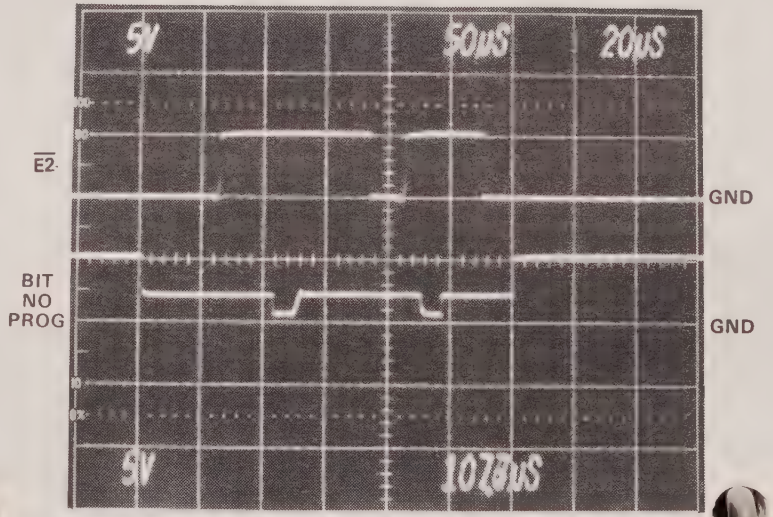
1


1V
50µS
2µS
E2
TPW
GND
202.2µS

2


50µS
5µS
TR2
VCC
GND
2V
127.2µS

3


5V
50µS
20µS
E2
GND
BIT
NO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	8.5		9.0	V	
	VOP	17.0	17.5	18.0	V	
	TPW	10		15	µs	
	TR1	15		20	µs	
	TR2	5		30	µs	See note 3
	TF	0.2		10	µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 09.*
2. *Load RAM with hex 01 for Family 10.*
3. *Load V_{CC} with a 330 Ω ½-watt resistor.*

B-13
10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		XX	5/83
		ECN #5023		CJJ	3/84

DATA I/O ISSAQUAH, WA

TITLE: **TIMING DIAGRAM**

FAMILY CODES 09, 10

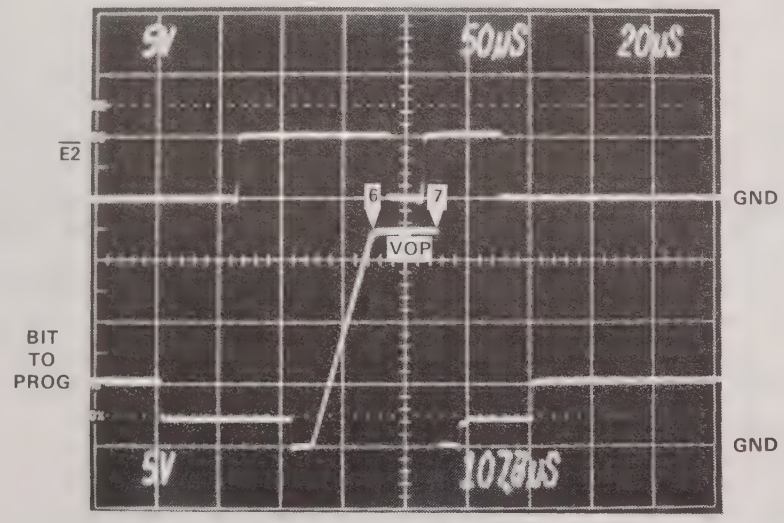
DRAWN BY: ES

CHECKED BY:

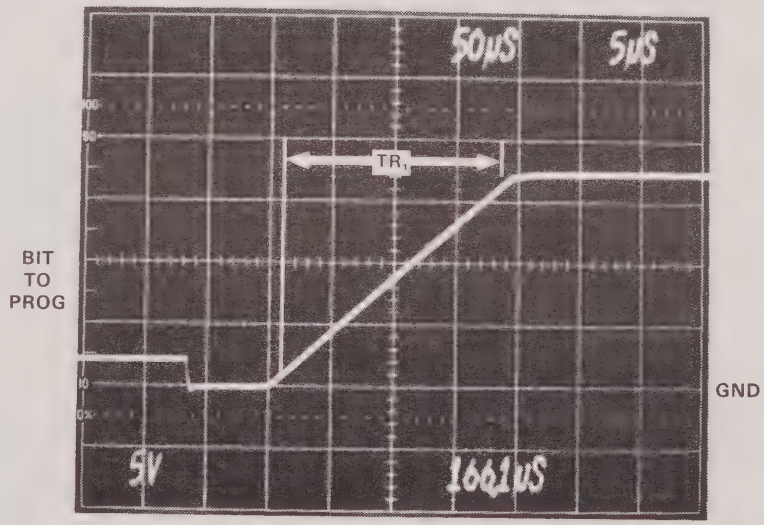
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

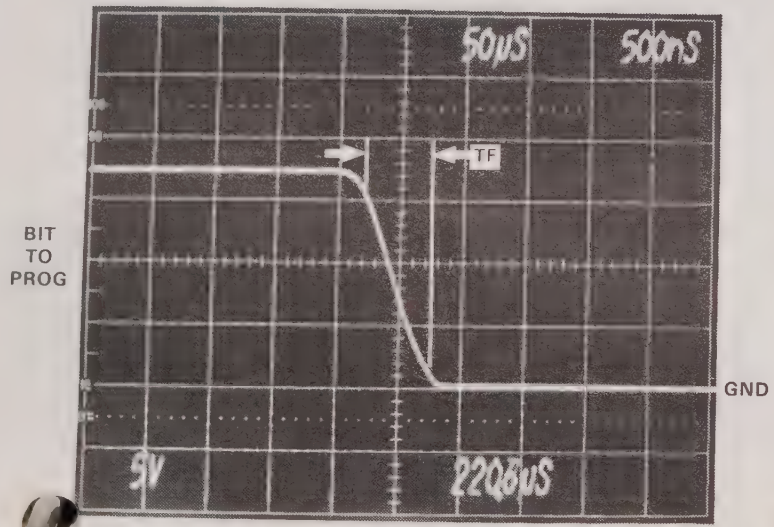
SHEET 1/2


5V
50µS
20µS
E2
6
7
VOP
GND
BIT
TO
PROG
GND
5V
1078µS

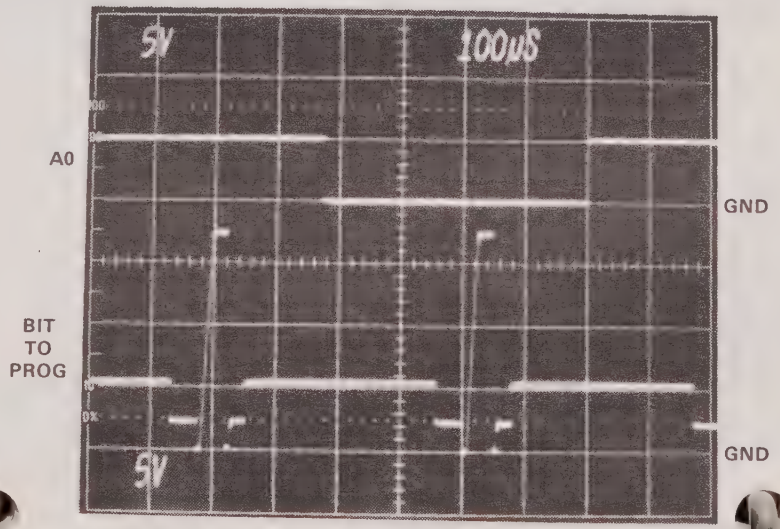
5


50µS
5µS
TR1
BIT
TO
PROG
GND
5V
1661µS

6


50µS
500nS
TF
BIT
TO
PROG
GND
5V
2206µS

7

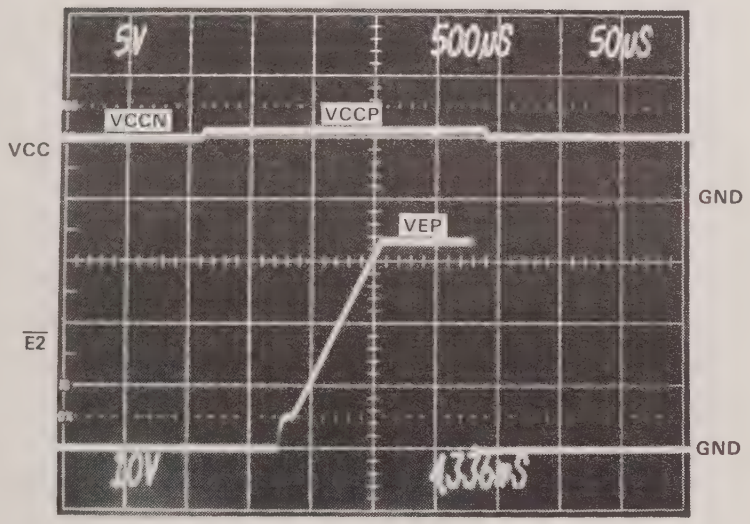

5V
100µS
A0
GND
BIT
TO
PROG
GND
5V

8

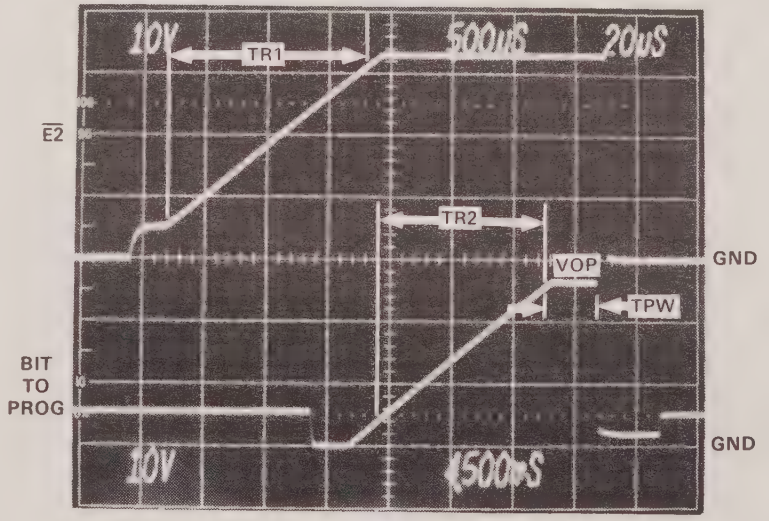
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

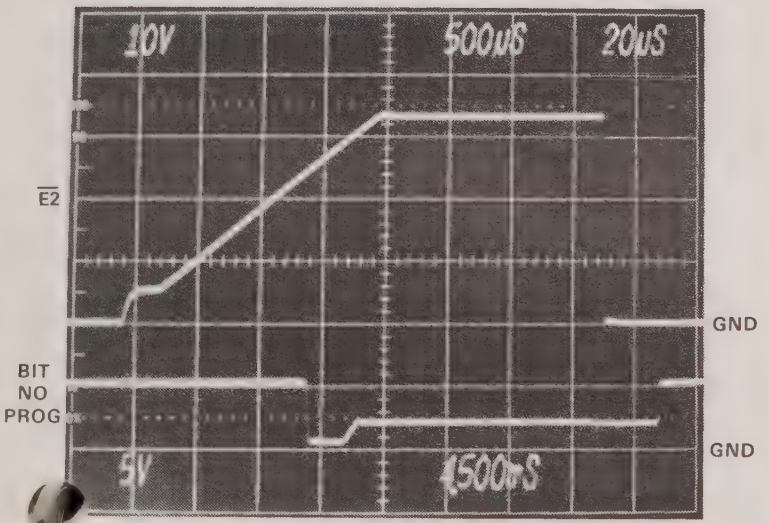
TITLE: TIMING DIAGRAM			DRAWN BY: ES
FAMILY CODES 09, 10			CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2


5V
500µS
50µS
VCCN
VCCP
VCC
GND
VEP
E2
10V
4336µS
GND

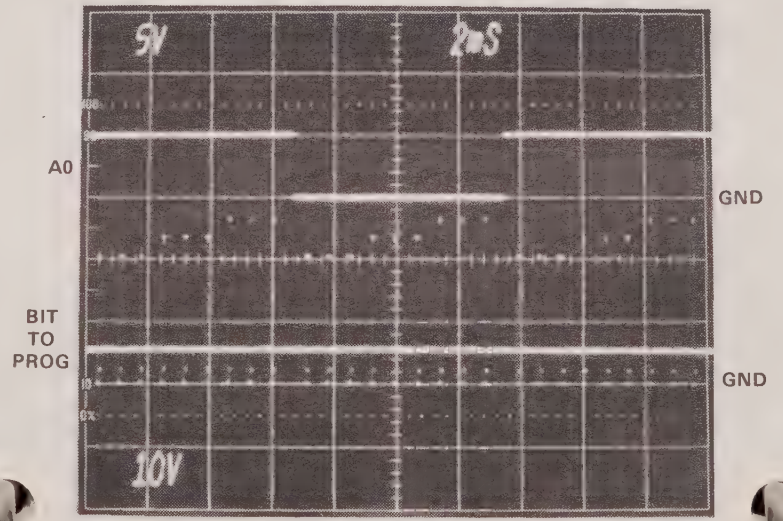
1


10V
TR1
500µS
20µS
E2
TR2
VOP
GND
TPW
BIT
TO
PROG
10V
4500µS
GND

2


10V
500µS
20µS
E2
GND
BIT
NO
PROG
5V
4500µS
GND

3


5V
2mS
A0
GND
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.4	5.5	5.6	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	19	20	21	V	Pulses 1-3
		22	23	24	V	Pulses 4-6
		25	26	27	V	Pulses 7-9
	VEP	26	27	28	V	Pulses 1-3
		29	30	31	V	Pulses 4-6
		32	33	34	V	Pulses 7-9
	TPW	10		40	µs	See Note 3
	TR1	53	66	88	µs	See Note 4
	TR2	42	52	69	µs	See Note 4
	TF					NA
	Reject		9		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	17.9	18.9	19.9	V	701-1655/TP4
	Low Load	17.9	18.9	19.9	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	4.6	5.6	6.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 11*
2. *Load RAM with hex 01 for Family 12.*
3. *This is measured at the 90% level of the pulse, and all three pulse levels must meet this specification.*
4. *This is measured from 10% to 90% on the tallest pulse.*

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10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		JH	5/83
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 11, 12

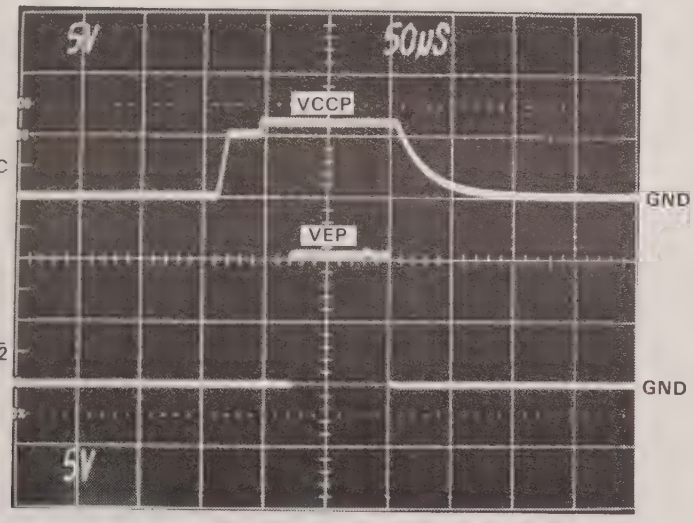
DRAWN BY: ES

CHECKED BY:

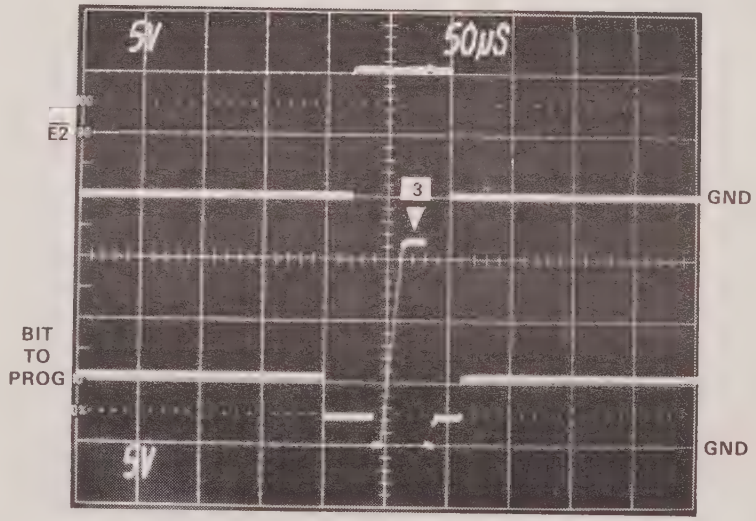
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

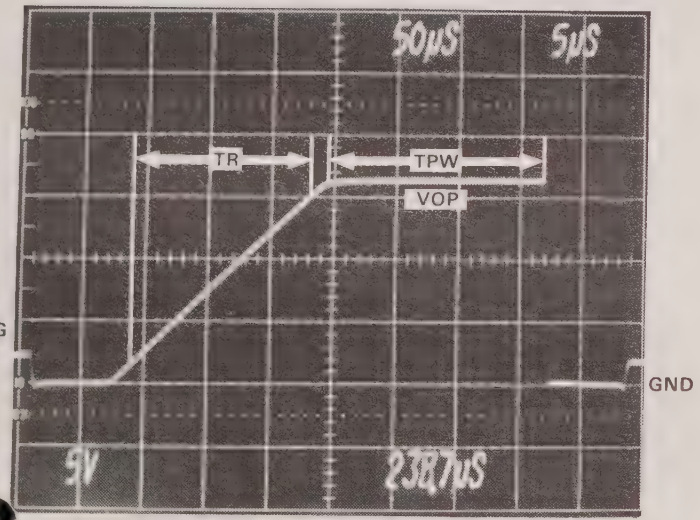
SHEET 1/1


5V
50µS
VCCP
VCC
GND
VEP
E2
GND
5V

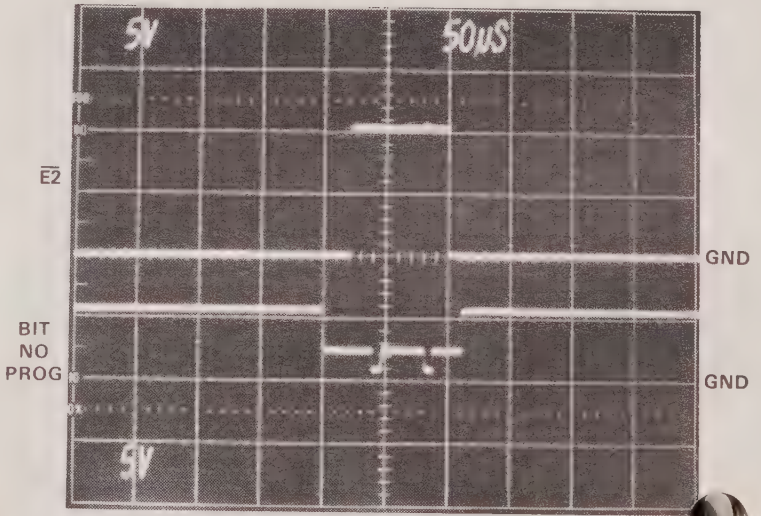
1


5V
50µS
E2
3
GND
BIT
TO
PROG
GND
5V

2


50µS
5µS
TR
TPW
VOP
BIT
TO
PROG
GND
5V
238.7µS

3


5V
50µS
E2
GND
BIT
NO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	
	VOP	15.75	16	16.25	V	
	VEP	9.75	10	11.0	V	
	TPW	15		20	µs	
	TR	10	15	20	µs	
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.9	1.0	1.1	V	701-1655/TP2
	High Load	16.3	17.3	18.3	V	701-1655/TP4
	Low Load	16.3	17.3	18.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	0	0	0.4	V	701-1655/TP4
	Low Load	12.6	13.6	14.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 13.*
2. *Load RAM with hex 01 for Family 14.*
3. *Photo 6 is for registered devices.*
4. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

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10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		XX	5/83
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 13, 14

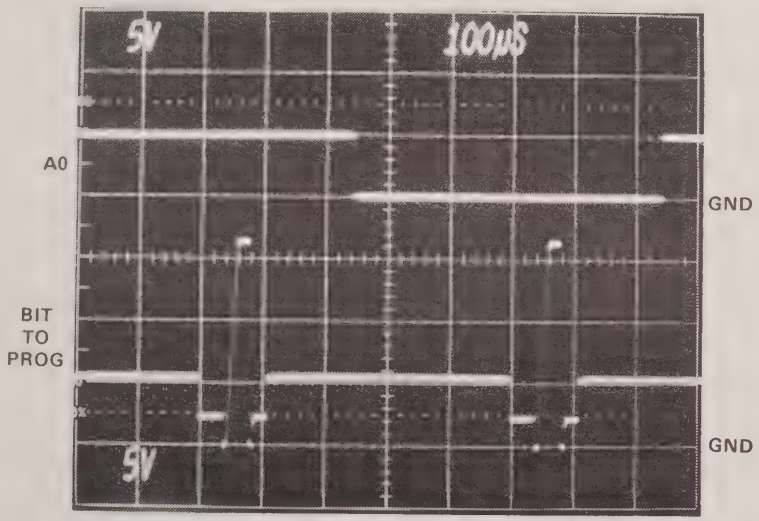
DRAWN BY:

CHECKED BY:

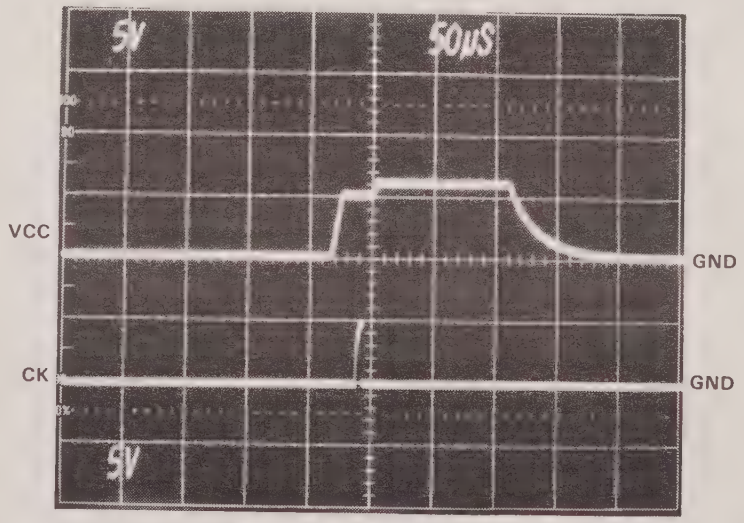
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2



5

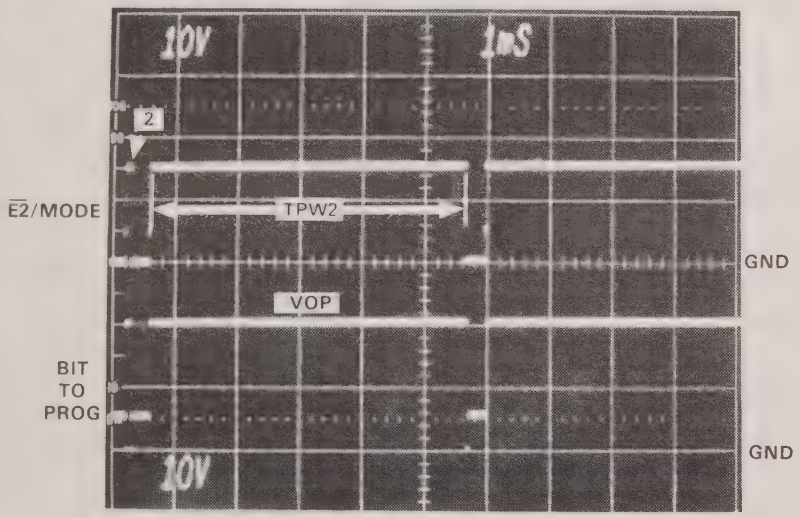


6

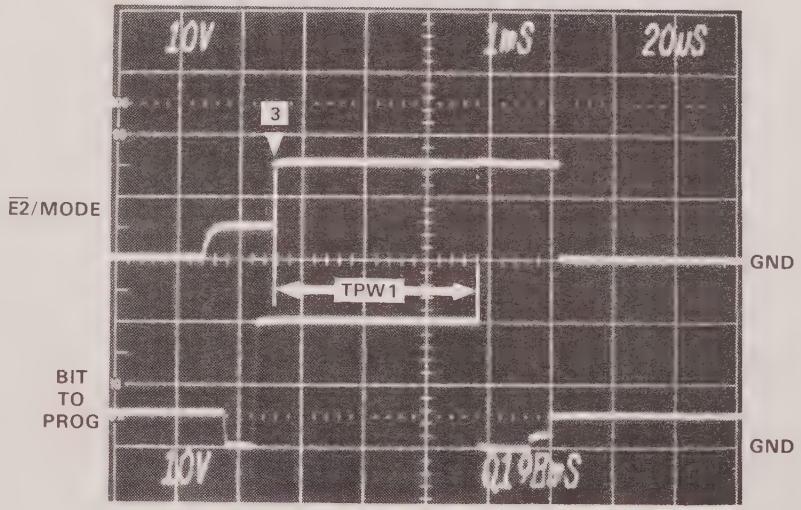
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

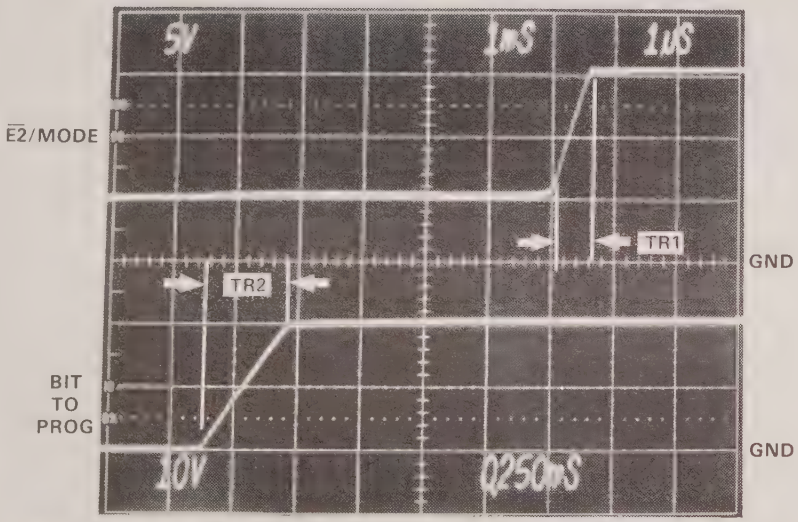
TITLE: TIMING DIAGRAM FAMILY CODES 13, 14			DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2


10V
1mS
2
E2/MODE
TPW2
GND
VOP
BIT
TO
PROG
GND
10V

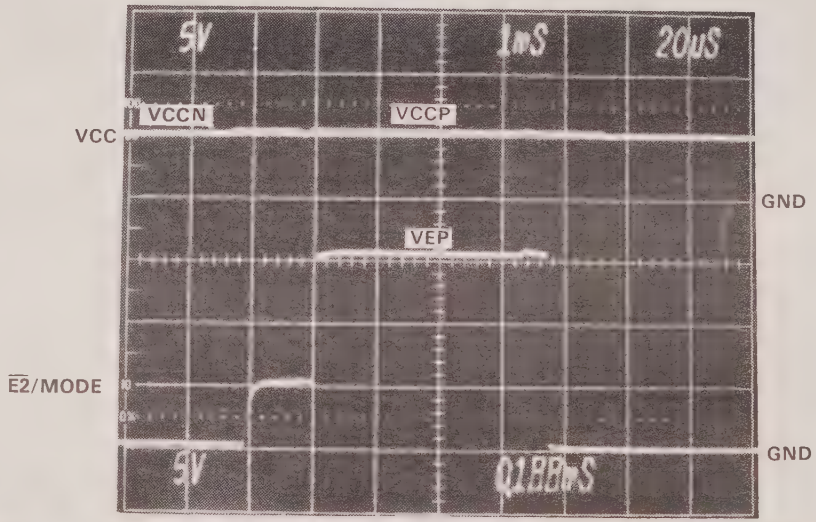
1


10V
1mS
20uS
3
E2/MODE
GND
TPW1
BIT
TO
PROG
GND
10V

2


5V
1mS
1uS
E2/MODE
TR1
GND
TR2
BIT
TO
PROG
GND
10V
Q250mS

3


5V
1mS
20uS
VCCN
VCCP
VCC
GND
VEP
E2/MODE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.0	5.25	5.5	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	19.5	20.0	20.5	V	
	VEP	14.5	15.0	15.5	V	
	TPW1	50		100	µs	Pulse 1
	TPW2	5		15	ms	Pulses 2-80
	TR1	0.2		0.7	µs	See Note 3
	TR2	0.6		1.4	µs	See Note 3
	TF					NA
	Reject		80		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.6	4.7	4.8	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	24.3	25.3	26.3	V	701-1655/TP4
	Low Load	24.3	25.3	26.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.3	2.4	2.5	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	18.0	19.0	20.0	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 15*
2. *Load RAM with hex 01 for Family 16.*
3. *Measured from 10% to 90%.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.B.	11/82
		ECN #4772		XX	1/83
		ECN #4831		XX	5/83
		ECN #5023		CJB	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

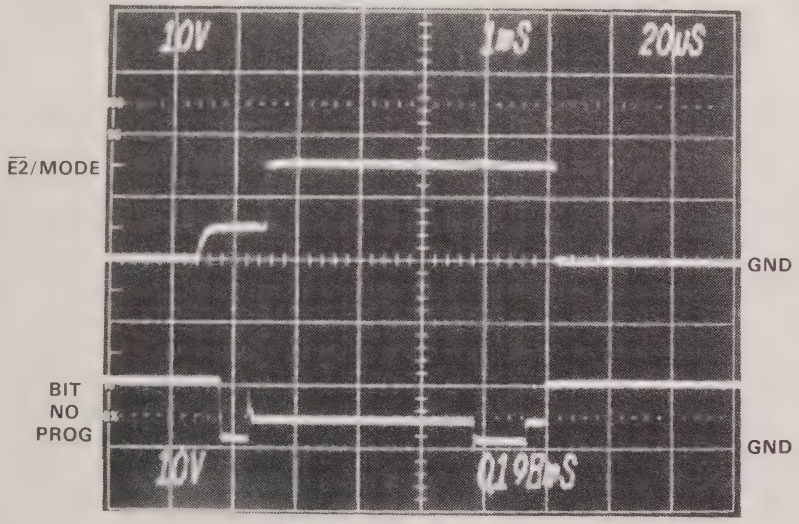
FAMILY CODES 15, 16

DRAWN BY: EE

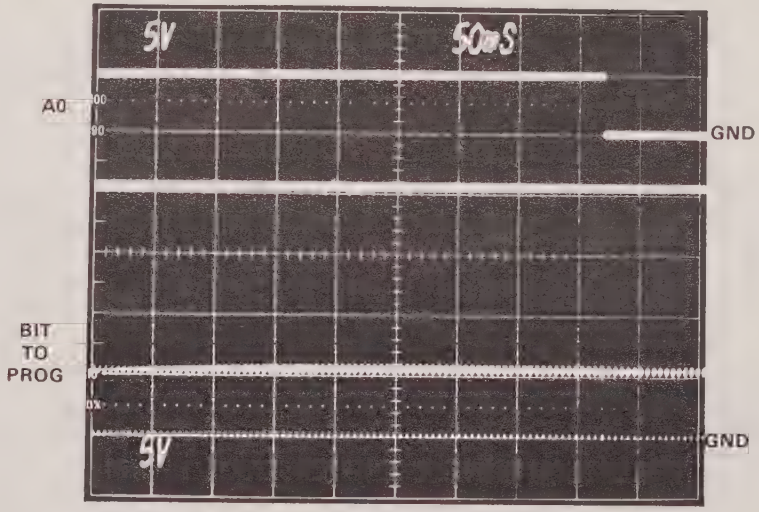
CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE | SHEET 1/2


10V
1mS
20µS
E2/MODE
GND
BIT
NO
PROG
GND
10V
Q19BmS

5

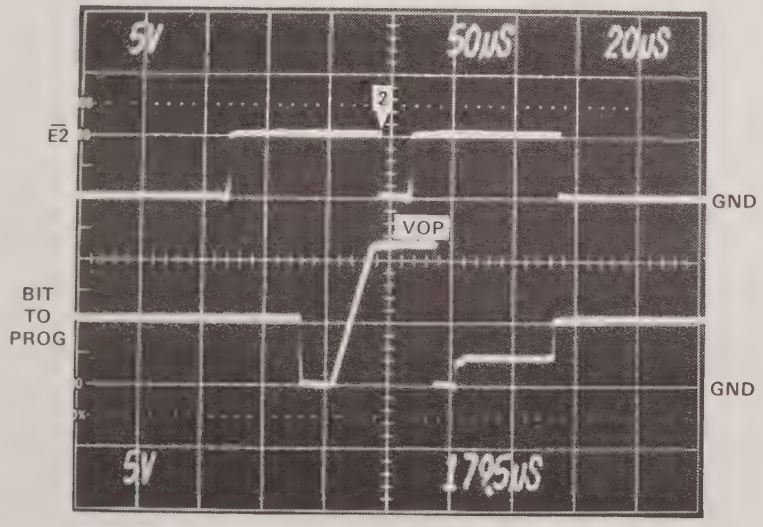

5V
50mS
A0
GND
BIT
TO
PROG
GND
5V

6

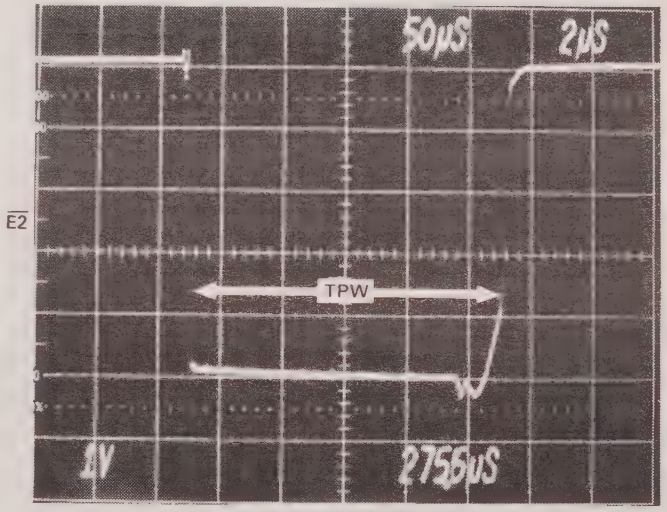
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.B.	11/82
		ECN #4831		JLH	5/83
		ECN #5023		CJB	3/84

DATA I/O ISSAQUAH, WA

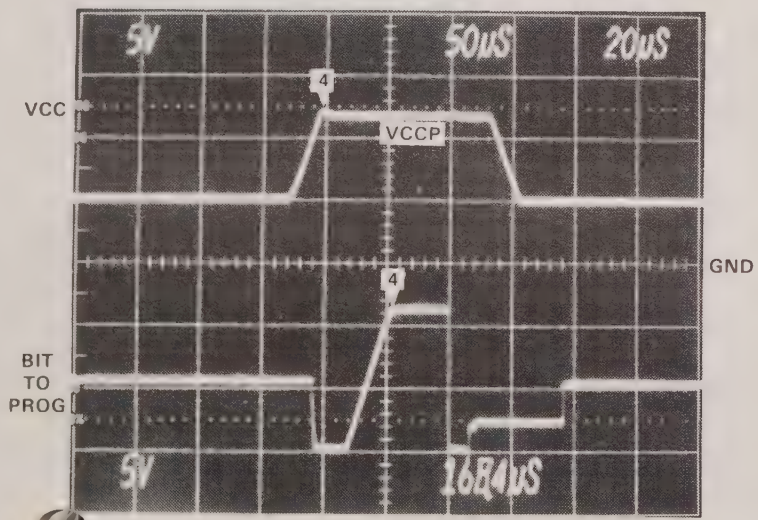
TITLE: TIMING DIAGRAM FAMILY CODES 15, 16		DRAWN BY: EE CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
50µS
20µS
2
E2
GND
VOP
BIT
TO
PROG
GND
5V
1795µS

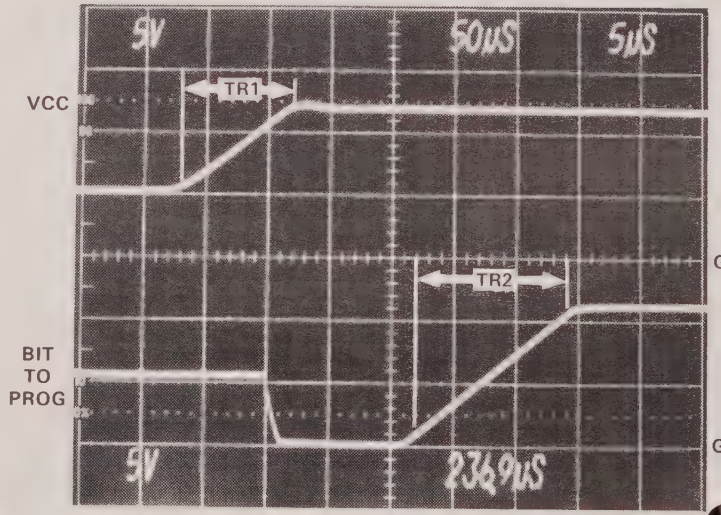
1


50µS
2µS
E2
TPW
GND
1V
2756µS

2


5V
50µS
20µS
4
VCC
VCCP
GND
4
BIT
TO
PROG
5V
1684µS

3


5V
50µS
5µS
VCC
TR1
GND
TR2
BIT
TO
PROG
GND
5V
2369µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.5	11.7	12.0	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	10.5	11.0	11.5	V	
	TPW	9.0	10.0	11.0	µs	
	TR1	1.0		20.0	µs	See note 3
	TR2	1.0		15.0	µs	
	TF					NA
	Reject		10		Pulses	
	Overprogram		5		Pulses	
1ST PASS VERIFY	VCC	4.2	4.3	4.4	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	7.8	8.8	9.8	V	701-1655/TP4
	Low Load	7.8	8.8	9.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 17.*
2. *Load RAM with hex 01 for Family 18.*
3. *Load V_{CC} with a 330 Ω ½-watt resistor.*

REVISIONS

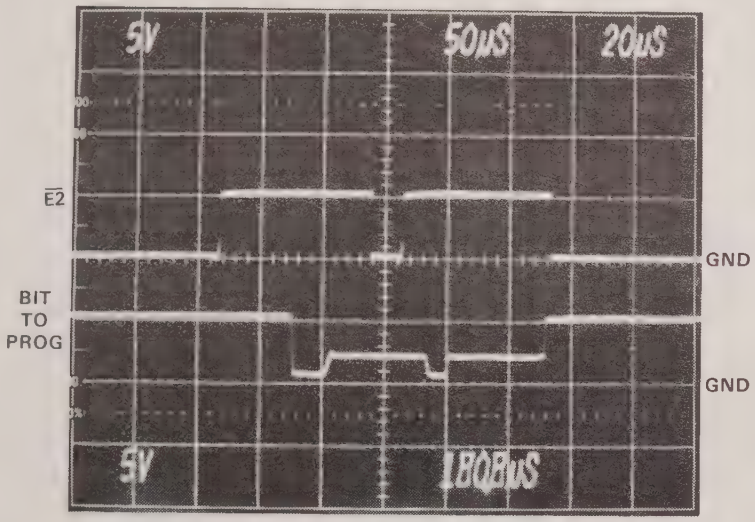
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		ZH	5/83
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

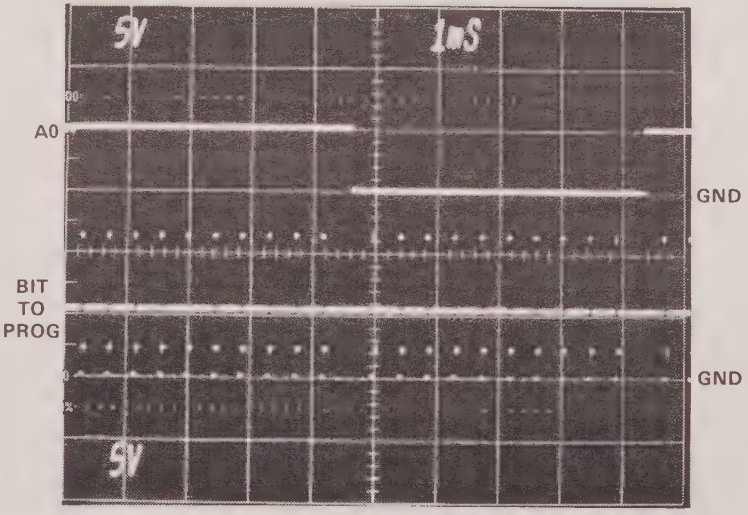
TITLE: TIMING DIAGRAM FAMILY CODES 17, 18	DRAWN BY: EE
	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE | SHEET 1/2


5V
50uS
20uS
E2
GND
BIT
TO
PROG
GND
5V
100uS

5

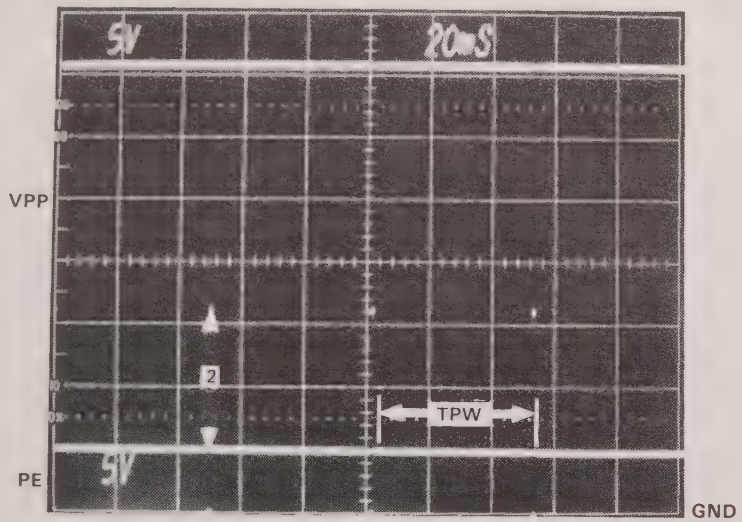

5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

6

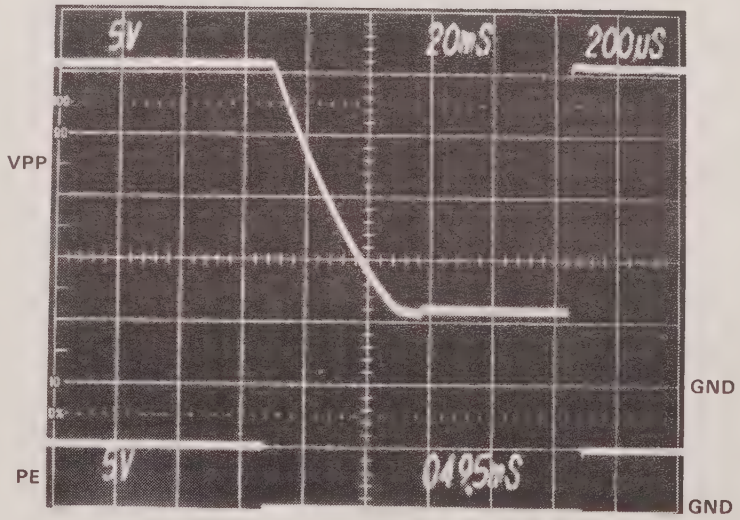
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		E.J.Z.	11/82
		ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

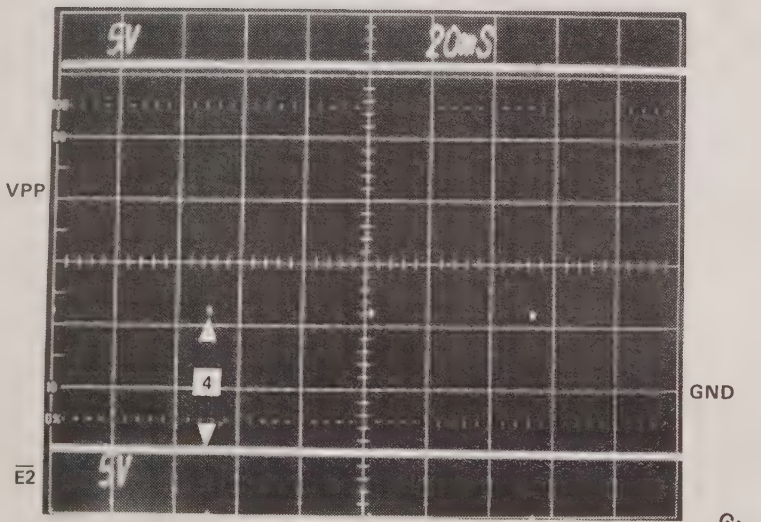
TITLE: TIMING DIAGRAM		DRAWN BY: EE
FAMILY CODES 17, 18		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
20mS
VPP
2
TPW
PE
5V
GND

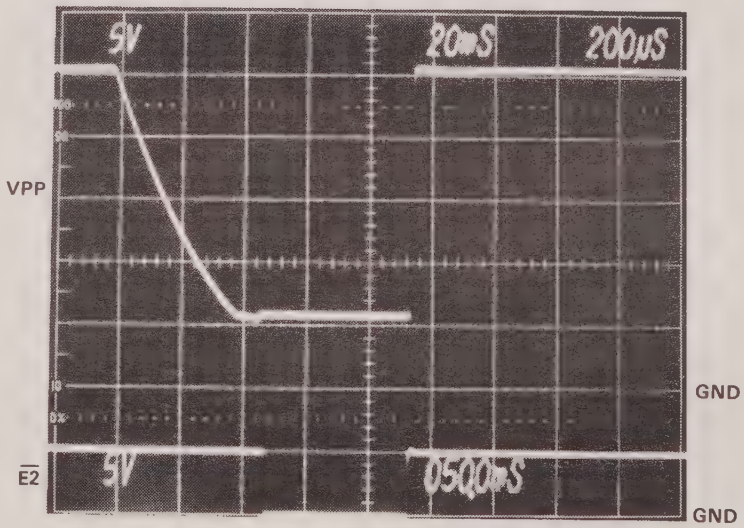
1


5V
20mS
200µS
VPP
GND
PE
5V
049.5mS
GND

2


5V
20mS
VPP
4
GND
E2
5V
GND

3


5V
20mS
200µS
VPP
GND
E2
5V
050.0mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.00	5.25	V	
	VPPV	0.0	0.0	0.8	V	Pinout 24
	TPW	48	50	52	ms	
	T_R	50			ns	
	T_F	50			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 19.*
2. *Load RAM with hex 01 for Family 20, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 11 and 12 are for Pinout 24.*
4. *Photos 13 and 14 are for Pinout 25.*
5. *Photo 15 is for Pinout 49, using the same setup as photo 12.*
6. *Photo 16 is for Pinout 50, using the same setup as photo 14.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		KH	5/83
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 19, 20

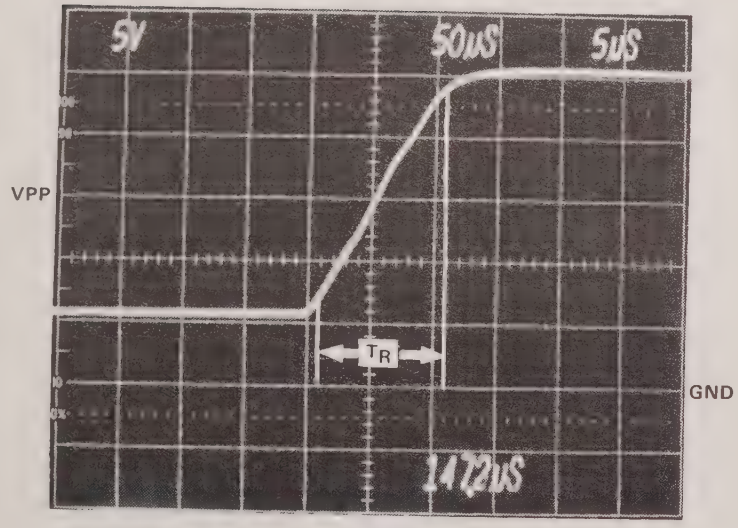
DRAWN BY:

CHECKED BY:

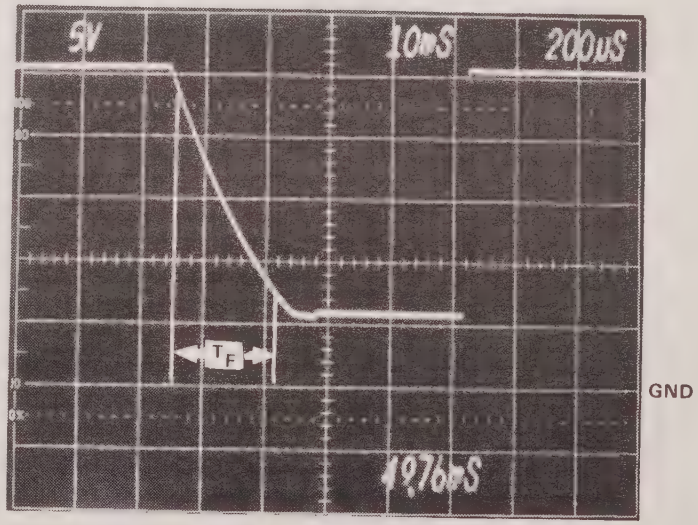
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

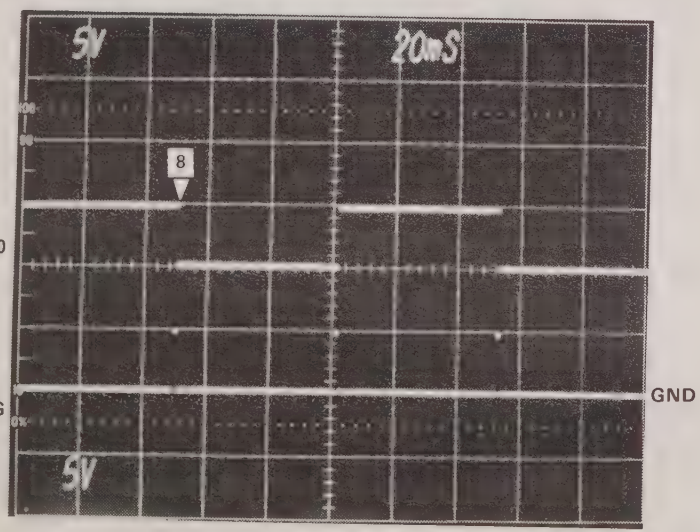
SHEET 1/3


5V
50uS
5uS
VPP
T_R
GND
1.12uS

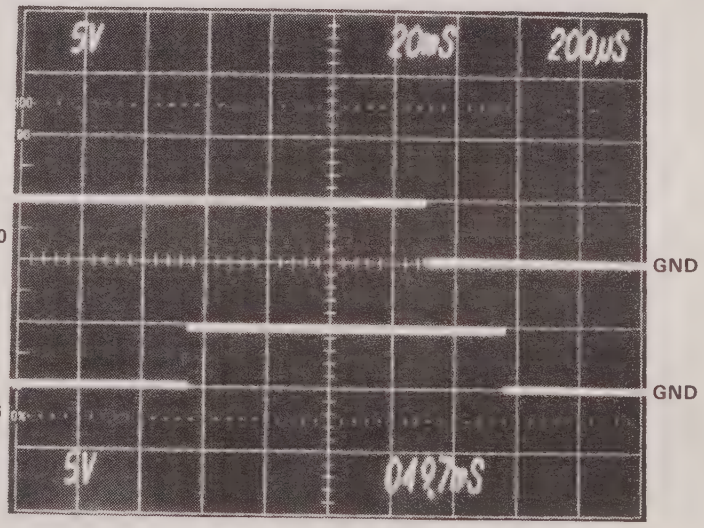
5


5V
10mS
200uS
T_F
GND
19.76mS

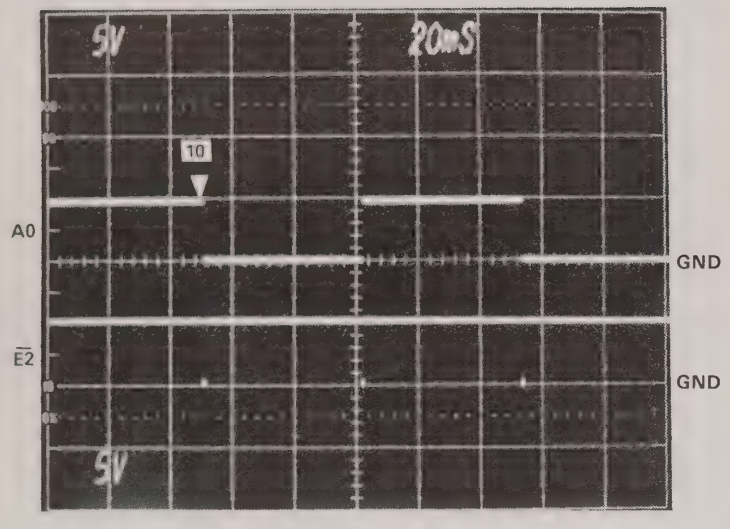
6


5V
20mS
8
A0
BIT
TO
PROG
GND
5V

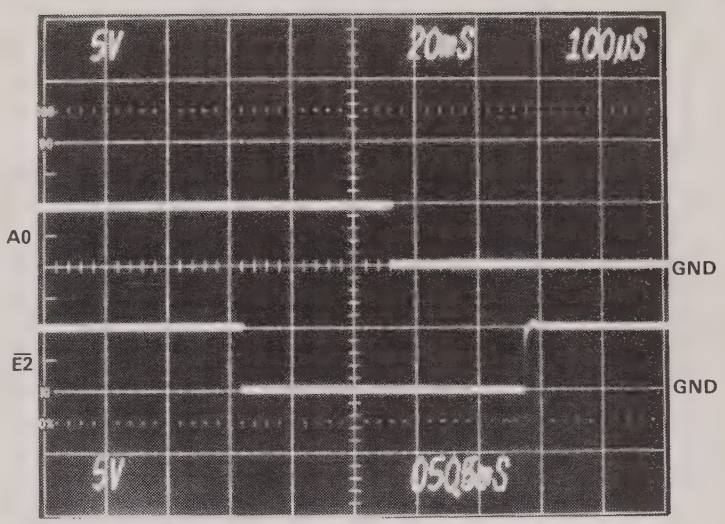
7


5V
20mS
200µS
A0
GND
BIT
TO
PROG
GND
5V
049.7mS

8



9



10

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJJ	11/82
		ECN #4831		JH	5/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 19, 20

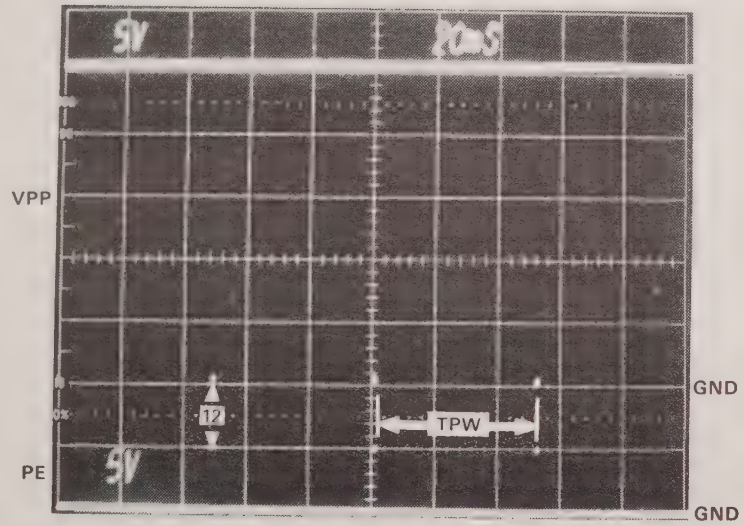
DRAWN BY:

CHECKED BY:

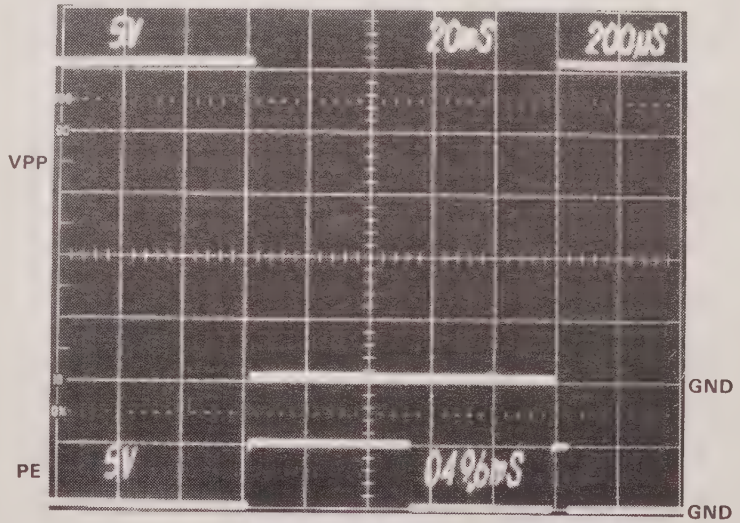
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

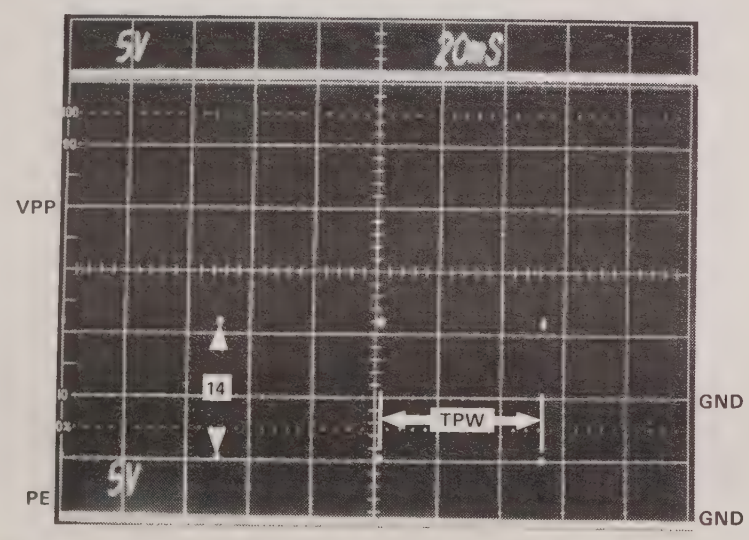
SHEET 2/3


5V
20mS
VPP
12
TPW
GND
PE
5V
GND

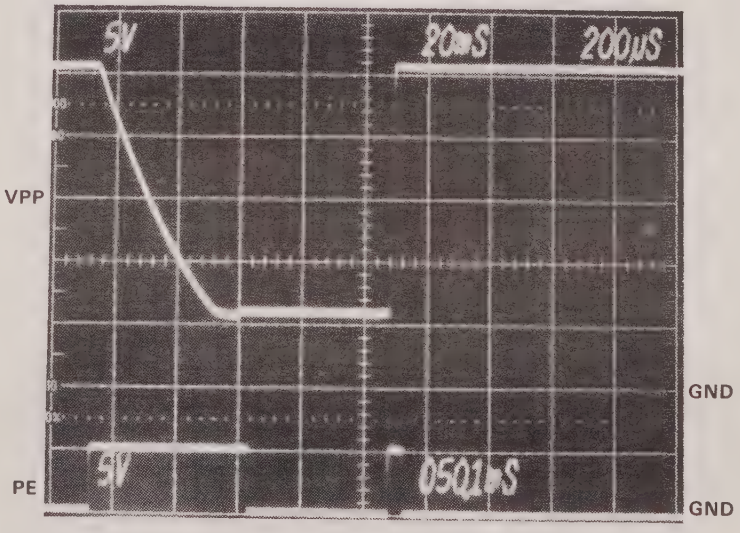
11


5V
20mS
200µS
VPP
GND
PE
5V
GND

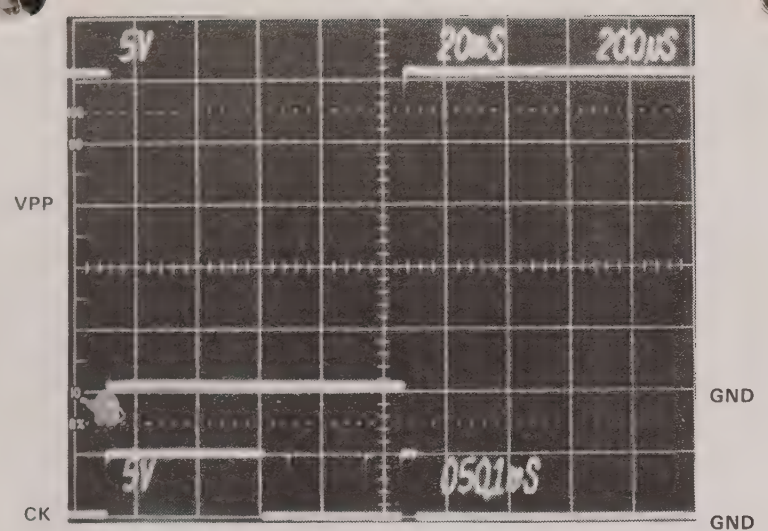
12


5V
20mS
VPP
14
TPW
GND
PE
5V
GND

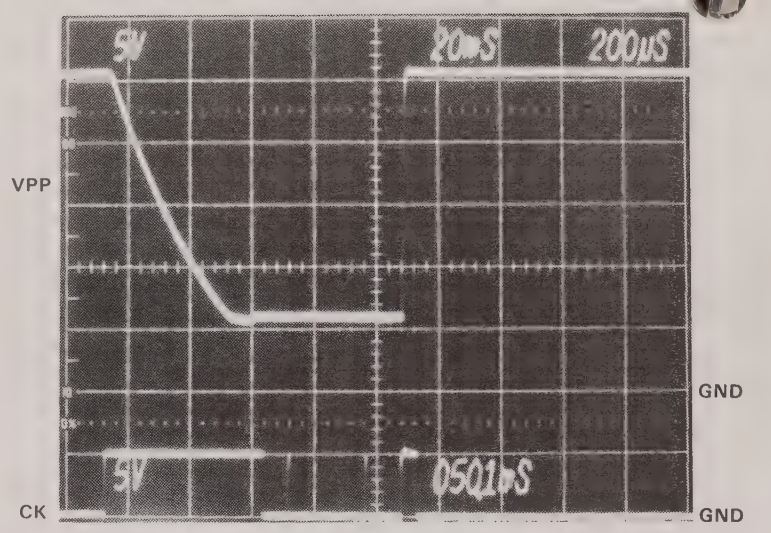
13


5V
20mS
200µS
VPP
GND
PE
5V
GND

14



15



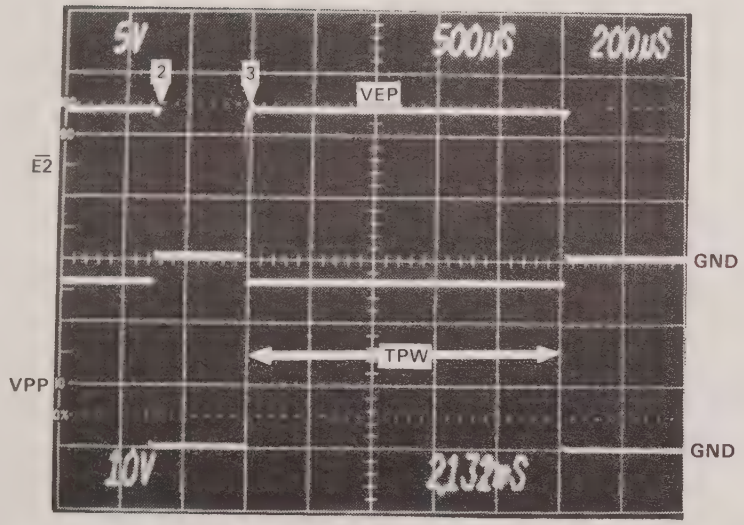
16

B-35
10-950-0059

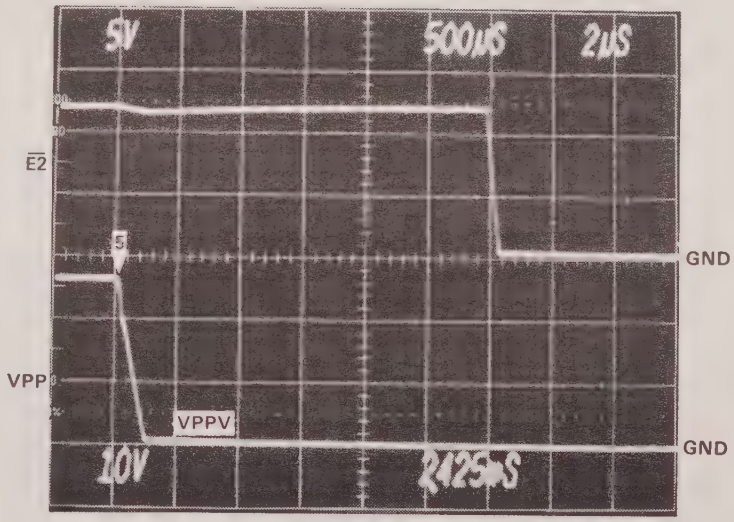
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJ	11/82
		ECN #4831		XA	5/83

DATA I/O ISSAQUAH, WA

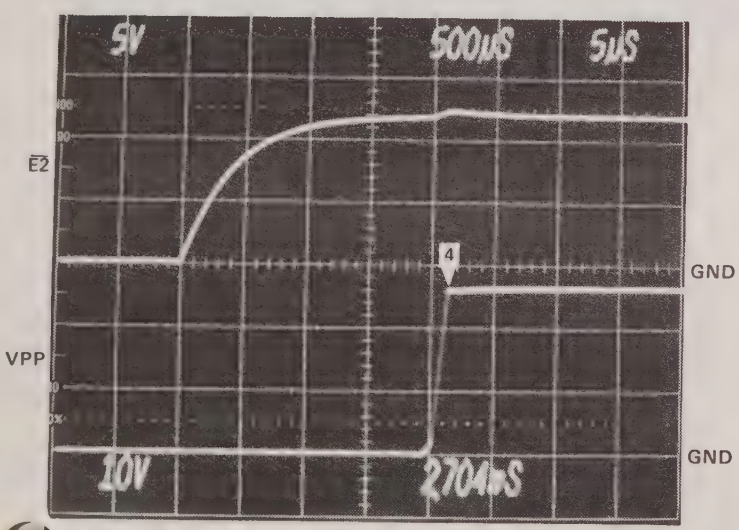
TITLE: TIMING DIAGRAM FAMILY CODES 19, 20		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 3/3


5V
500µS
200µS
2
3
VEP
E2
GND
TPW
VPP
GND
10V
2132µS

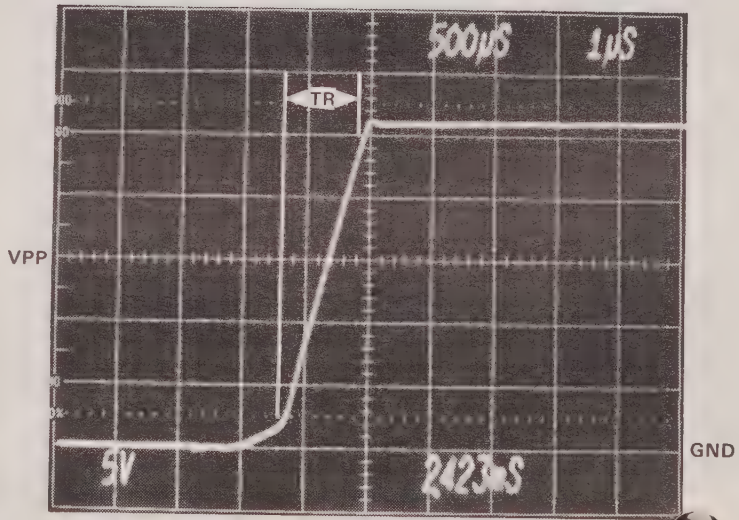
1


5V
500µS
2µS
E2
5
GND
VPP
VPPV
GND
10V
2425µS

2


5V
500µS
5µS
E2
4
GND
VPP
GND
10V
2704µS

3


500µS
1µS
TR
VPP
GND
5V
2423µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	25.0	26.0	27.0	V	
	VPPV	0.0	0.0	1.0	V	
	VEP	11.4	12.0	12.6	V	
	VBB	-5.25	-5.00	-4.75	V	Not Shown
	VDD	11.4	12.0	12.6	V	Not Shown
	TPW	0.8	1.0	1.2	ms	
	TR	0.5	1.0	2.0	µs	
	TF	0.5	1.0	2.0	µs	
	Reject		100		Loops	See Note 3
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	16.3	17.3	18.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 21.*
2. *Load RAM with hex 01 for Family 22, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *A loop is defined as a complete pass from Address 0 to maximum device address, applying one pulse at each address.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		XX	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 21, 22

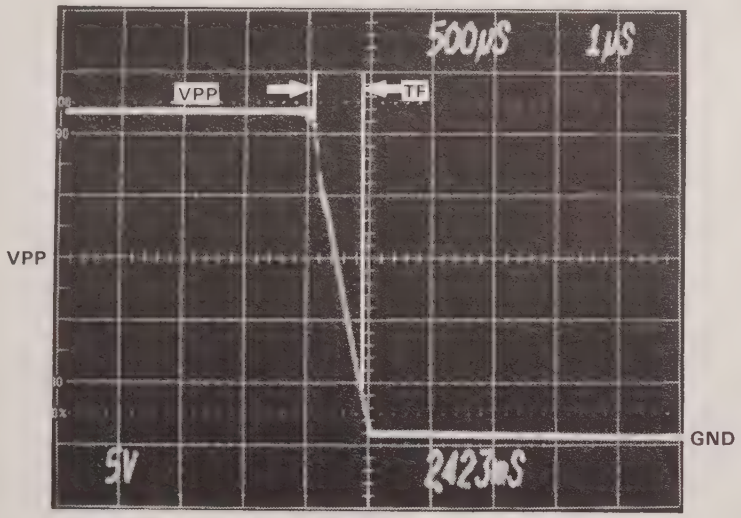
DRAWN BY: EE

CHECKED BY:

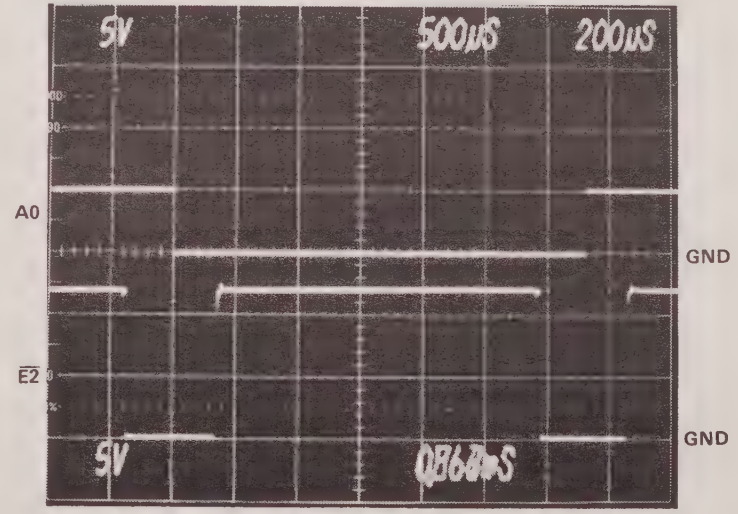
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

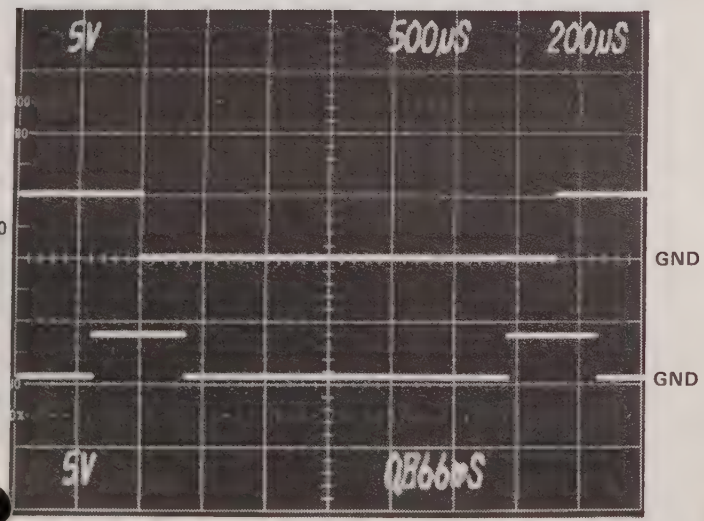
SHEET 1/2


500µS
1µS
VPP
TF
VPP
GND
5V
2423µS

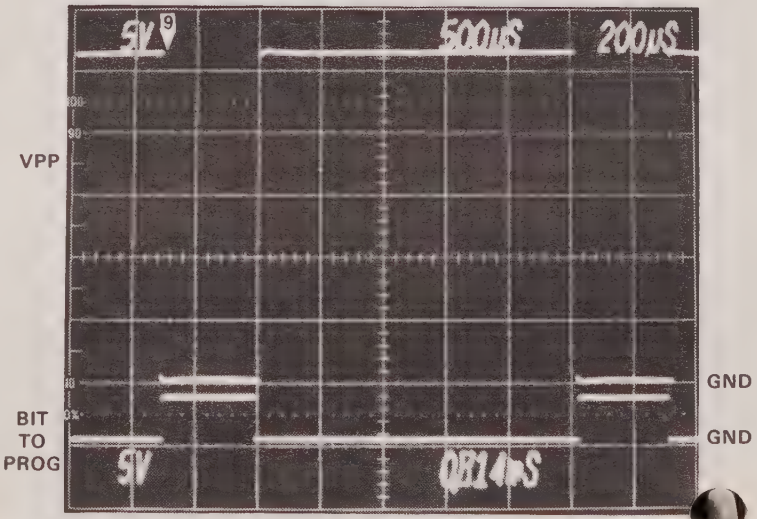
5


5V
500µS
200µS
A0
GND
E2
GND
5V

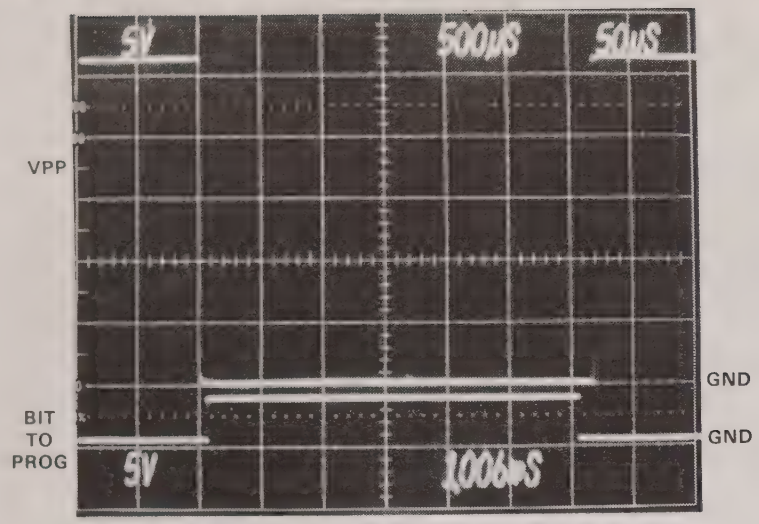
6


5V
500µS
200µS
A0
GND
BIT
TO
PROG
GND
5V
0866µS

7


5V
9
500µS
200µS
VPP
GND
BIT
TO
PROG
GND
5V

8

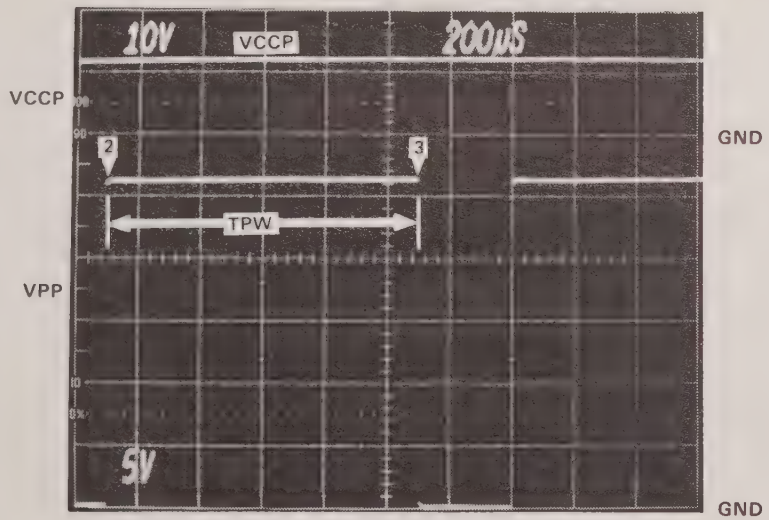


9

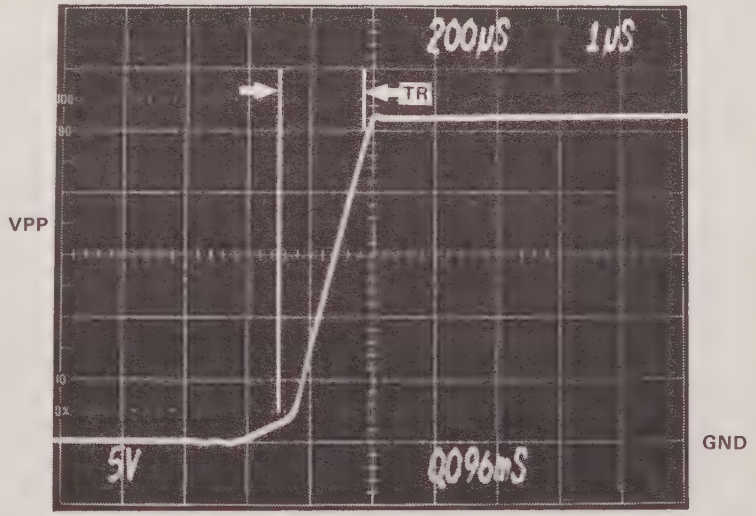
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.F.Z.	11/82
		ECN #4831		XX	5/83

DATA I/O ISSAQUAH, WA

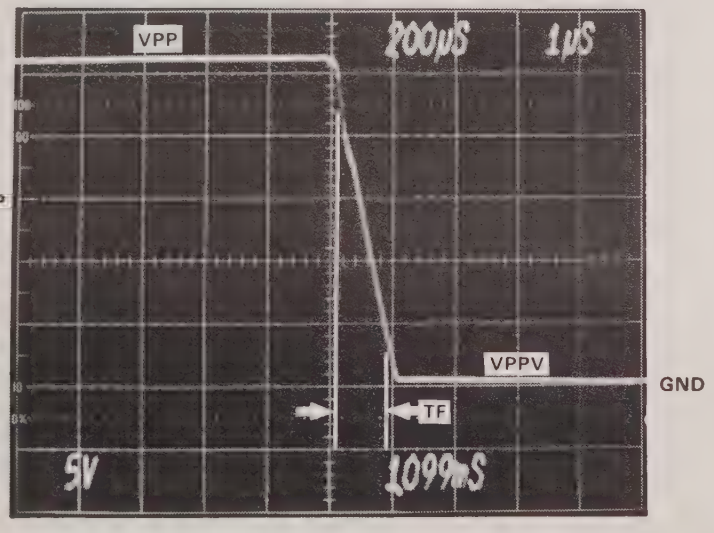
TITLE: TIMING DIAGRAM FAMILY CODES 21, 22			DRAWN BY: ES CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2


10V
VCCP
200µS
VCCP
GND
2
3
TPW
VPP
5V
GND

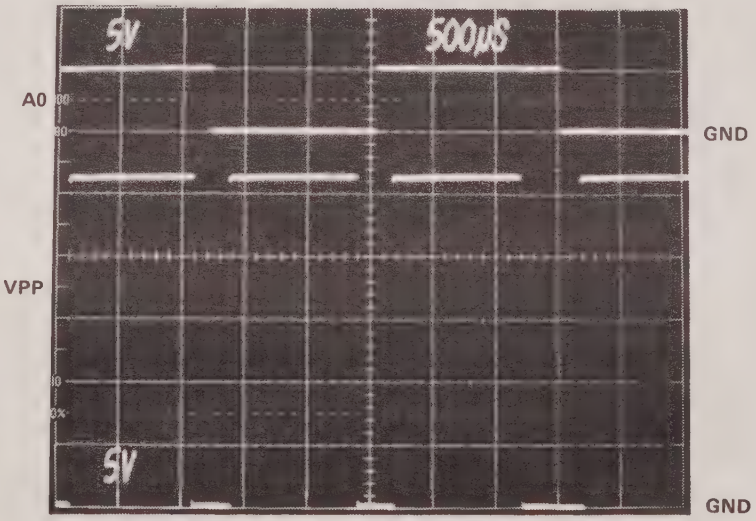
1


200µS
1µS
TR
VPP
GND
5V
0096mS

2


VPP
200µS
1µS
VPP
VPPV
GND
TF
5V
1099mS

3


5V
500µS
A0
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.4	12.0	12.6	V	
	VOP					NA
	VPP	25.0	26.0	27.0	V	
	VPPV	0.0		1.0	V	
	VBB	-5.25	-5.0	-4.75	V	Not Shown
	VDD	11.4	12.0	12.4	V	Not Shown
	TPW	0.8	1.0	1.2	ms	
	TR	0.5		2.0	µs	
	TF	0.5		2.0	µs	
	Reject		100		Loops	See Note 3
	Overprogram		0		Pulses	
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	16.3	17.3	18.3	V	701-1655/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 23.*
2. *Load RAM with hex 01 for Family 24, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *A loop is defined as a complete pass from Address 0 to maximum device address applying one pulse at each address. All 100 loops are performed, and the device is read and verified after all 100 loops.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.T.J.	11/82
		ECN #4831		XA	5/83
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 23, 24

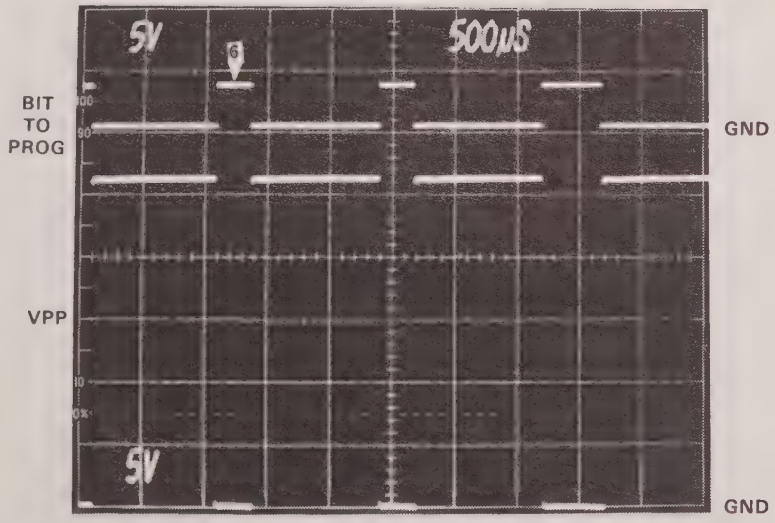
DRAWN BY:

CHECKED BY:

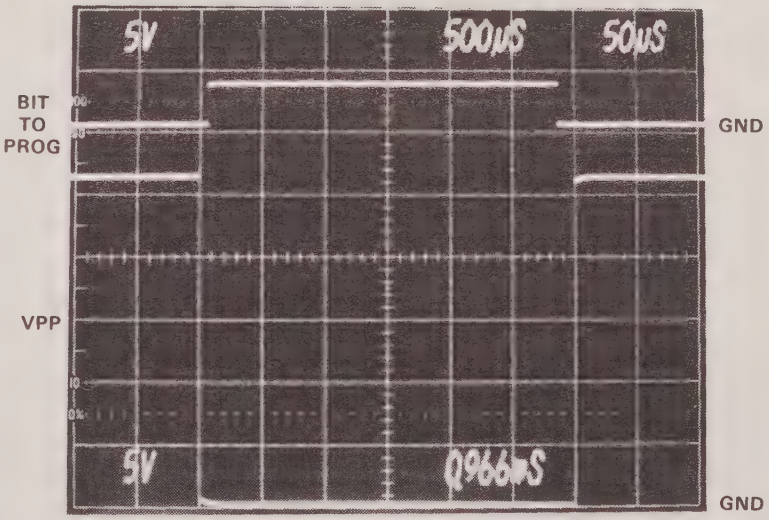
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


5V
6
500µS
BIT
TO
PROG
GND
VPP
5V
GND

5


5V
500µS
50µS
BIT
TO
PROG
GND
VPP
5V
GND

6

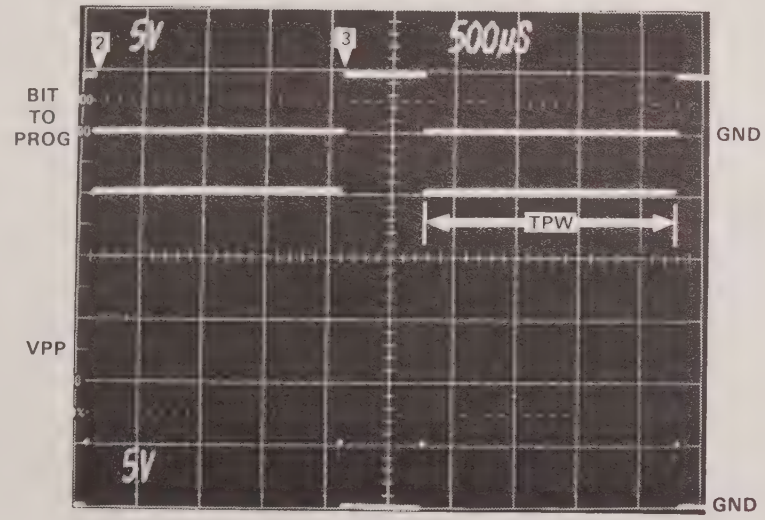
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.3	11/82
		ECN #4831		JCH	5/83

DATA I/O ISSAQUAH, WA

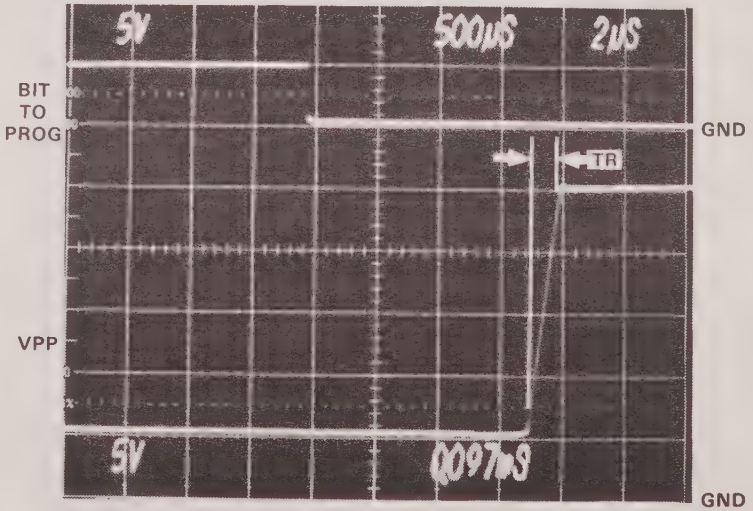
TITLE: TIMING DIAGRAM FAMILY CODES 23, 24	DRAWN BY: [illegible] CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

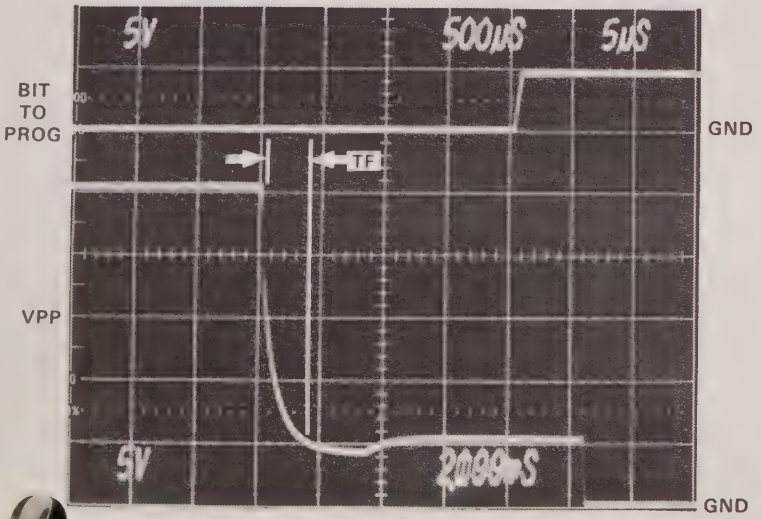
SCALE | SHEET 2/2


2
5V
3
500µS
BIT
TO
PROG
GND
TPW
VPP
5V
GND

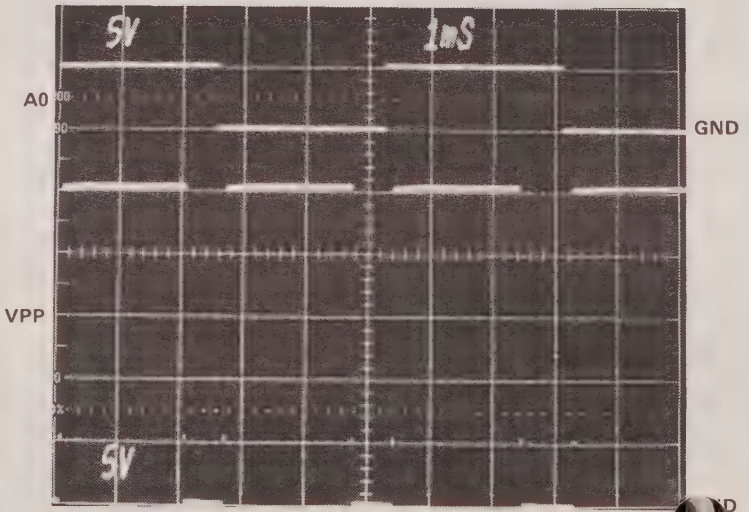
1


5V
500µS
2µS
BIT
TO
PROG
GND
TR
VPP
5V
GND

2


5V
500µS
5µS
BIT
TO
PROG
GND
TF
VPP
5V
GND

3


5V
1mS
A0
GND
VPP
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	1.9	2.0	2.1	ms	
	TR	0.5		2.0	µs	
	TF	0.5		5.0	µs	
	Reject		20		Loops	See Note 3
	Overprogram		5		Loops	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

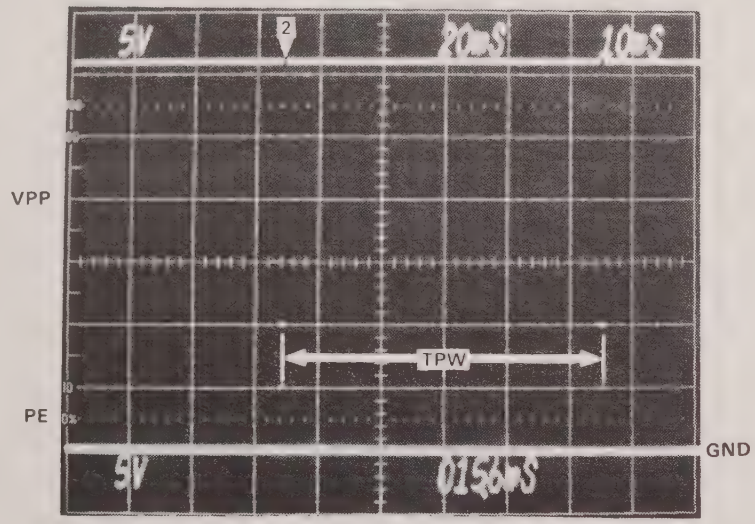
1. *Load RAM with hex FE for Family 25.*
2. *Load RAM with hex 01 for Family 26, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *A loop is defined as one complete pass from Address 0 to maximum device address applying one pulse at each address. A read and verify is done after each loop, and when the device verifies, five more loops are applied.*

REVISIONS

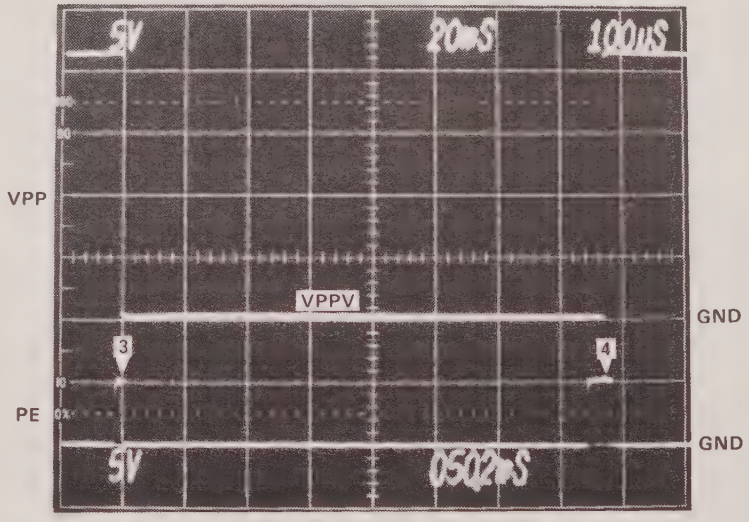
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJJ.	11/82
		ECN #4831		KH	5/83
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

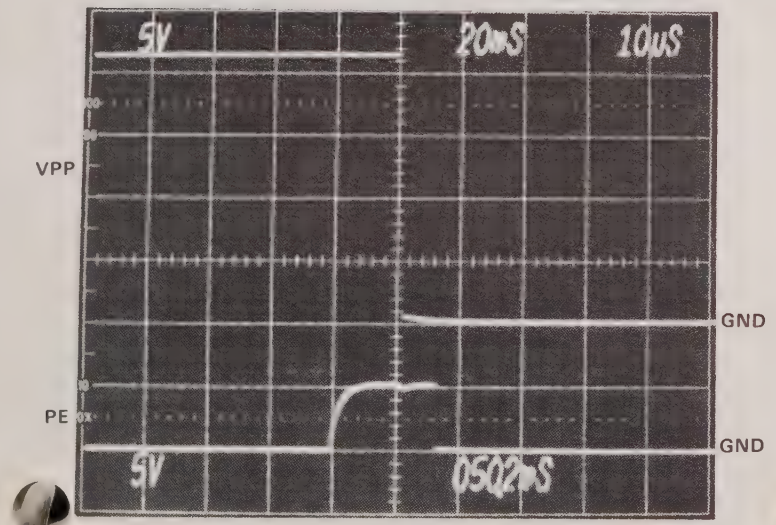
TITLE: TIMING DIAGRAM FAMILY CODES 25, 26	DRAWN BY: CE	
	CHECKED BY:	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/1


5V
2
20mS
10uS
VPP
TPW
PE
GND
5V
0156mS

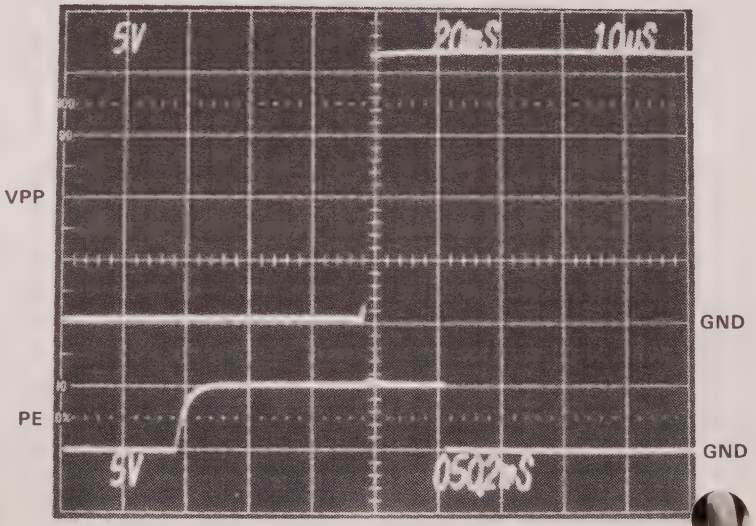
1


5V
20mS
100uS
VPP
VPPV
GND
3
4
PE
GND
5V
0502mS

2


5V
20mS
10uS
VPP
GND
PE
GND
5V
0502mS

3


5V
20mS
10uS
VPP
GND
PE
GND
5V
0502mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.00	6.00	V	
	VPP	20 5	21.0	21.5	V	
	VPPV	0.0	0.0	0.8	V	
	TPW	48	50	52	ms	
	TR	50			ns	
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

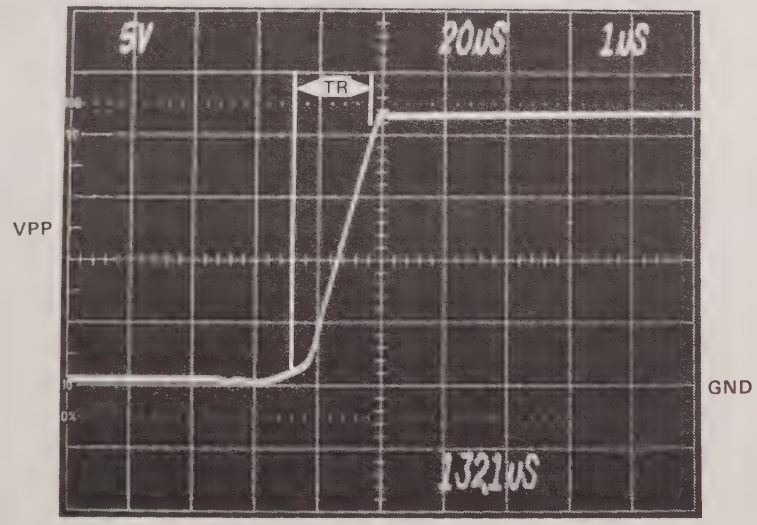
1. *Load RAM with hex FE for Family 27.*
2. *Load RAM with hex 01 for Family 28, and bit-to-prog waveform becomes bit-no-prog waveform.*

REVISIONS

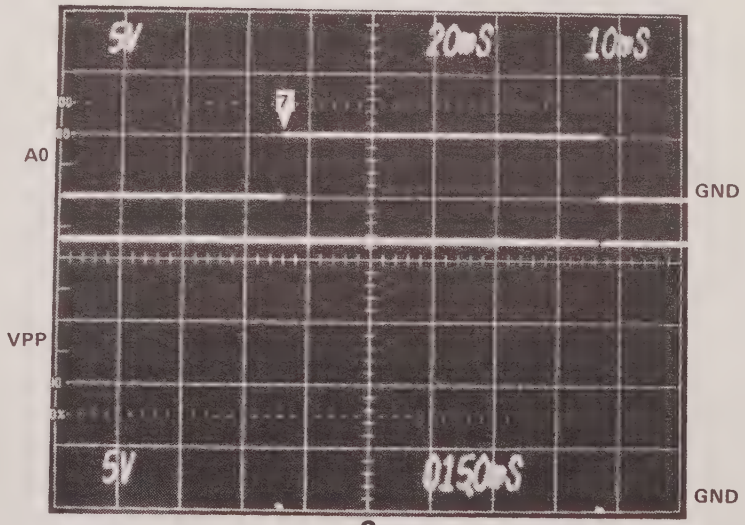
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C 73	11/82
		ECN #4831		XH	5/83
		ECN #5023		C73	3/84

DATA I/O ISSAQUAH, WA

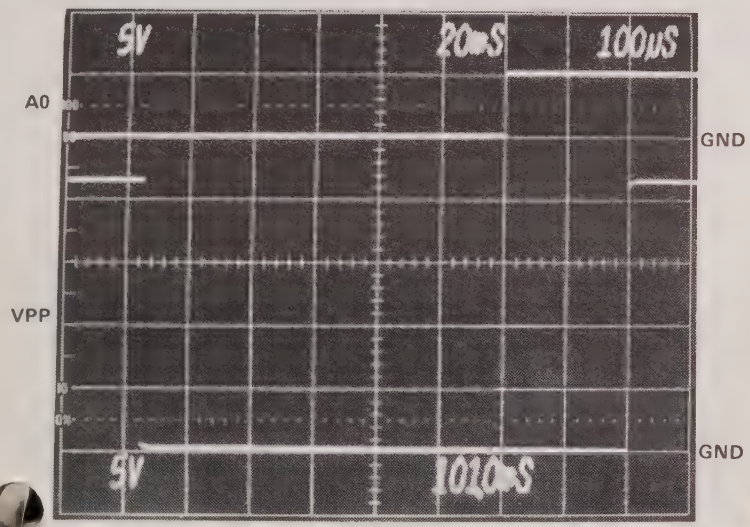
TITLE: TIMING DIAGRAM FAMILY CODES 27, 28	DRAWN BY: ES CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	
SCALE	SHEET 1/2


5V
20uS
1uS
TR
VPP
GND
1321uS

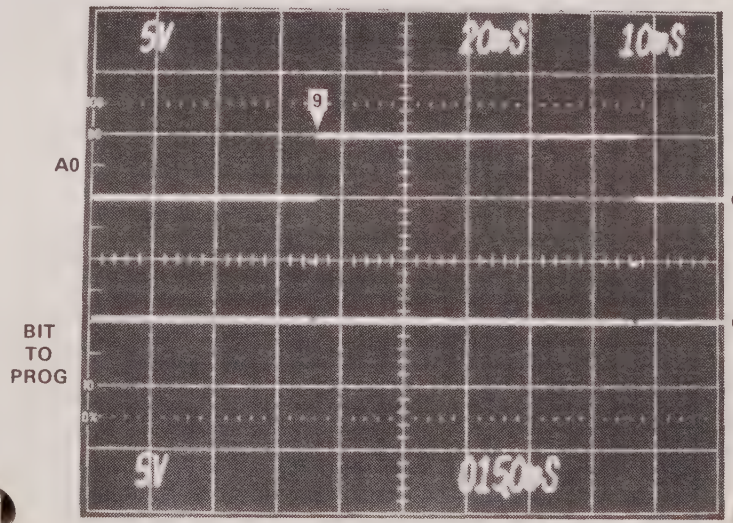
5


5V
20mS
10mS
7
A0
GND
VPP
5V
0150mS
GND

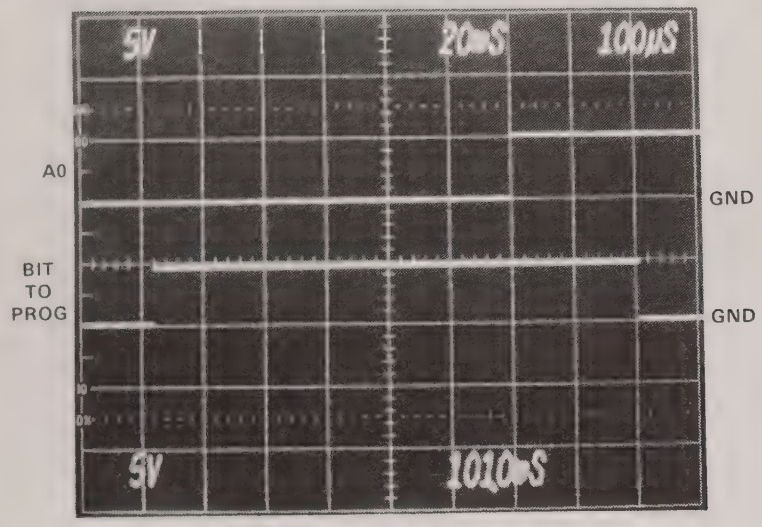
6


5V
20mS
100uS
A0
GND
VPP
GND
5V
1010mS

7


5V
20mS
10mS
9
A0
GND
GND
BIT
TO
PROG
5V
0150mS

8

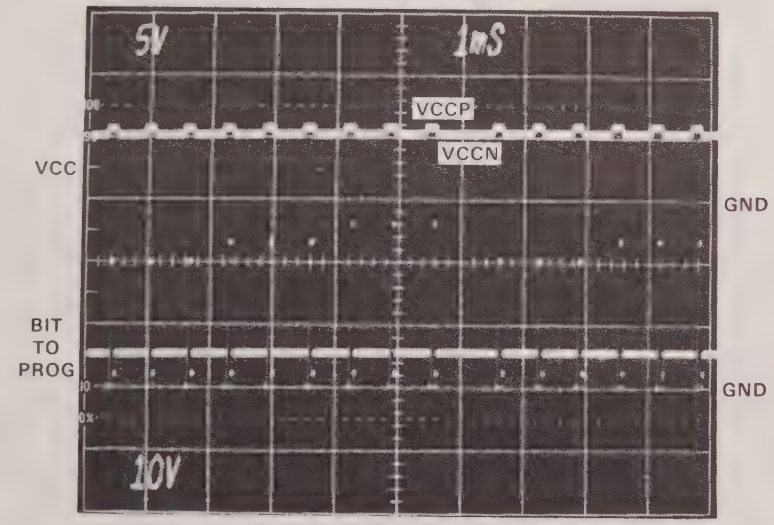


9

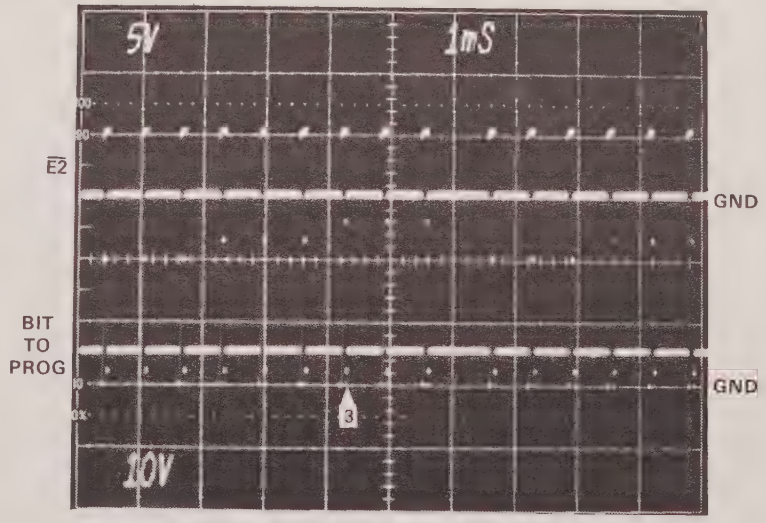
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		[illegible]	[illegible]

DATA I/O ISSAQUAH, WA

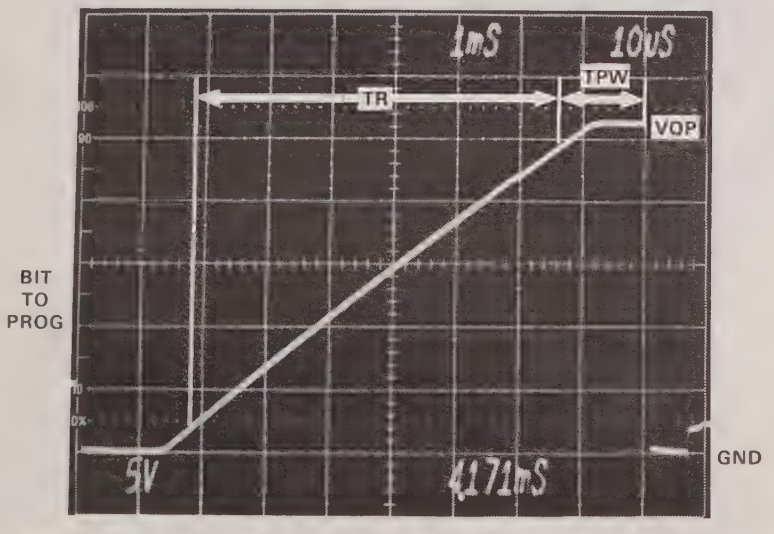
TITLE TIMING DIAGRAM FAMILY CODES 27, 28		DRAWN BY: ES
		CHECKED BY:
SIZE B	CODE IDENT. NO. 54193	DRAWING NO. 33-950-0059
SCALE		SHEET 2/2


5V
1mS
VCCP
VCCN
VCC
GND
BIT
TO
PROG
GND
10V

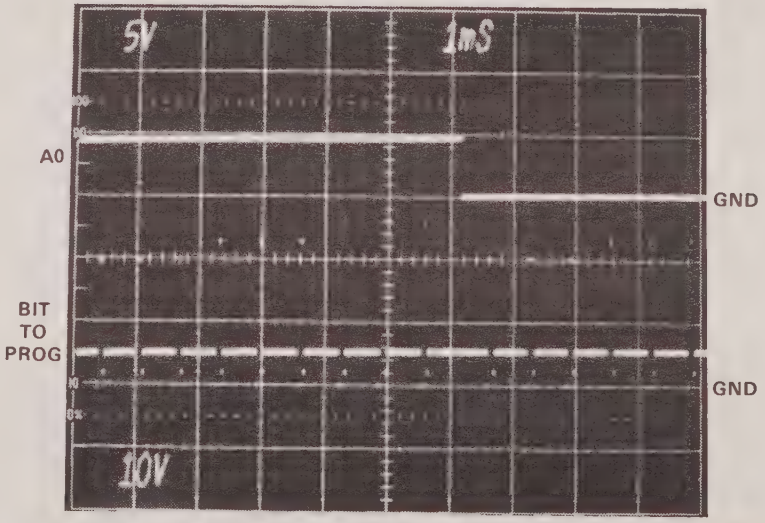
1


5V
1mS
E2
GND
BIT
TO
PROG
GND
3
10V

2


1mS
10uS
TPW
TR
VOP
BIT
TO
PROG
GND
5V
4.171mS

3


5V
1mS
A0
GND
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.4	5.5	5.6	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	19	20	21	V	Pulses 1-3
		22	23	24	V	Pulses 4-6
		25	26	27	V	Pulses 7-9
	TPW	10		40	µs	See note 3
	TR	42	52	69	µs	See note 4
	Reject		9		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	17.9	18.9	19.9	V	701-1655/TP4
	Low Load	17.9	18.9	19.9	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	4.6	5.6	6.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 29.*
2. *Load RAM with hex 01 for Family 30.*
3. *This is measured at the 90% level of the pulse, and all three pulses must meet this specification.*
4. *This is measured from 10% to 90% on the 26V pulses.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C73	11/82
		ECN #4831		JK	1/84
		ECN #5023		C73	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 29, 30

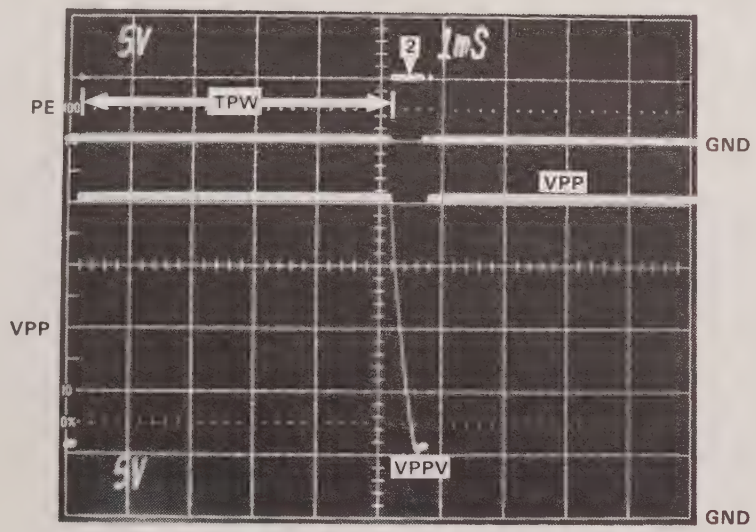
DRAWN BY: EG

CHECKED BY:

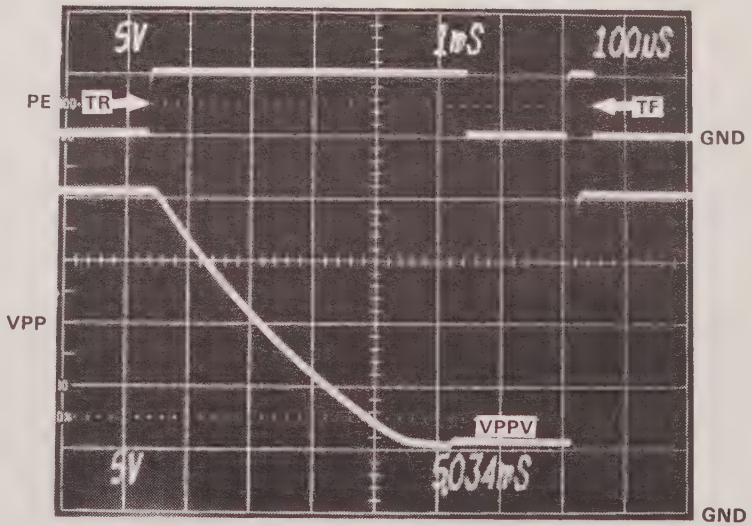
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

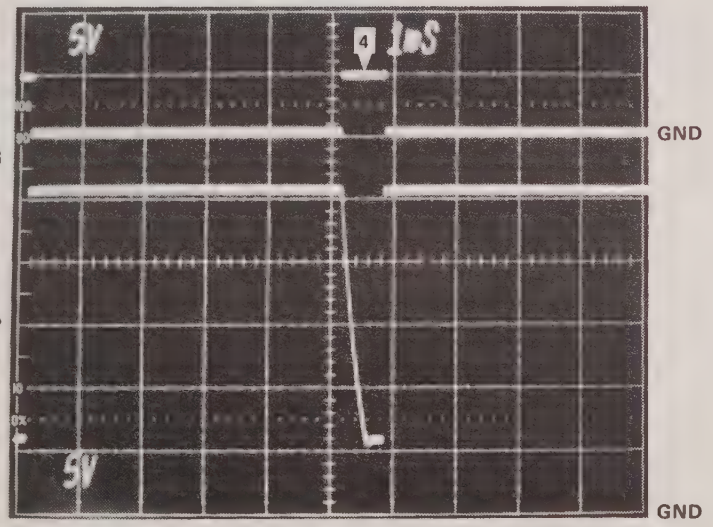
SHEET 1/1


5V
2
1mS
PE
TPW
GND
VPP
VPP
VPPV
5V
GND

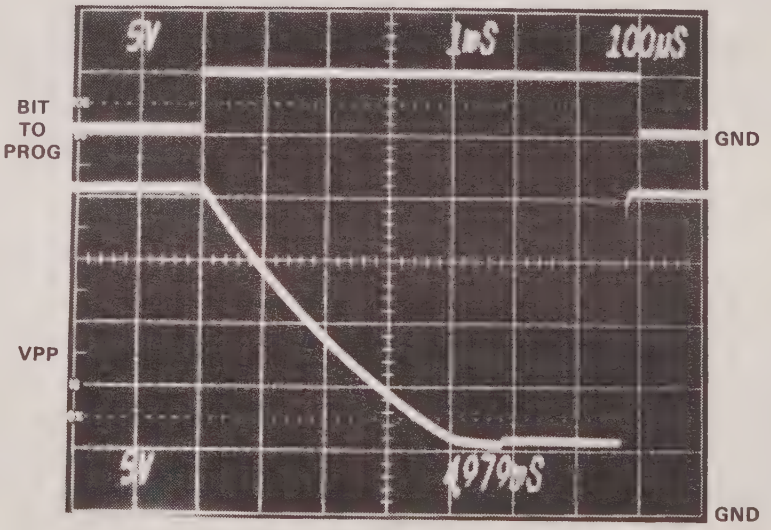
1


5V
1mS
100uS
PE
TR
TF
GND
VPP
VPPV
5V
5034mS
GND

2


5V
4
1mS
BIT
TO
PROG
GND
VPP
5V
GND

3


5V
1mS
100uS
BIT
TO
PROG
GND
VPP
5V
1979mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	4.9	5.0	5.1	ms	
	TR	5			ns	
	TF	5			ns	
	Reject		5		Pulses	
	Overprogram		x		Pulses	See Note 3
1ST PASS	VCC	4.7	4.8	4.9	V	
VERIFY	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS	VCC	5.1	5.2	5.3	V	
VERIFY	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

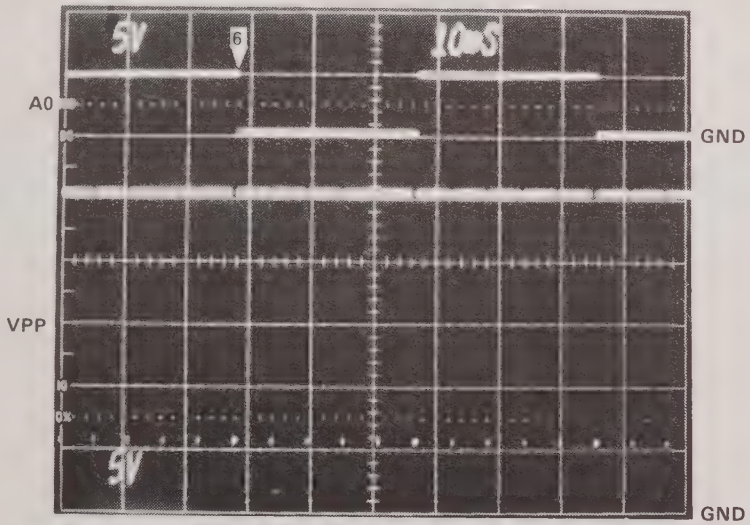
NOTES

1. *Load RAM with hex FE for Family 31.*
2. *Load RAM with hex 01 for Family 32, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The number of overprogram pulses is equal to the greatest number of reject pulses applied to any address.*

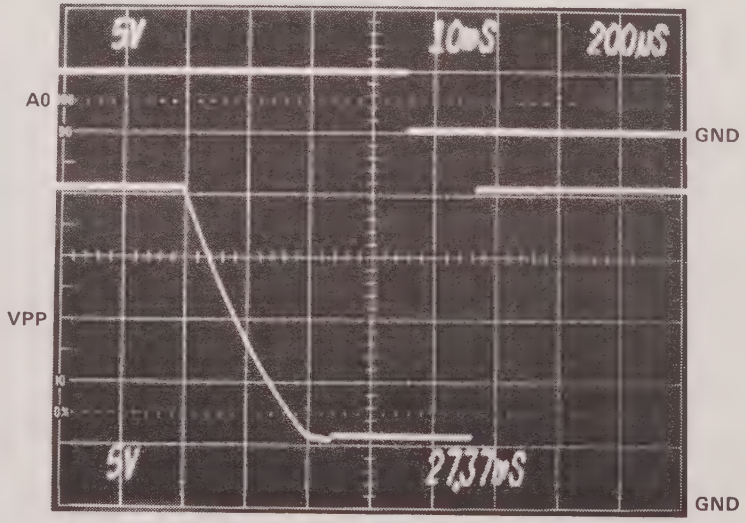
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		[illegible]	1/84
		ECN #4831		[illegible]	[illegible]
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM		DRAWN BY:
FAMILY CODES 31, 32		CHECKED BY:
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059
SCALE		SHEET 1/2


5V
6
10mS
A0
GND
VPP
5V
GND

5


5V
10mS
200uS
A0
GND
VPP
5V
27.37uS
GND

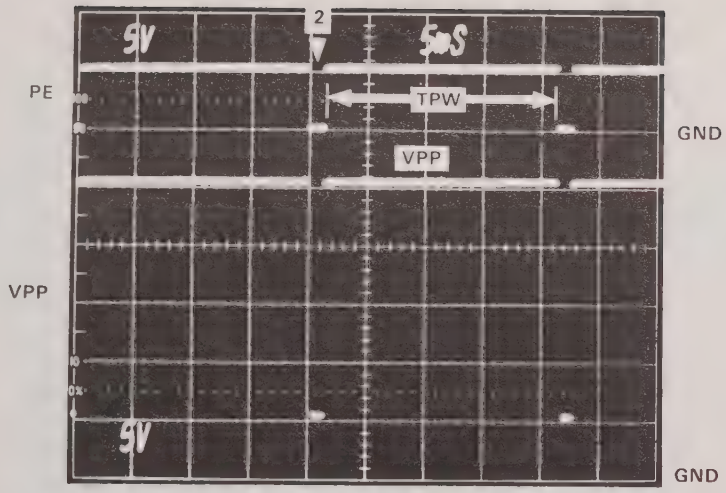
6

REVISIONS

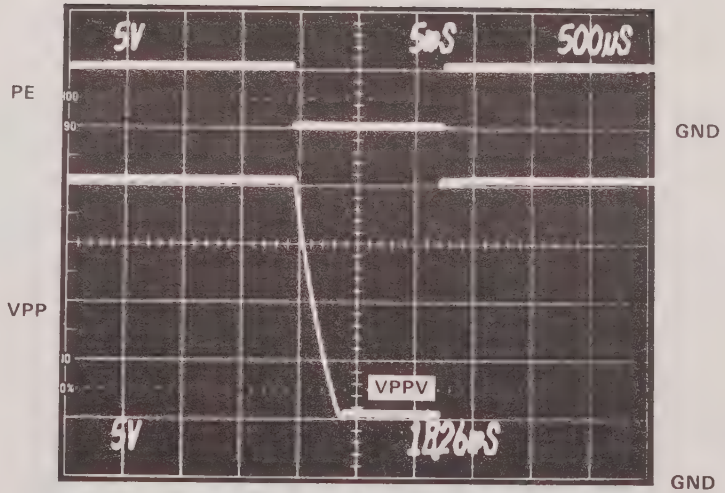
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		J.H.	[illegible]

DATA I/O ISSAQUAH, WA

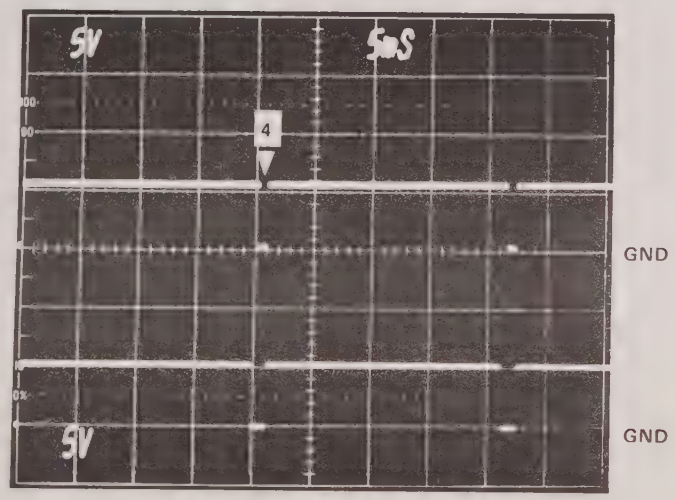
TITLE TIMING DIAGRAM FAMILY CODES 31, 32		DRAWN BY: [illegible] CHECKED BY:
SIZE B	CODE IDENT. NO. 54193	DRAWING NO. 33-950-0059
SCALE		SHEET 2/2


5V
2
5mS
PE
TPW
GND
VPP
VPP
5V
GND

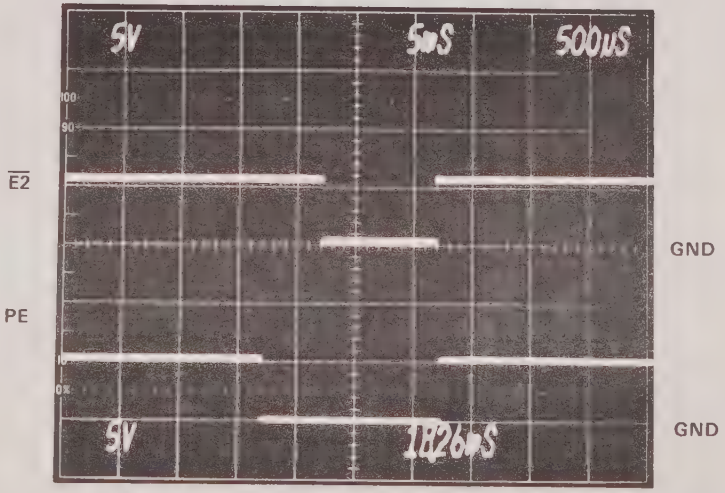
1


5V
5mS
500uS
PE
GND
VPP
VPPV
5V
1.826mS
GND

2


5V
5mS
4
E2
GND
PE
5V
GND

3


5V
5mS
500uS
E2
GND
PE
5V
1.826mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4 75	5.0	5.25	V	
	TPW	19.8	20.0	20.2	ms	
	TR					NA
	TEW	200			ms	
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

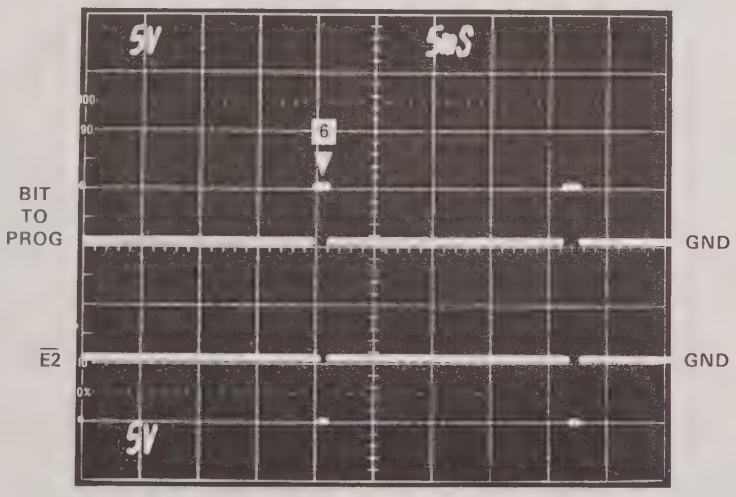
1. *Load RAM with hex FE for Family 33.*
2. *Load RAM with hex 01 for Family 34, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photo 9 is the erase waveform.*

REVISIONS

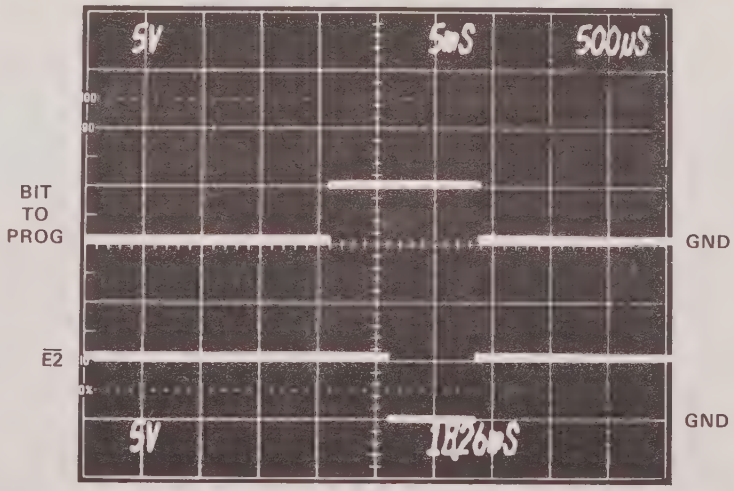
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C73	11/82
		ECN #4831			
		ECN #5023		C73	3/84

DATA I/O ISSAQUAH, WA

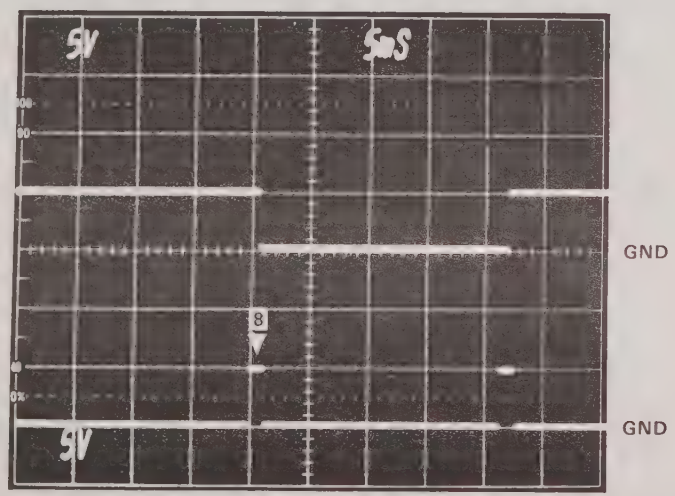
TITLE: TIMING DIAGRAM		DRAWN BY:
FAMILY CODES 33, 34		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


5V
5mS
6
BIT
TO
PROG
GND
E2
GND
5V

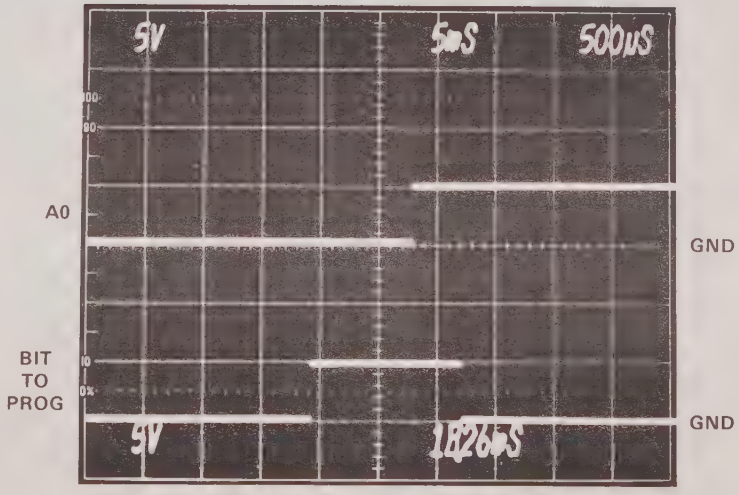
5


5V
5mS
500µS
BIT
TO
PROG
GND
E2
GND
5V
GND

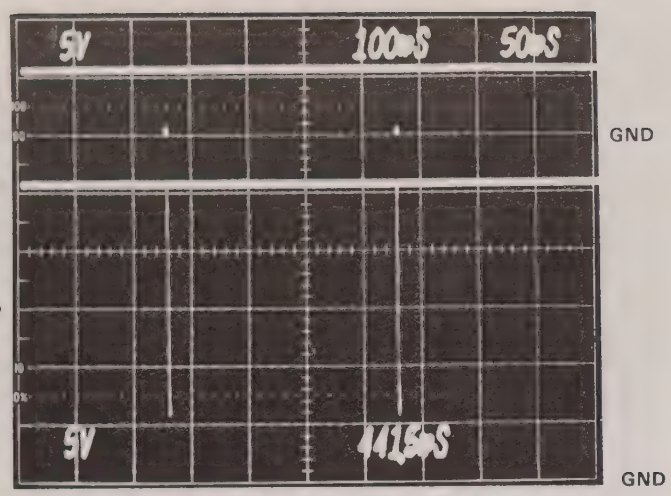
6


5V
5mS
A0
GND
8
BIT
TO
PROG
GND
5V

7


5V
5mS
500µS
A0
GND
BIT
TO
PROG
GND
5V
GND

8



9

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10-950-0059

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831			
		ECN #5023		C7J	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 33, 34

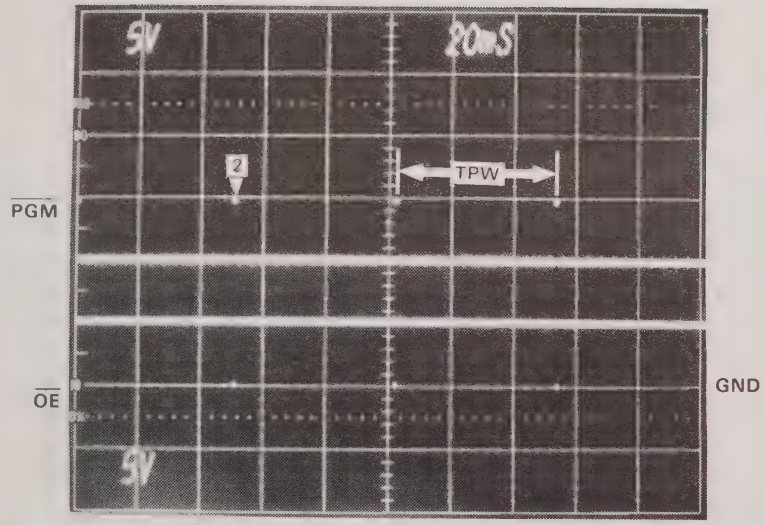
DRAWN BY: cca

CHECKED BY:

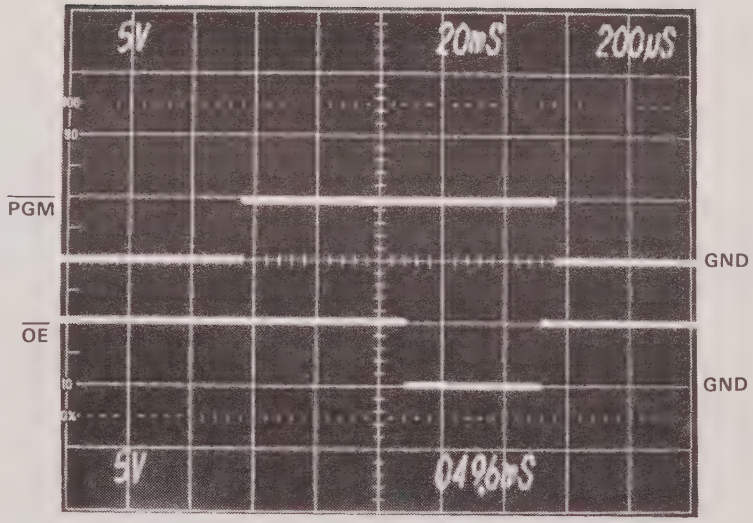
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

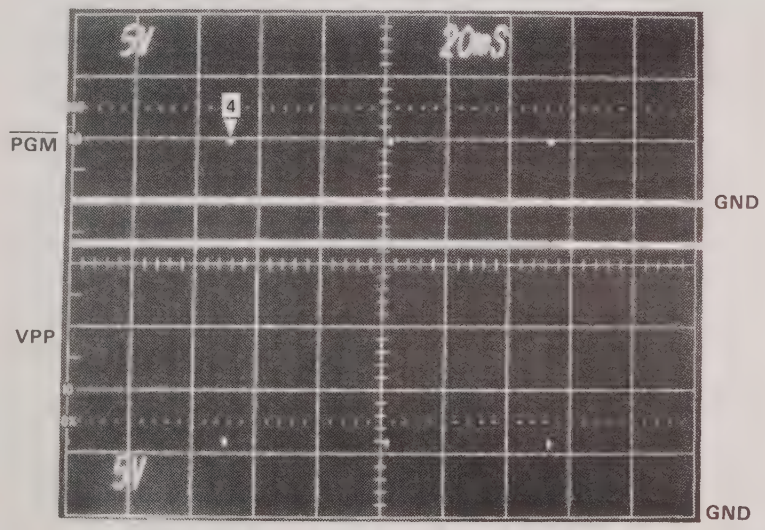
SHEET 2/2


5V
20mS
2
TPW
PGM
OE
GND
5V

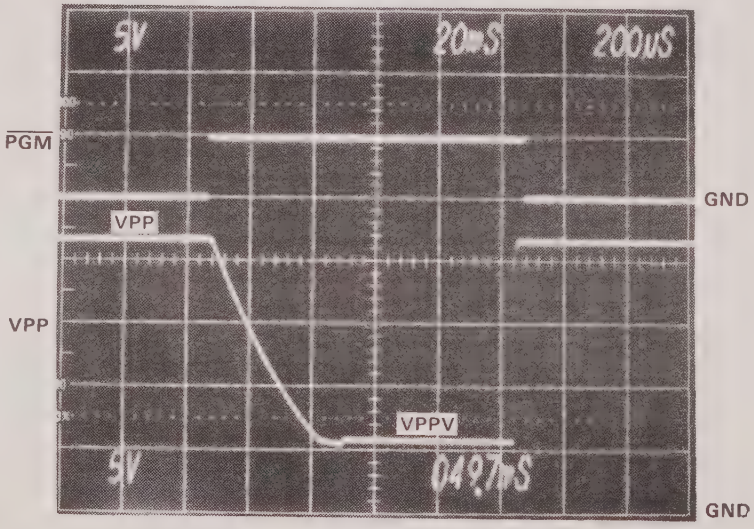
1


5V
20mS
200uS
PGM
GND
OE
GND
5V
049.6mS

2


5V
20mS
4
PGM
GND
VPP
5V
GND

3


5V
20mS
200uS
PGM
GND
VPP
VPP
VPPV
5V
049.7mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP	3.8	5.0	6.0	V	
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.00	5.25	V	
	TPW	48	50	52	ms	
	TR					NA
	TF					NA
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

GND

NOTES

1. *Load RAM with hex FE for Family 35.*
2. *Load RAM with hex 01 for Family 36, and bit-to-prog waveform becomes bit-no-prog waveform.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CTZ	11/82
		ECN #4831		[illegible]	[illegible]
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 35, 36

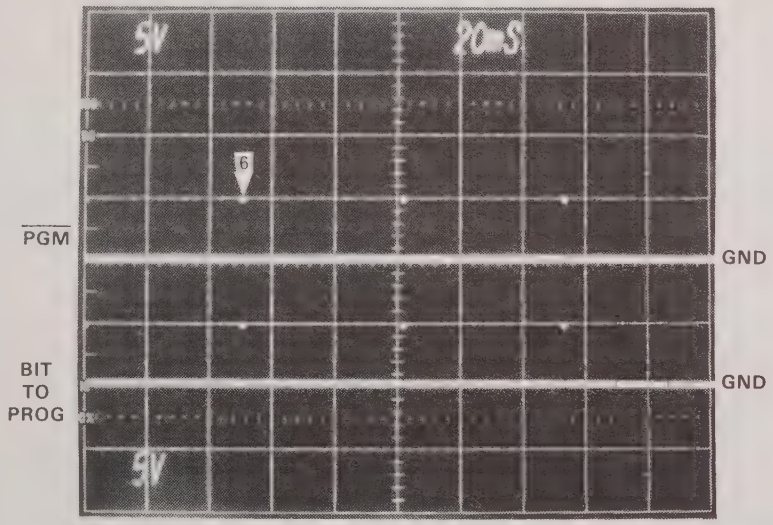
DRAWN BY: BG

CHECKED BY:

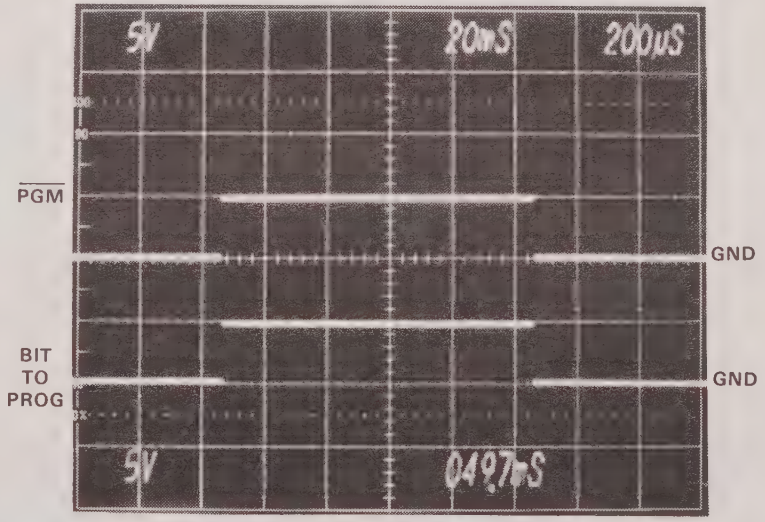
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

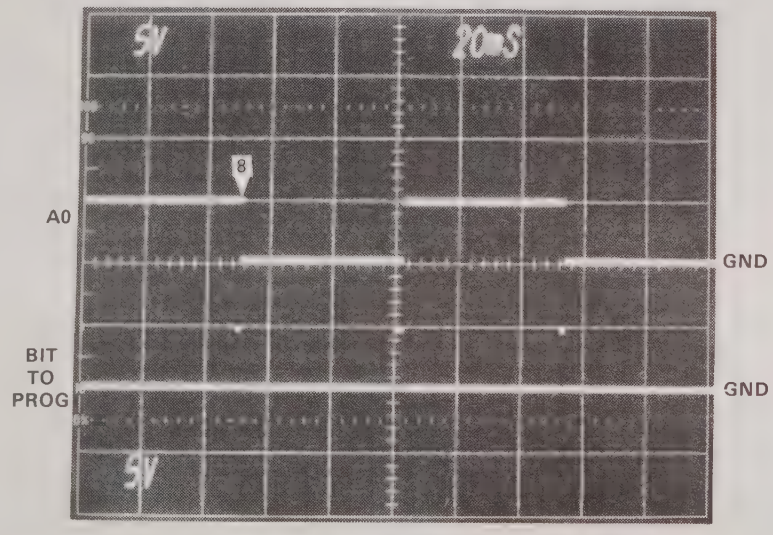
SHEET 1/2


5V
20mS
6
PGM
GND
BIT
TO
PROG
GND
5V

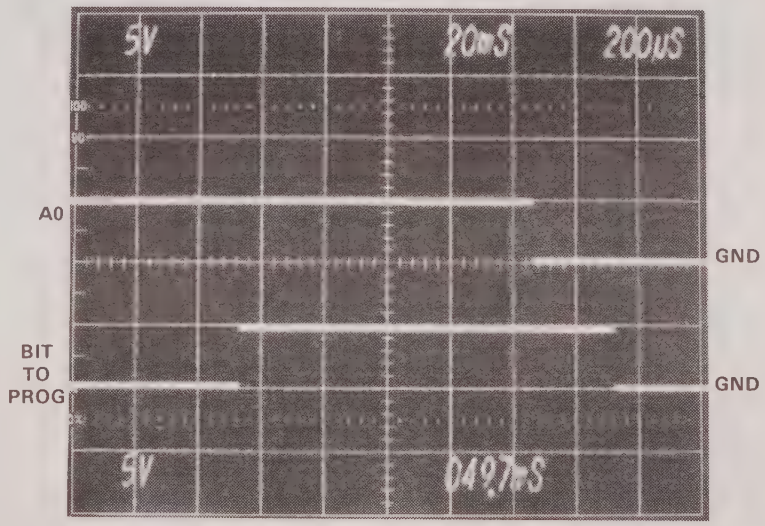
5


5V
20mS
200µS
PGM
GND
BIT
TO
PROG
GND
5V
049.7mS

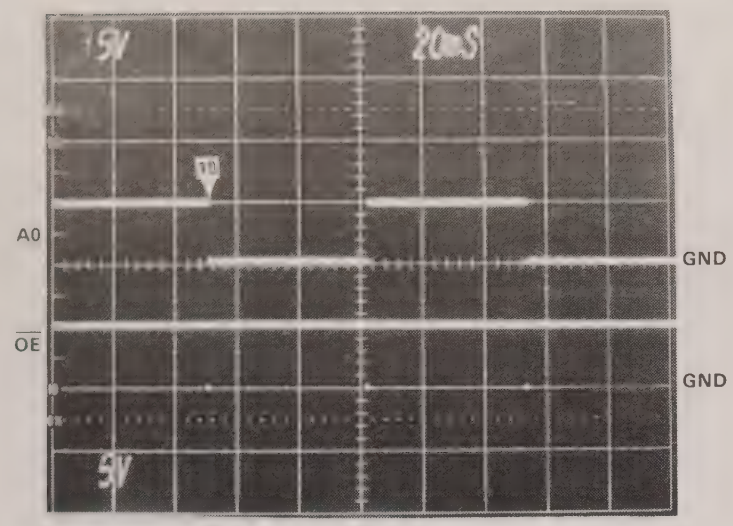
6


5V
20mS
8
A0
GND
BIT
TO
PROG
GND
5V

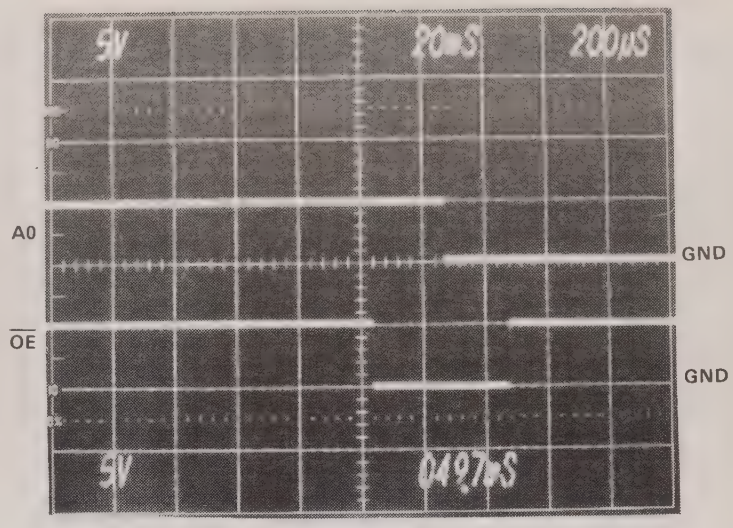
7


5V
20mS
200µS
A0
GND
BIT
TO
PROG
GND
5V
049.7mS

8



9



10

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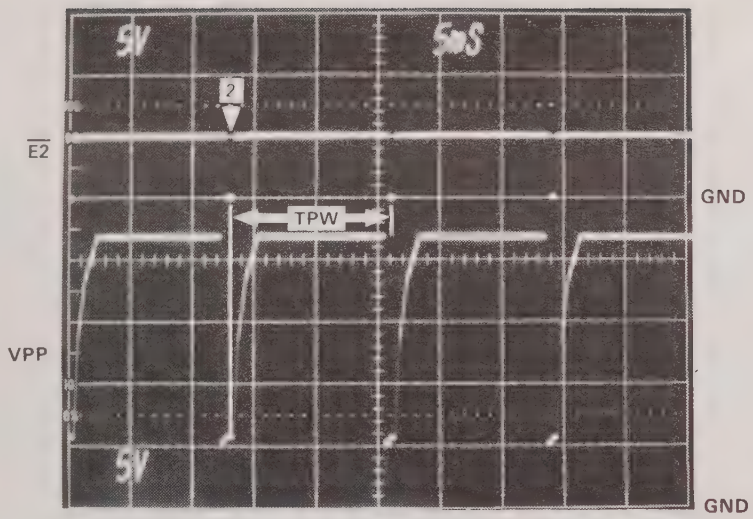
10-950-0059

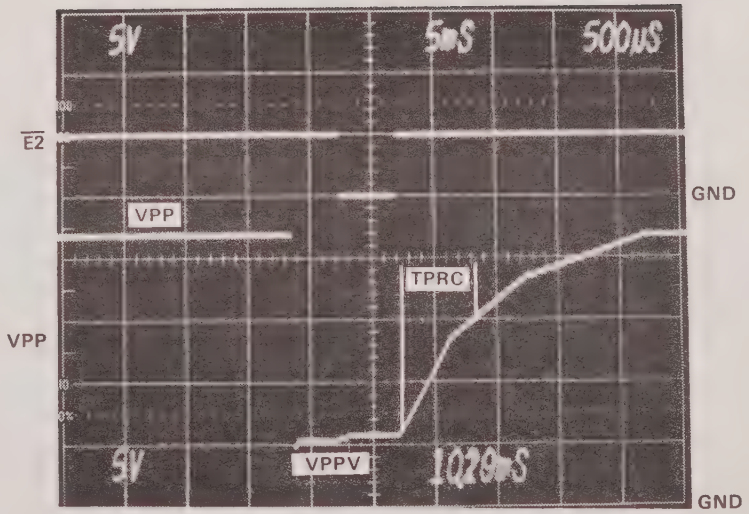
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		22	5-23.

DATA I/O ISSAQUAH, WA

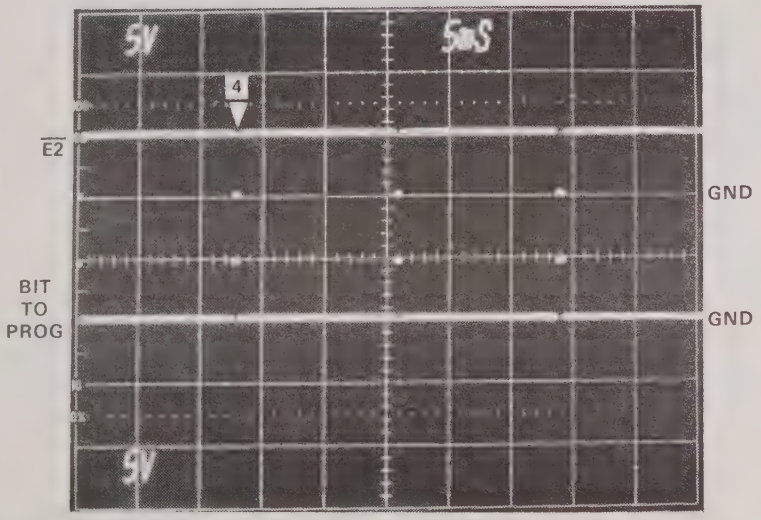
TITLE: TIMING DIAGRAM FAMILY CODES 35, 36			DRAWN BY: BG CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2


5V
5mS
2
E2
TPW
GND
VPP
5V
GND

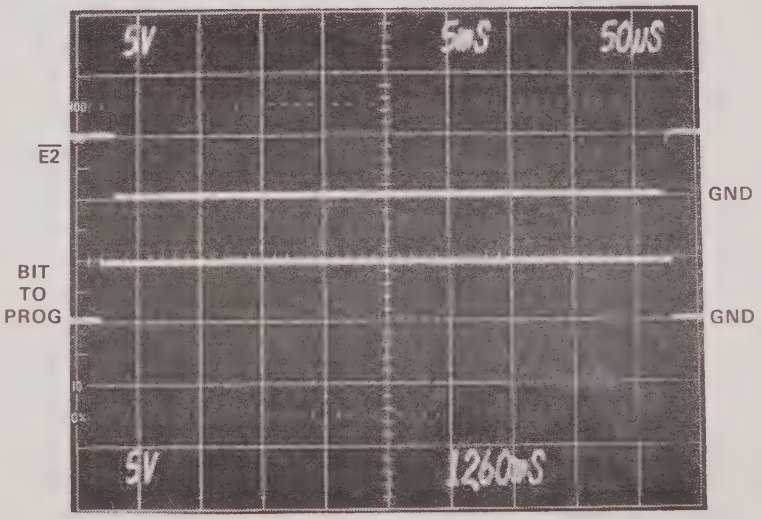
1


5V
5mS
500uS
E2
GND
VPP
TPRC
VPP
5V
VPPV
1029mS
GND

2


5V
5mS
4
E2
GND
BIT
TO
PROG
GND
5V

3


5V
5mS
50uS
E2
GND
BIT
TO
PROG
GND
5V
1260mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.0	5.0	6.0	V	
	VOE	9.0	12.0	15.0	V	
	TPW	9.0	10.0	15.0	ms	
	TPRC	450	600	750	µs	See Note 3
	TF			100	µs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 37.*
2. *Load RAM with hex 01 for Family 38, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *TPRC is measured from 6V to 15.5V.*
4. *Photos 10 and 11 are erase waveforms.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.	11/82
		ECN #4831		KA	5/83
		ECN #5023		CJB	3/84

DATA I/O ISSAQUAH, WA

TITLE **TIMING DIAGRAM**

FAMILY CODES 37, 38

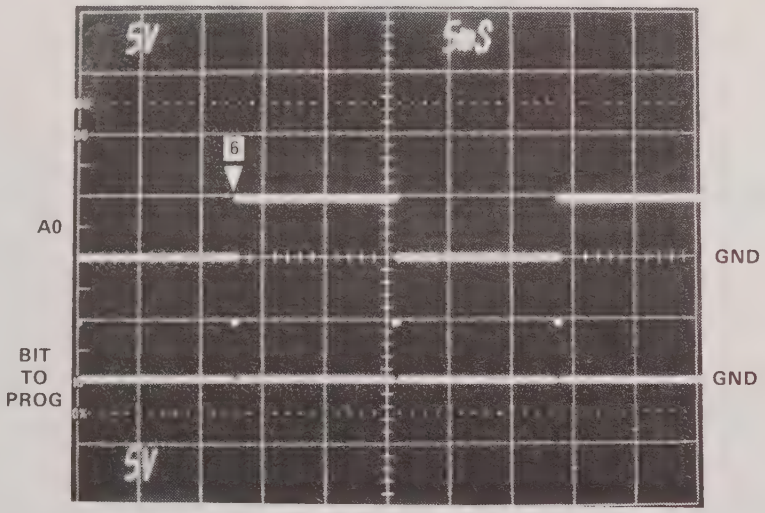
DRAWN BY: KEV

CHECKED BY:

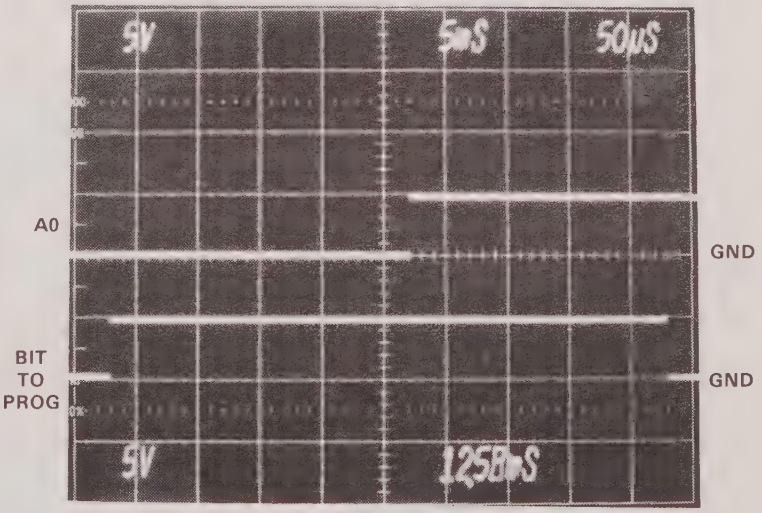
SIZE	CODE IDENT NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

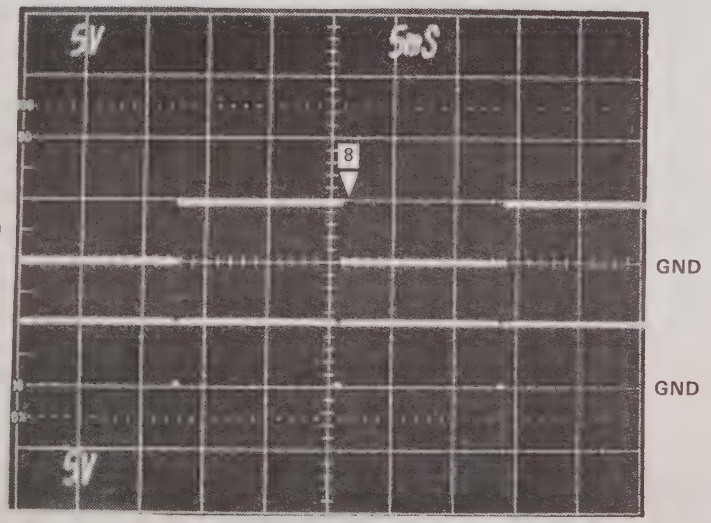
SHEET 1/3


5V
5mS
6
A0
GND
BIT
TO
PROG
GND
5V

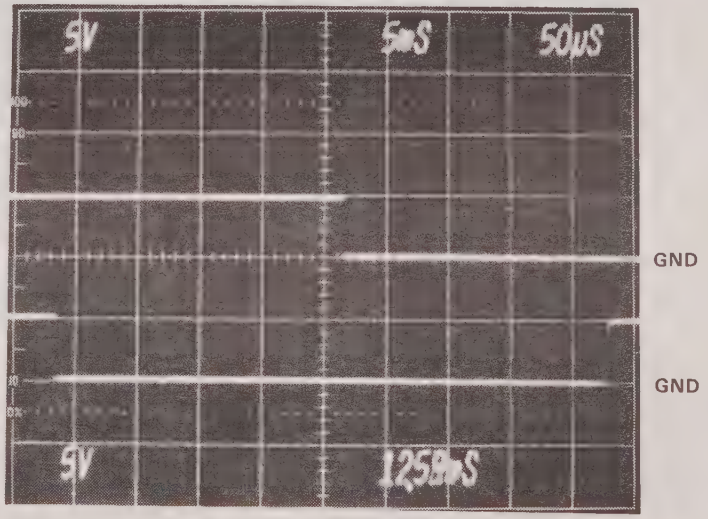
5


5V
5mS
50µS
A0
GND
BIT
TO
PROG
GND
5V
125mS

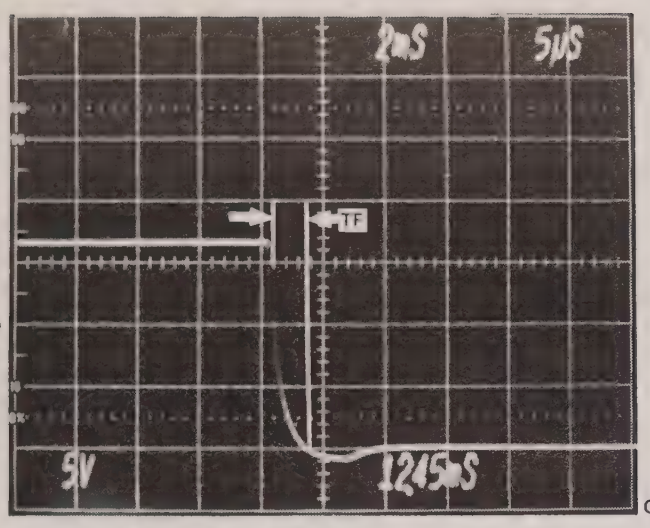
6


5V
5mS
8
A0
GND
E2
GND
5V

7

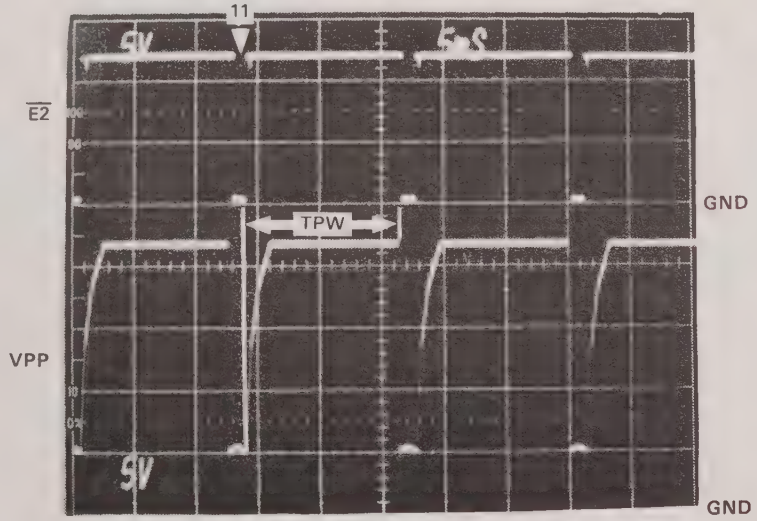

5V
5mS
50µS
A0
GND
E2
GND
5V
125mS

8

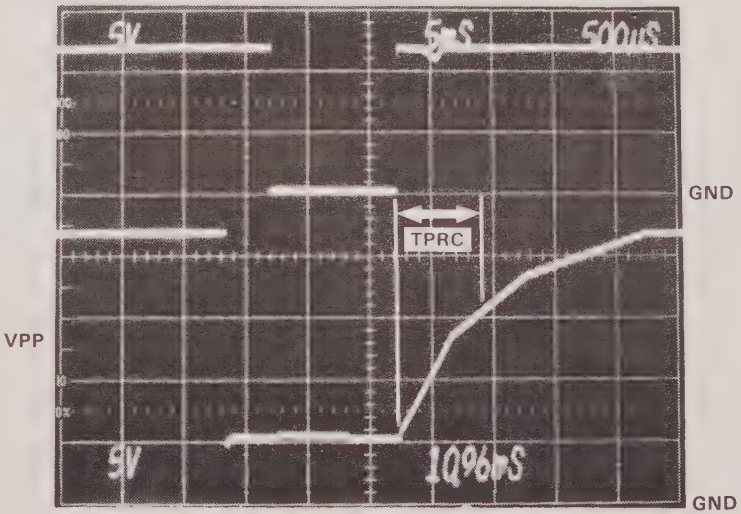


9

REVISIONS						DATA I/O ISSAQUAH, WA	
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE		
		Release		CJB	11/82	TITLE: TIMING DIAGRAM	DRAWN BY: KEV
		ECN #4831		KA	[illegible]		
						FAMILY CODES 37, 38	CHECKED BY:
						SIZE: B	CODE IDENT. NO.: 54193
						DRAWING NO.: 33-950-0059	
						SCALE	SHEET 2/3



10

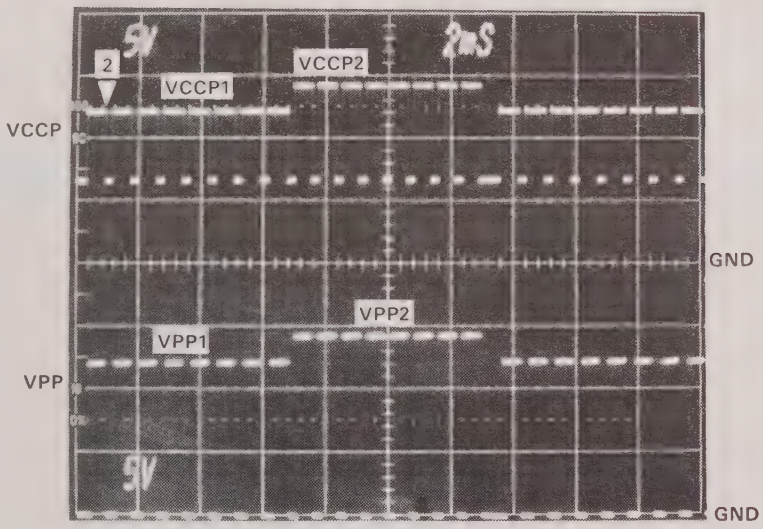


11

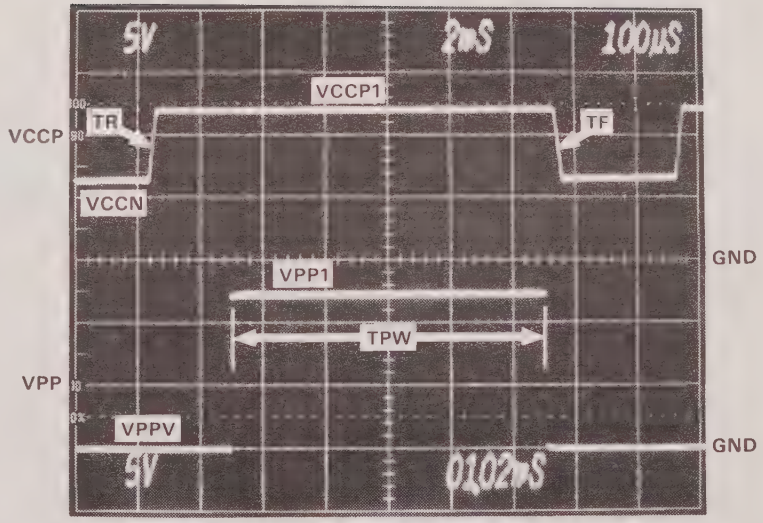
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.3	11/82
		ECN #4831		G	5/83

DATA I/O ISSAQUAH, WA

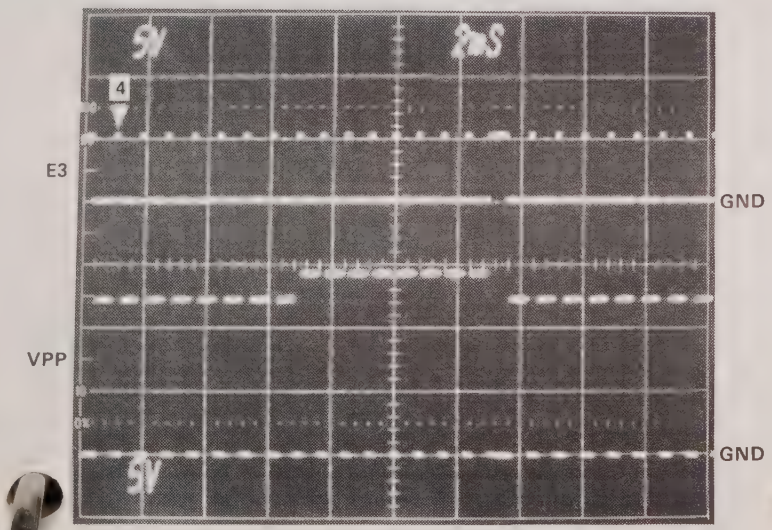
TITLE: TIMING DIAGRAM FAMILY CODES 37, 38		DRAWN BY: KEV CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 3/3


5V
2mS
2
VCCP1
VCCP2
VCCP
GND
VPP2
VPP1
VPP
5V
GND

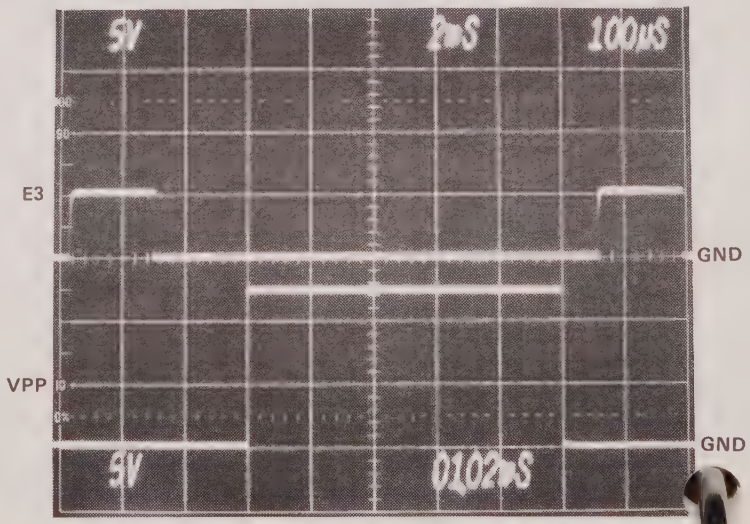
1


5V
2mS
100µS
VCCP1
VCCP
TR
TF
VCCN
GND
VPP1
TPW
VPP
VPPV
GND
5V
0102mS

2


5V
2mS
4
E3
GND
VPP
GND
5V

3


5V
2mS
100µS
E3
GND
VPP
GND
5V
0102mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCN	6.0	6.5	7.0	V	
	VCCP1	11.5	12.0	12.5	V	Pulses 1-8
	VCCP2	13.5	14.0	14.5	V	Pulses 9-16
	VPP1	11.5	12.0	12.5	V	Pulses 1-8
	VPP2	13.5	14.0	14.5	V	Pulses 9-16
	VPPV	0.0		1.0	V	
	VOP1	11.5	12.0	12.5	V	Pulses 1-8
	VOP2	13.5	14.0	14.5	V	Pulses 9-16
	TPW	450	500	550	µs	
	T_R	1.0			µs	
	T_F	1.0			µs	
	Reject		16		Pulses	
	Overprogram		2		Pulses	
1ST PASS VERIFY	VCC	3.9	4.0	4.1	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	6.1	7.1	8.1	V	701-1655/TP4
	Low Load	6.1	7.1	8.1	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	4.0	4.1	4.2	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	8.7	9.7	10.7	V	701-1655/TP3

NOTES

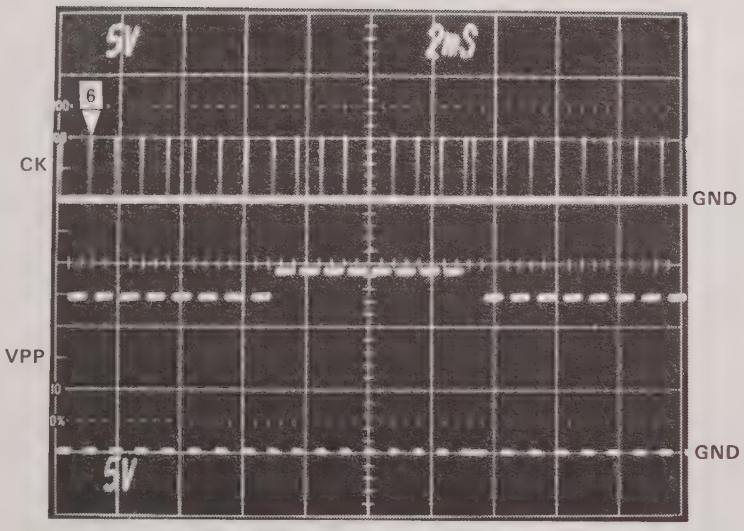
1. *Load RAM with hex FE for Family 39.*
2. *Load RAM with hex 01 for Family 40.*
3. *V_{CC} is loaded with a 100 Ω, 2-watt resistor.*

REVISIONS

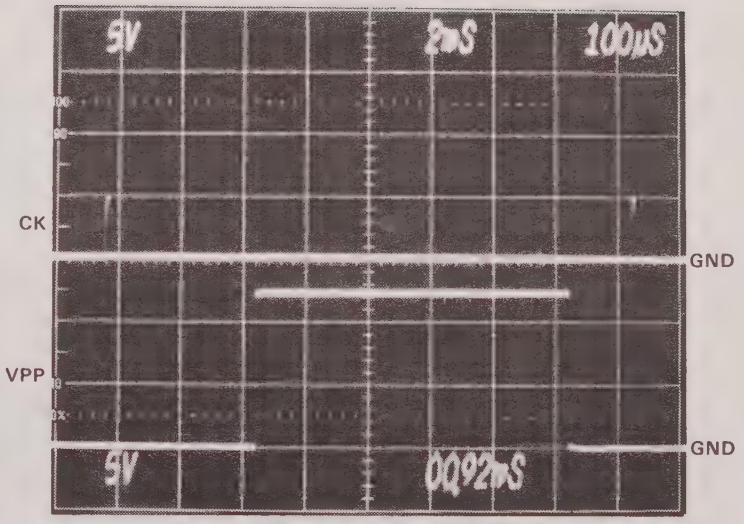
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CTJ	11/82
		ECN #4831		[illegible]	[illegible]
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

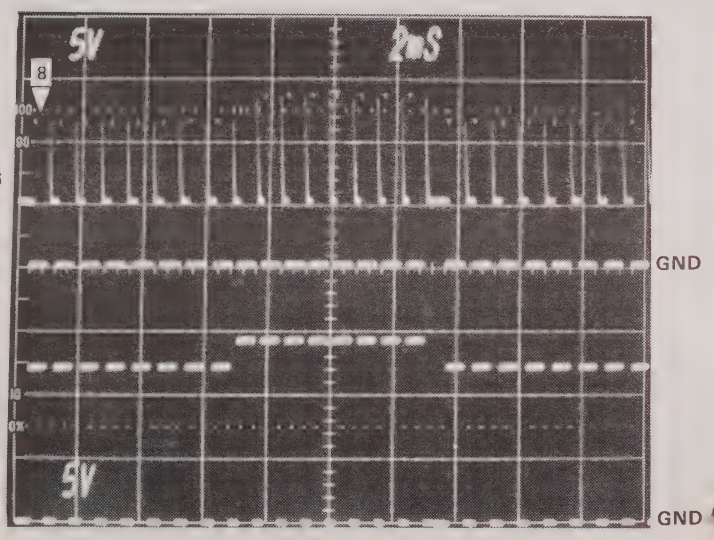
TITLE: TIMING DIAGRAM FAMILY CODES 39, 40	DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	
SCALE	SHEET 1/3


5V
2mS
6
CK
GND
VPP
GND
5V

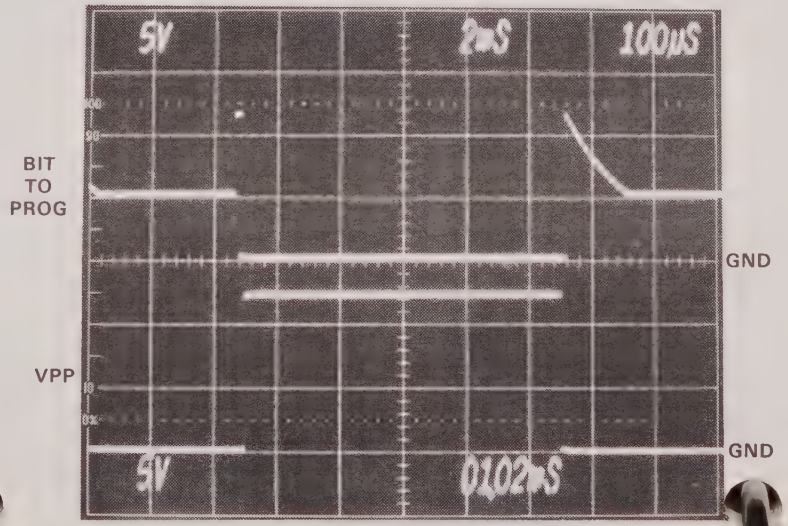
5


5V
2mS
100µS
CK
GND
VPP
GND
5V
0Q92mS

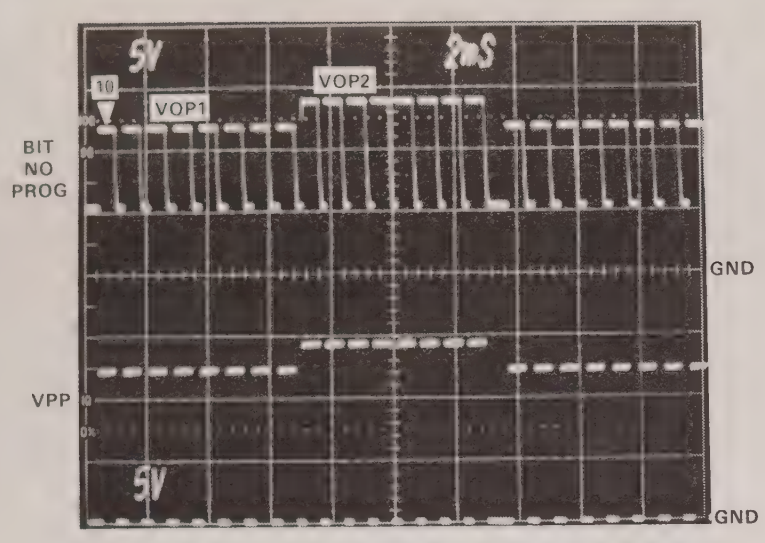
6


5V
2mS
8
BIT
TO
PROG
GND
VPP
5V
GND

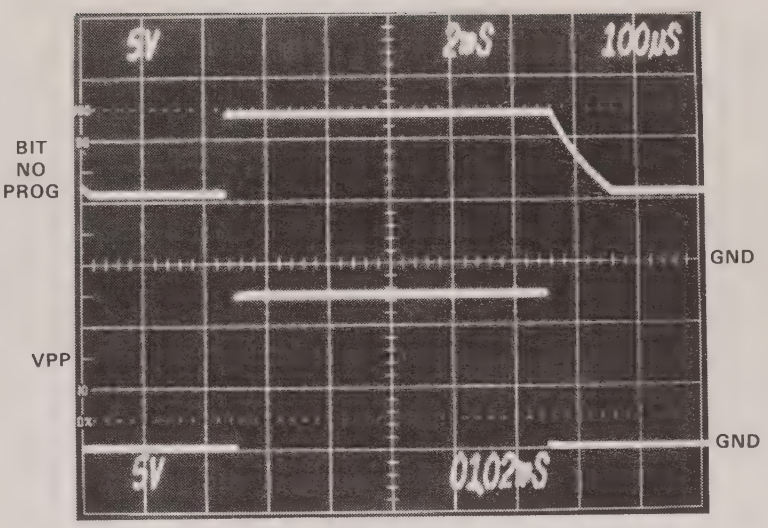
7


5V
2mS
100µS
BIT
TO
PROG
GND
VPP
GND
5V
0102mS

8



9



1C

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		[illegible]	[illegible]

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 39, 40

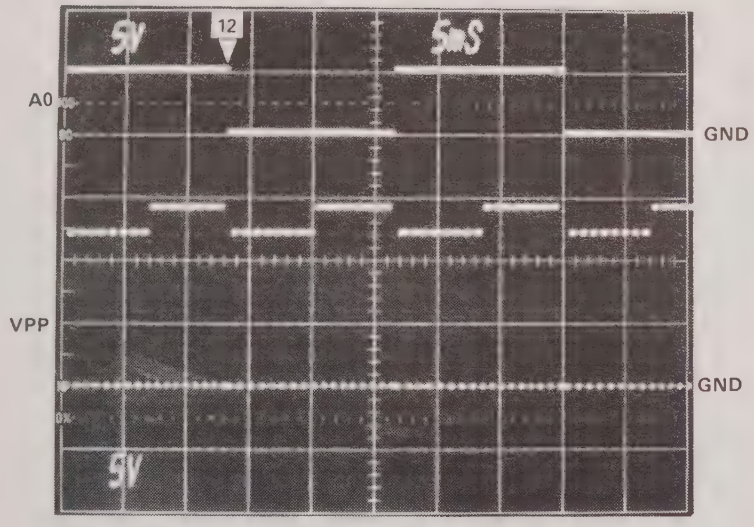
DRAWN BY:

CHECKED BY:

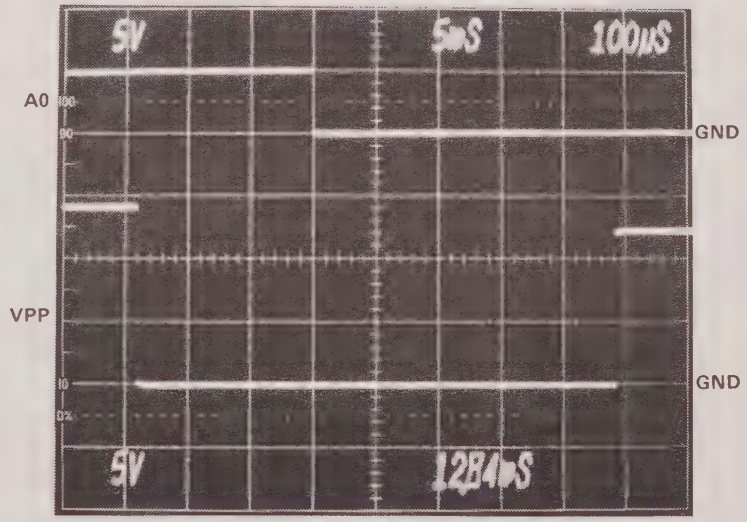
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 2/3



11

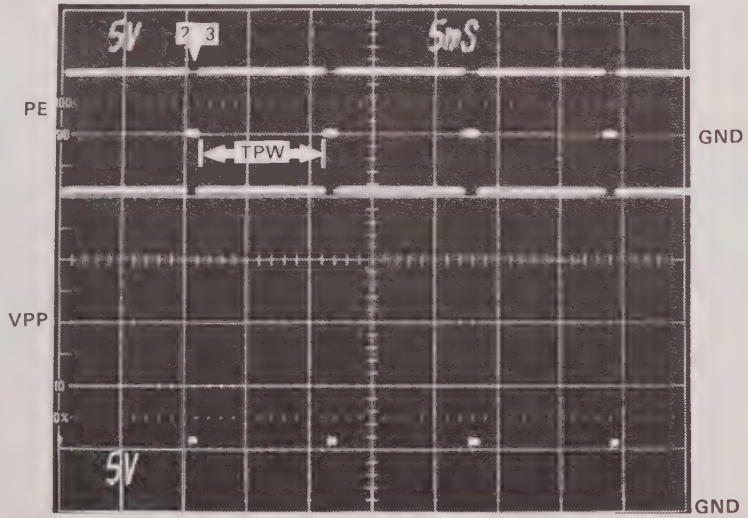


12

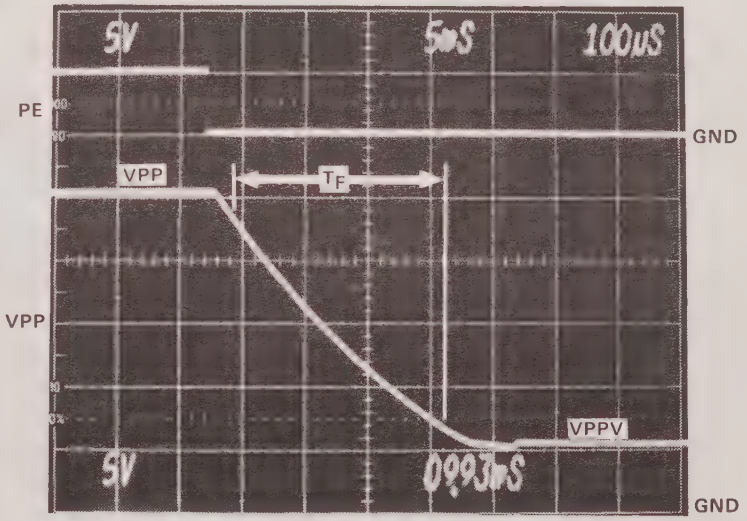
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		[illegible]	[illegible]

DATA I/O ISSAQUAH, WA

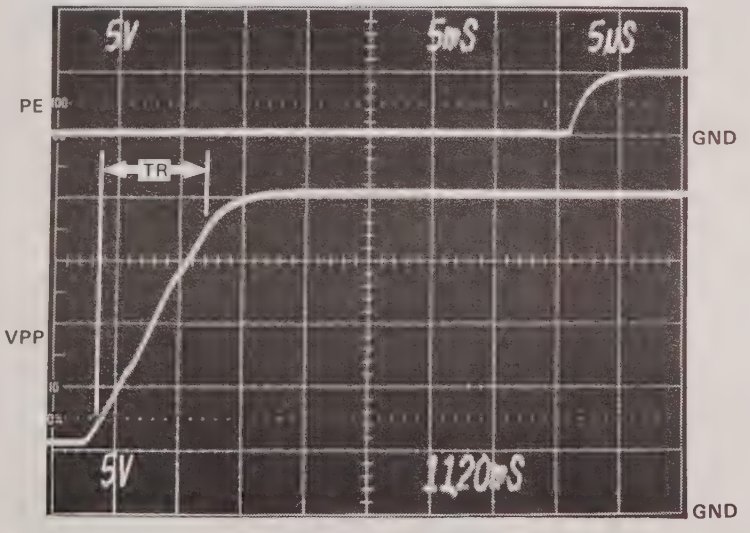
TITLE: TIMING DIAGRAM FAMILY CODES 39, 40		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0099
SCALE		SHEET 3/3


5V
2 3
5mS
PE
GND
TPW
VPP
5V
GND

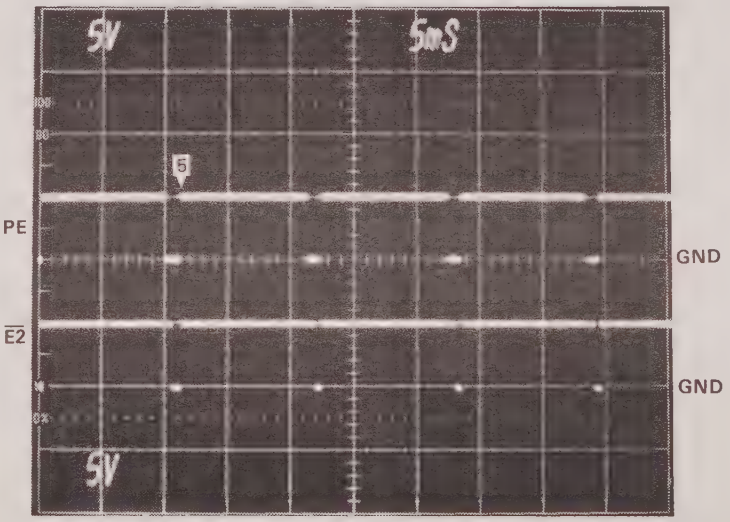
1


5V
5mS
100uS
PE
GND
VPP
TF
VPP
VPPV
5V
0.993mS
GND

2


5V
5mS
5uS
PE
GND
TR
VPP
5V
1120mS
GND

3


5V
5mS
5
PE
GND
E2
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.00	5.25	V	
	TPW	9.8	10.0	10.2	ms	
	TR	50			ns	
	TEP	98	100	102	ms	
	TF	50			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 43.*
2. *Load RAM with hex 01 for Family 44, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photo 10 is the erase waveform.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		[illegible]	11/82
		ECN #4831		[illegible]	[illegible]
		ECN #5023		C73	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 43, 44

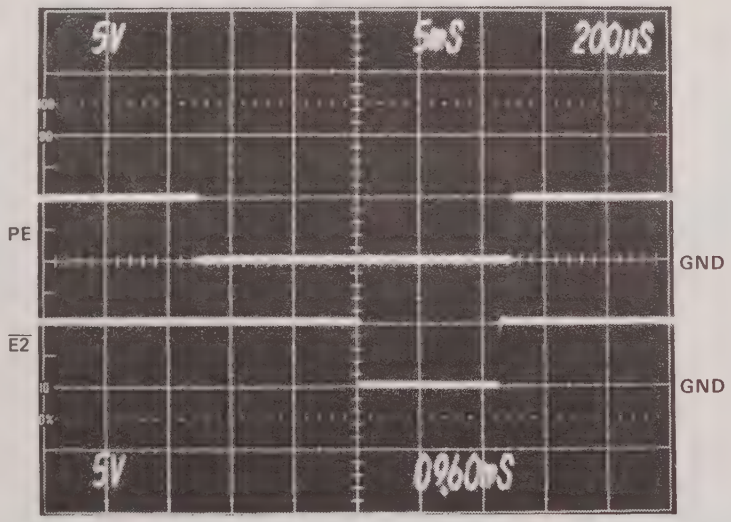
DRAWN BY: EE

CHECKED BY:

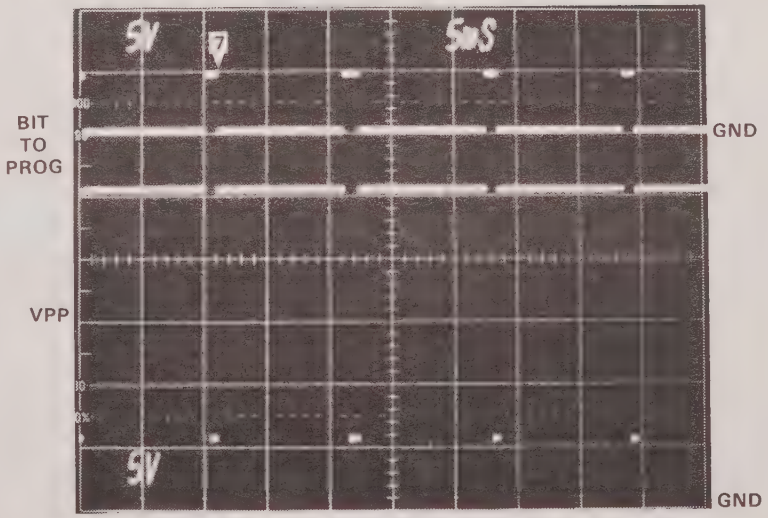
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

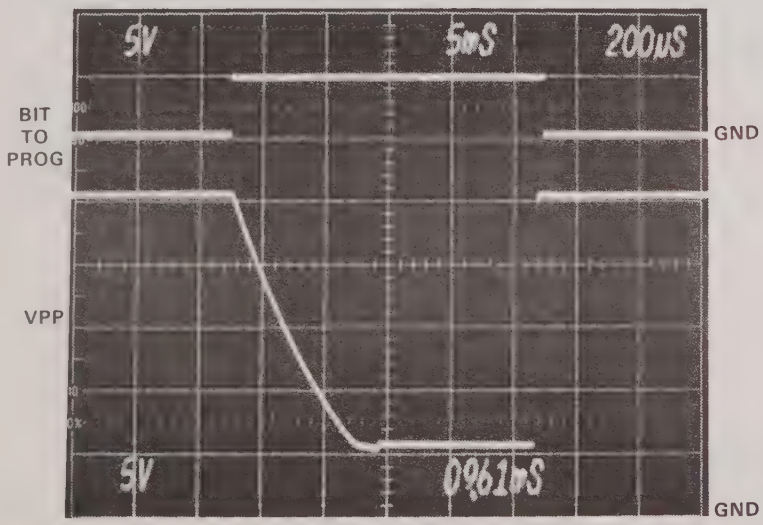
SHEET 1/2


5V
5mS
200uS
PE
GND
E2
GND
5V
0960mS

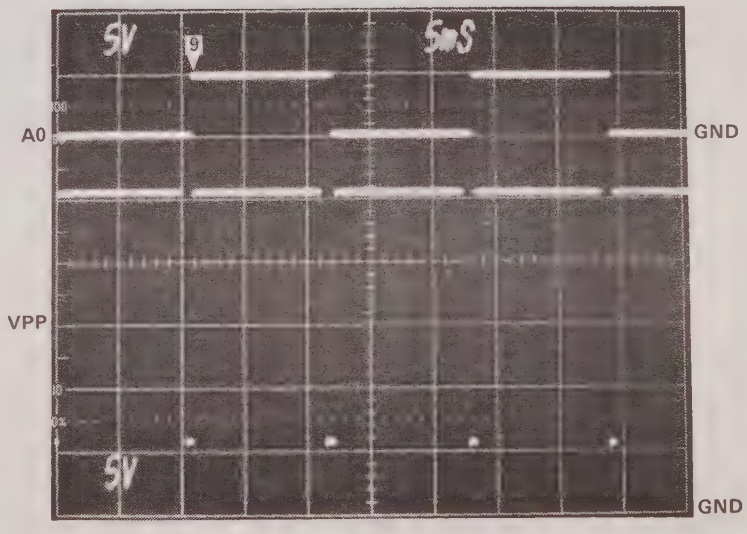
5


5V
7
5mS
BIT
TO
PROG
GND
VPP
5V
GND

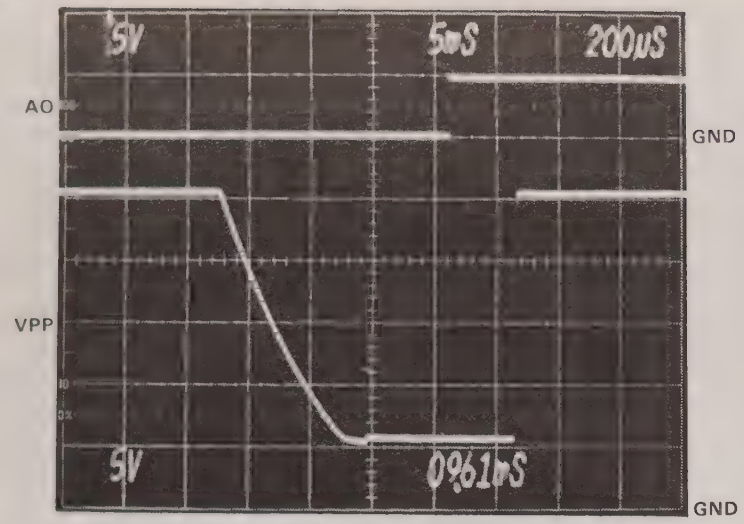
6


5V
5mS
200uS
BIT
TO
PROG
GND
VPP
5V
0961mS
GND

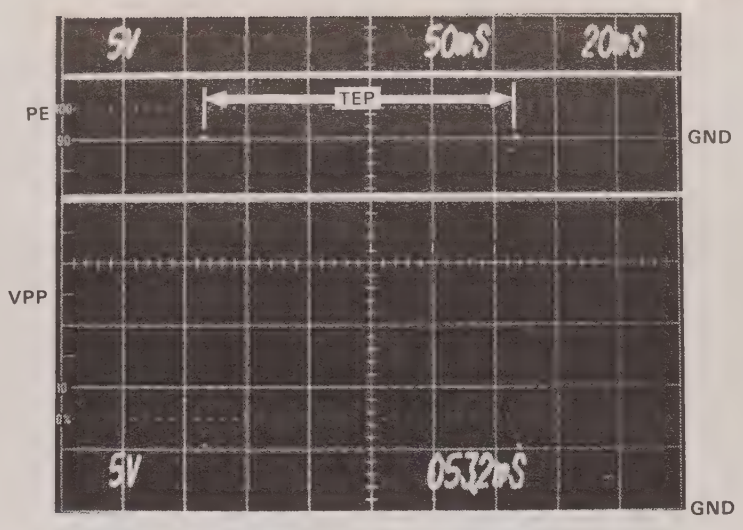
7


5V
9
5mS
A0
GND
VPP
5V
GND

8



9



10

B-79
10-950-0059

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.3	11/82
		ECN #4831		JN	2/84
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 43, 44

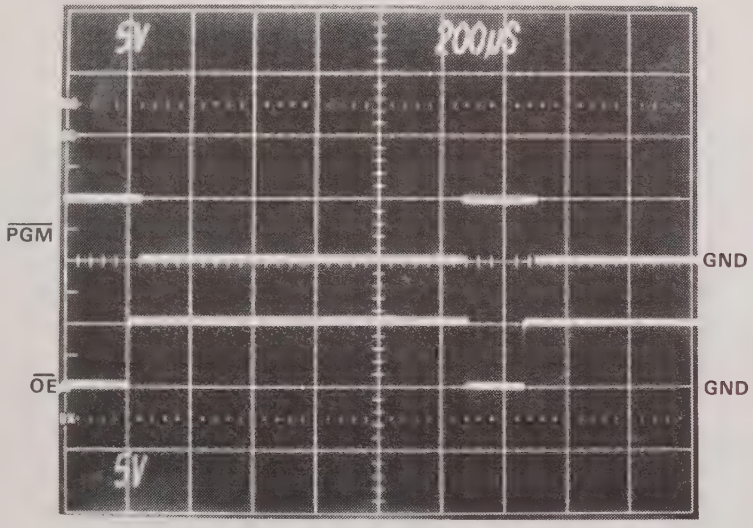
DRAWN BY: EE

CHECKED BY:

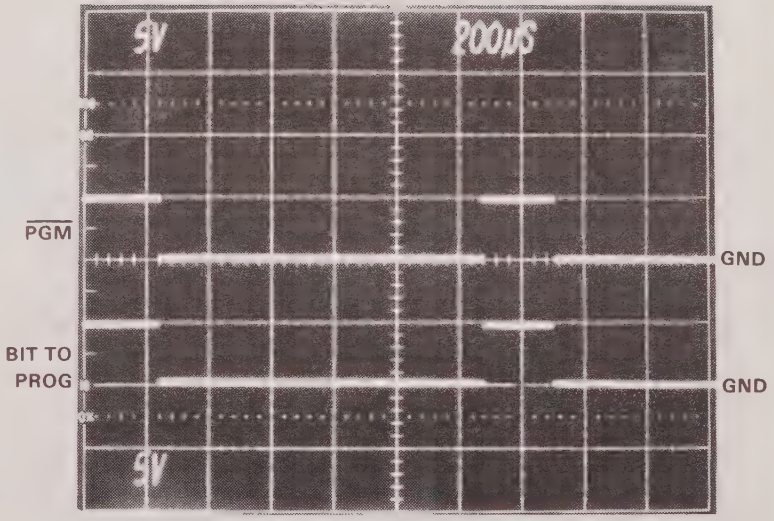
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

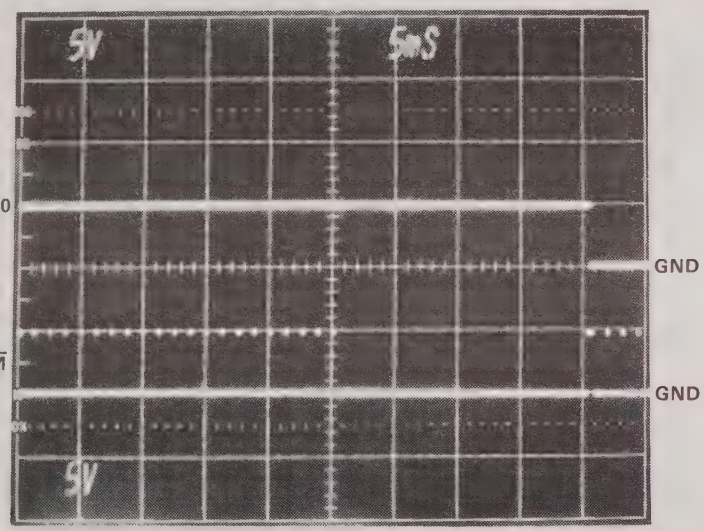
SHEET 2/2


5V
200µS
PGM
GND
OE
GND
5V

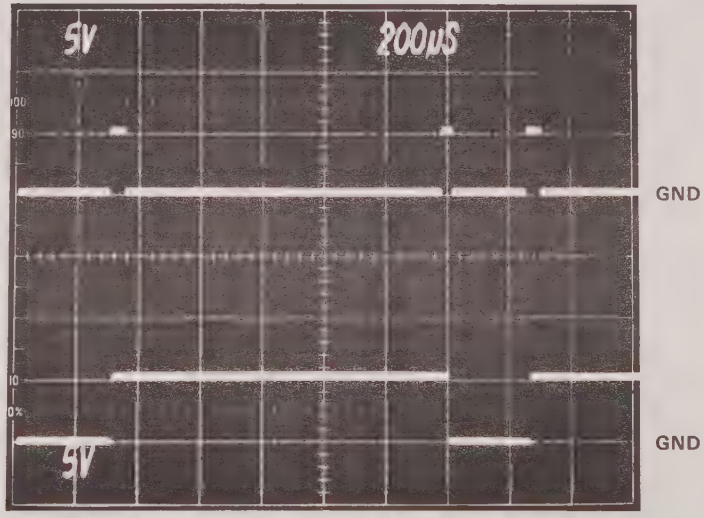
1


5V
200µS
PGM
GND
BIT TO
PROG
GND
5V

2


5V
5mS
A0
GND
PGM
GND
5V

3


5V
200µS
PGM
GND
OE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.00	6.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	Not shown
	VPPV					NA
	TPW	.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		20		Pulses	
	Overprogram		1		Pulse	See note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

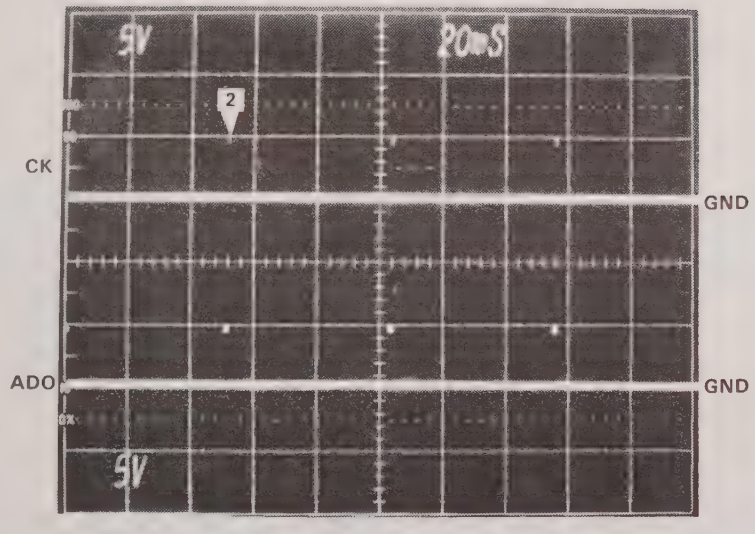
NOTES

1. *Load RAM with hex FE for Family 45.*
2. *Load RAM with hex 01 for Family 46 and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 1 ms times the number of programming pulses required to program the location.*
4. *Photo 4 is for Pinout 32.*

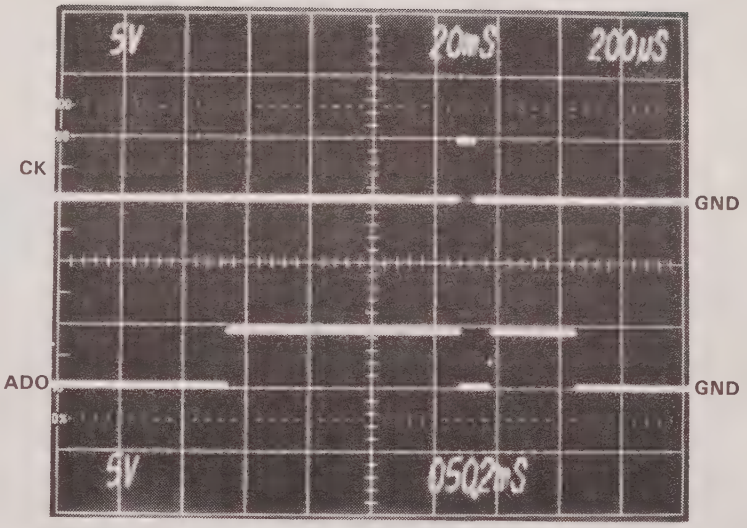
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		JH	5/5
		ECN #5023		CJZ	3/84

DATA I/O

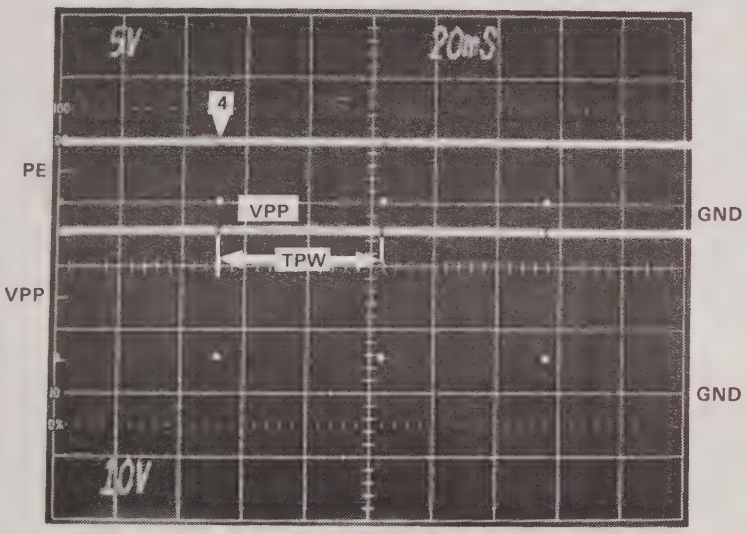
TITLE: TIMING DIAGRAM FAMILY CODES 45, 46		DRAWN BY:
		CHECKED BY: JH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 1


5V
20mS
2
CK
GND
ADO
GND
5V

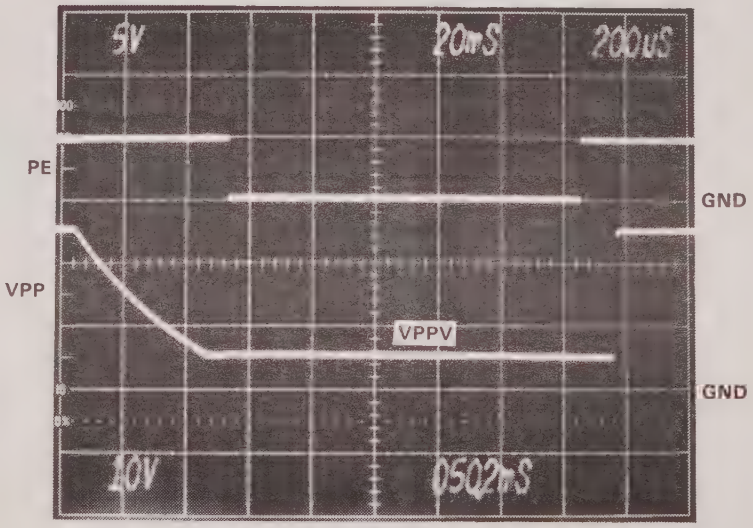
1


5V
20mS
200uS
CK
GND
ADO
GND
5V
0502mS

2


5V
20mS
4
PE
VPP
GND
TPW
VPP
GND
10V

3


5V
20mS
200uS
PE
GND
VPP
VPPV
GND
10V
0502mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not shown
	VOP					NA
	VPP	24.5	25.0	25.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

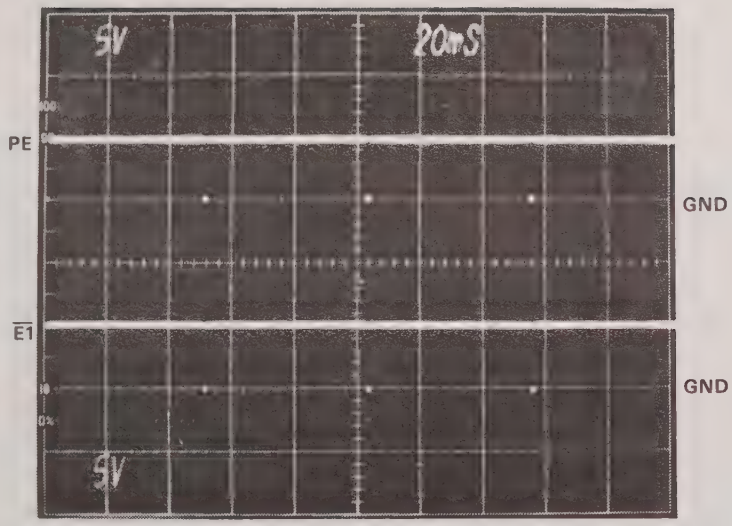
1. *Load RAM with hex FE for Family 47.*
2. *Load RAM with hex 01 for Family 48 and bit-to-prog waveform becomes bit-no-prog waveform.*

REVISIONS

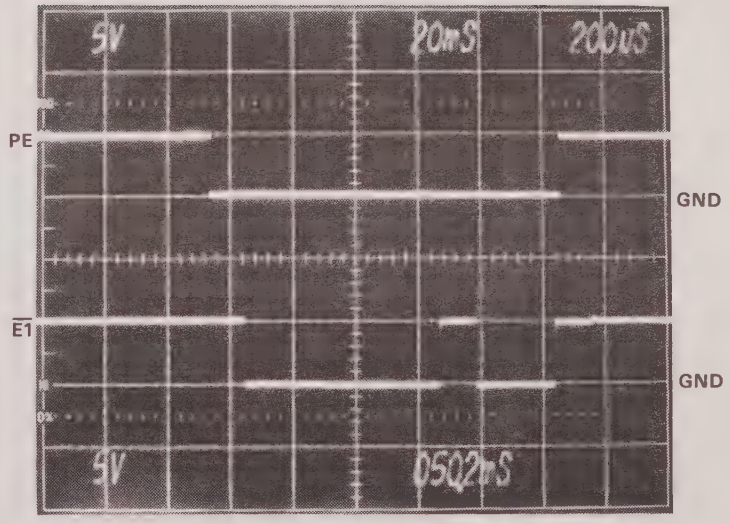
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	2/6/84
		ECN #5023		CJZ	3/84

DATA I/O

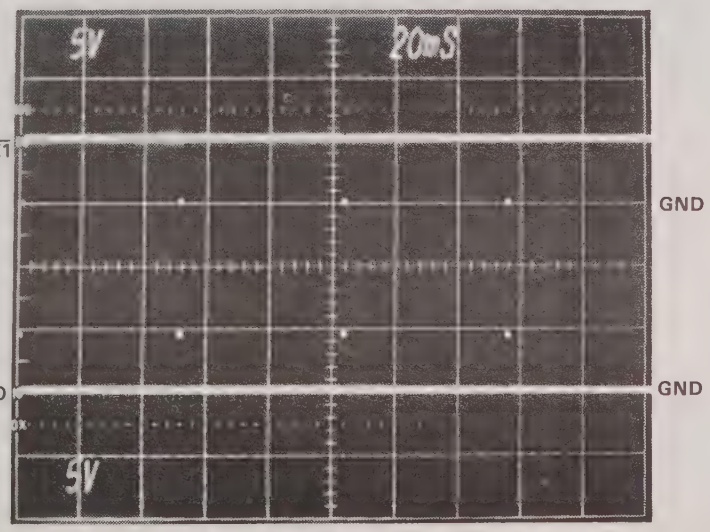
TITLE: TIMING DIAGRAM FAMILY CODES 47, 48		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


5V
20mS
PE
GND
E1
GND
5V

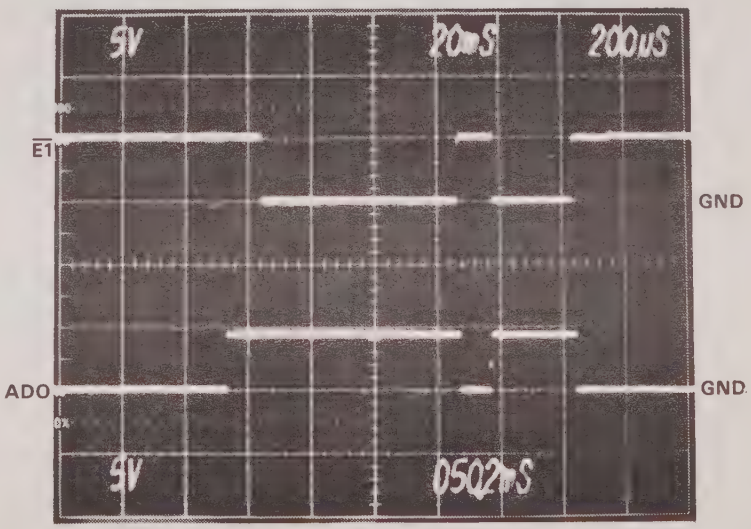
5


5V
20mS
200uS
PE
GND
E1
GND
5V
0502mS

6


5V
20mS
E1
GND
ADO
GND
5V

7


5V
20mS
200uS
E1
GND
ADO
GND
5V
0502mS

8

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		[illegible]	[illegible]

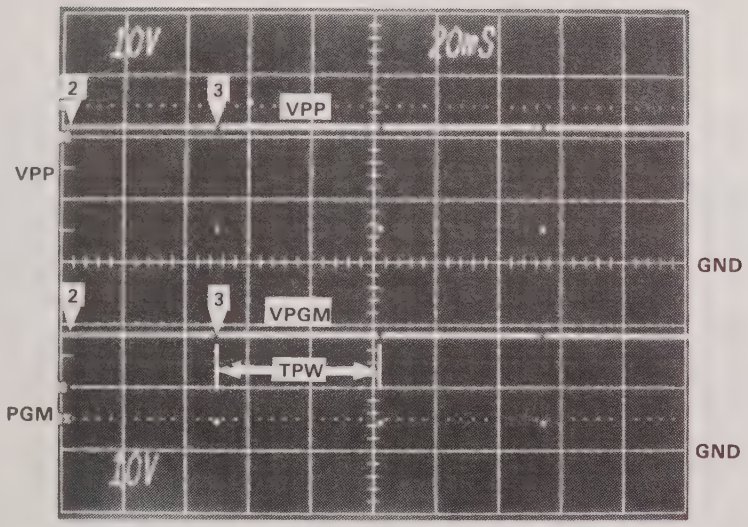
DATA I/O

TITLE	DRAWN BY:
TIMING DIAGRAM FAMILY CODES 47, 48	CHECKED BY: 27

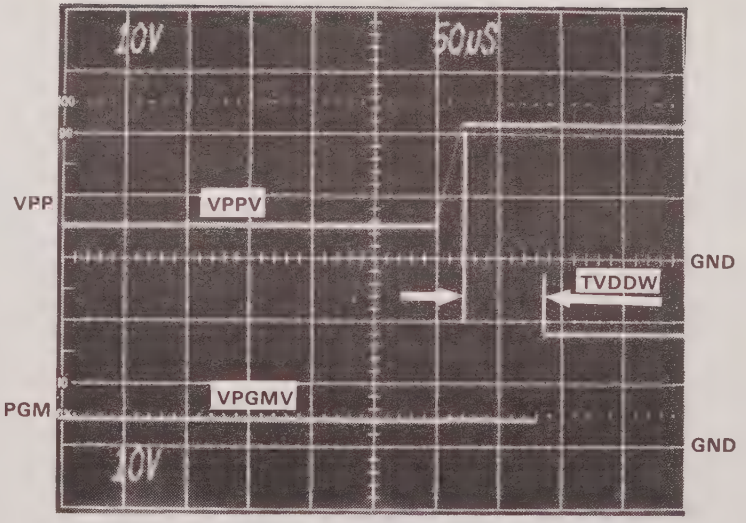
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

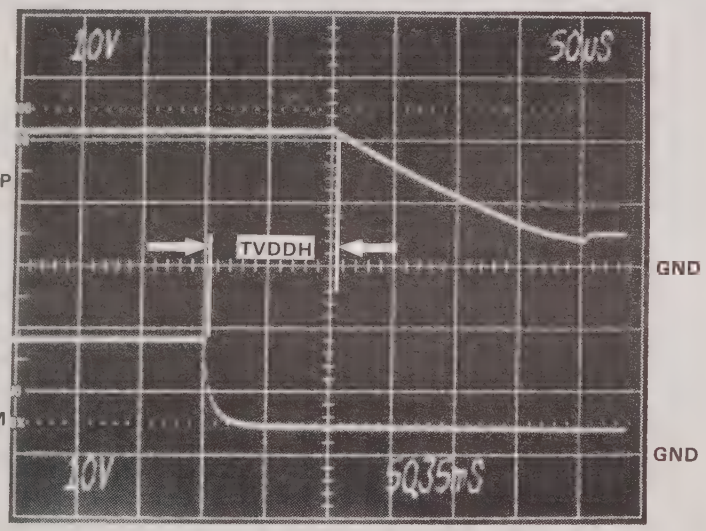
SHEET 2 of 2


10V
20mS
2
3
VPP
VPP
GND
2
3
VPGM
TPW
PGM
GND
10V

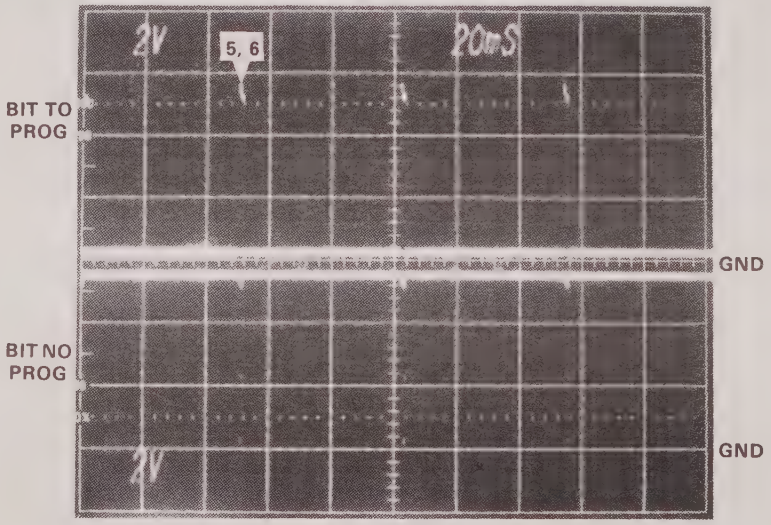
1


10V
50uS
VPP
VPPV
GND
TVDDW
PGM
VPGMV
GND
10V

2


10V
50uS
VPP
TVDDH
GND
PGM
GND
10V

3


2V
5, 6
20mS
BIT TO
PROG
GND
BIT NO
PROG
GND
2V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.9	5.0	5.1	V	Not shown
	VEA	17.5	18.0	18.5	V	Not shown
	VPP	20.5	21.0	21.5	V	
	VPPV	4.8	5.0	5.2	V	
	VPGM	17.5	18.0	18.5	V	
	VPGMV	4.0		5.1	V	
	TVDDW	0		1.0	ms	
	TVDDH	0		1.0	ms	
	TPW	50		60	ms	
	TWW	17			µs	See note 3
	TAW	17			µs	See note 3
	TWA	17			µs	See note 3
	Reject Overprogram		1 0		Pulse Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

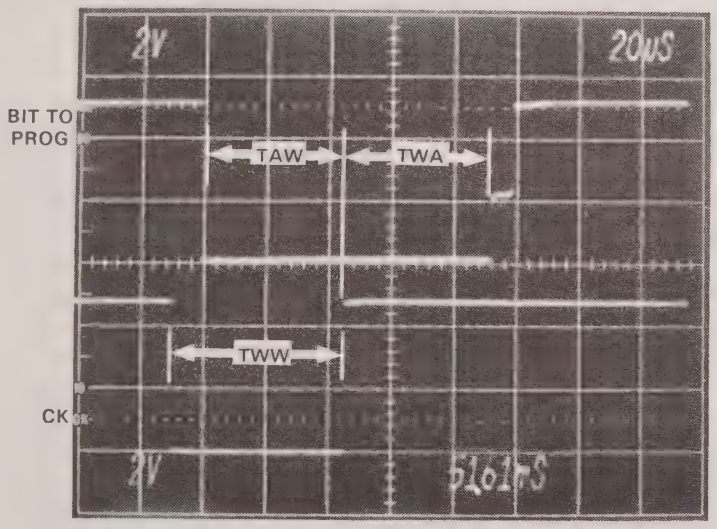
1. *Load RAM with hex FE for Family 49.*
2. *Load RAM with hex 01 for Family 50 and bit-to-prog waveform becomes bit-no-prog waveform and vice versa.*
3. *4TCY = 17 us @ 3.579545 MHz*

REVISIONS

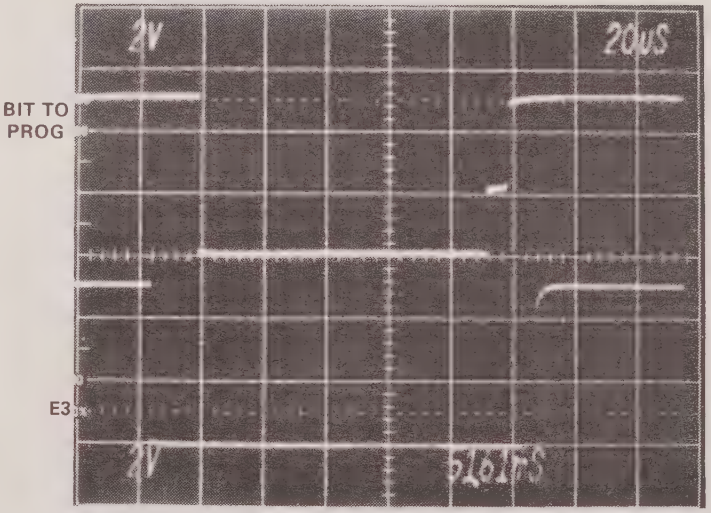
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		CH	2/83
		ECN #5023		CTB	3/84

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES 49, 50	DRAWN BY: CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193
DRAWING NO.: 33-950-0059	
SCALE	SHEET 1 of 2


2V
20uS
BIT TO PROG
TAW
TWA
TWW
CK
2V
5161-5

5

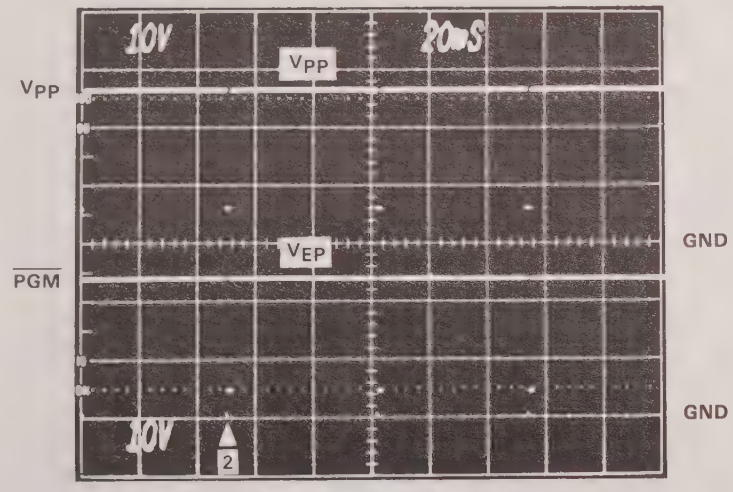

2V
20uS
BIT TO PROG
E3
2V
5161-5

6

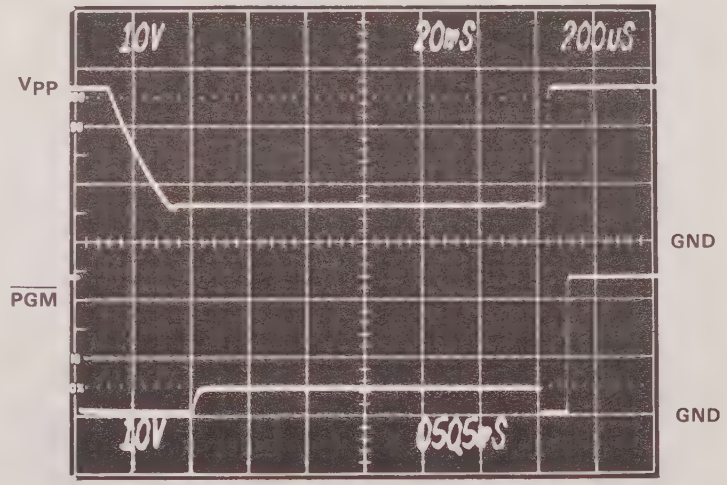
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831			

DATA I/O

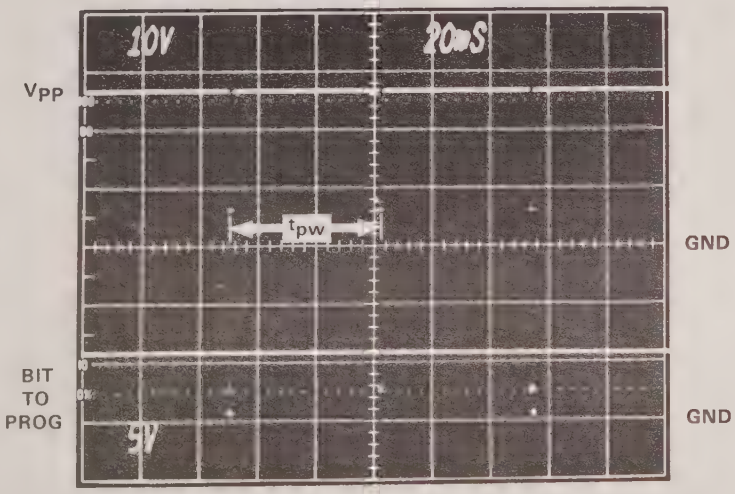
TITLE: TIMING DIAGRAM FAMILY CODES 49, 50		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


10V
20mS
VPP
VPP
VEP
PGM
GND
GND
10V
2

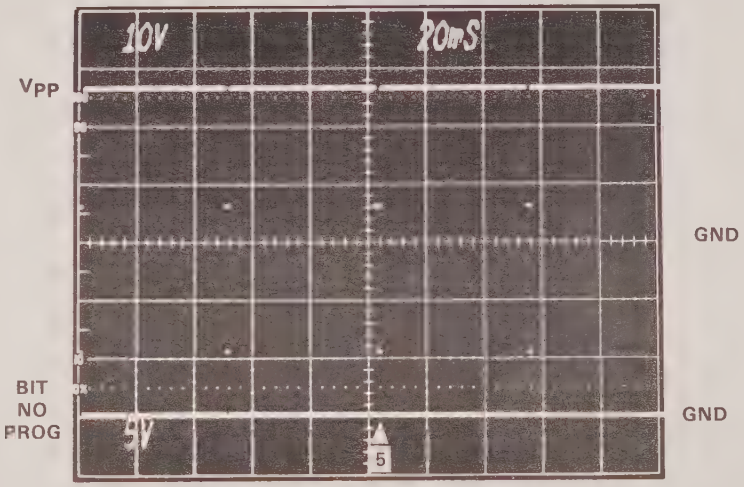
1


10V
20mS
200uS
VPP
PGM
GND
GND
10V
0505mS

2


10V
20mS
VPP
tpw
GND
BIT
TO
PROG
GND
5V

3


10V
20mS
VPP
GND
BIT
NO
PROG
GND
5V
5

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	24.0	25.0	26.0	V	
	V_{PPV}					N.A.
	V_{EP}	21.5	23	24.5	V	
	t_{pw}	49	50	51	ms	
	t_r					N.A.
	t_{ww}	20			μs	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		1		PULSE	
1ST PASS	V_{CC}	4.7	4.8	4.9	V	
VERIFY	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS	V_{CC}	5.1	5.2	5.3	V	
VERIFY	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 51.*
2. *Load RAM with hex 01 for Family 52.*

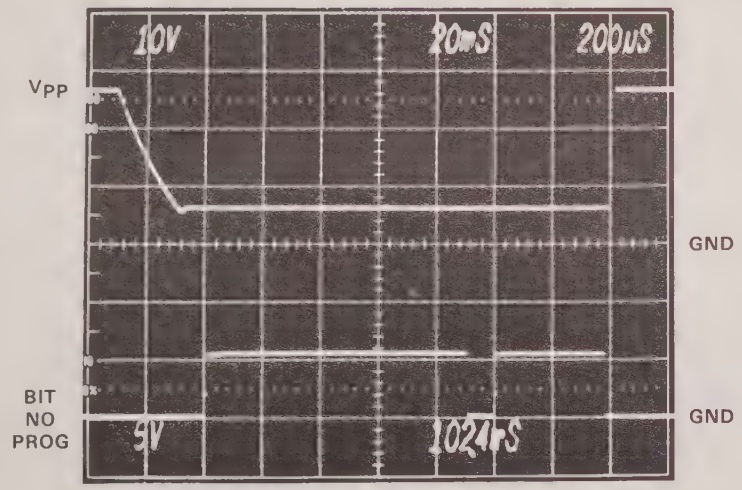
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CJZ	3/84

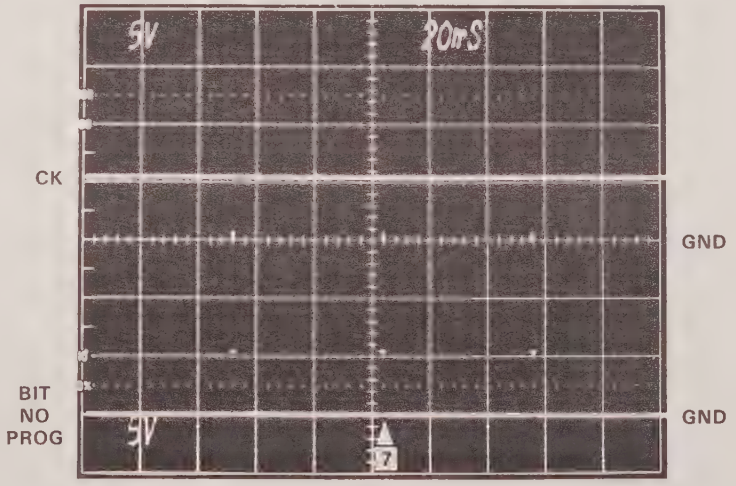
TIMING DIAGRAM

FAMILY CODES 51, 52

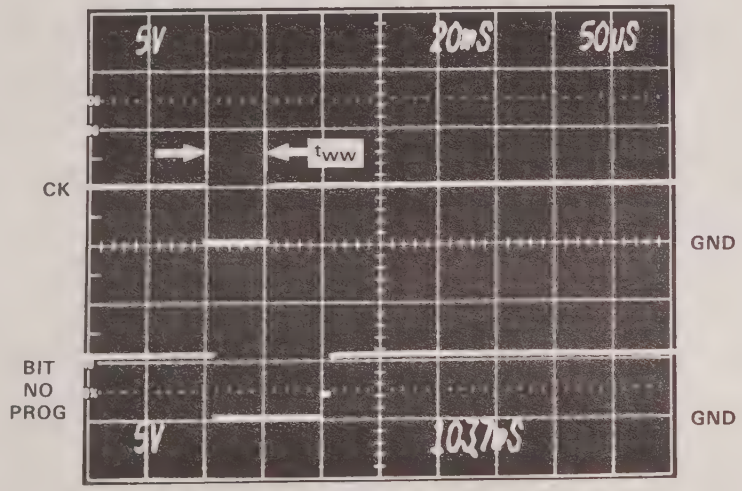
DATA I/O


10V
20mS
200µS
VPP
GND
BIT
NO
PROG
GND
5V
1024mS

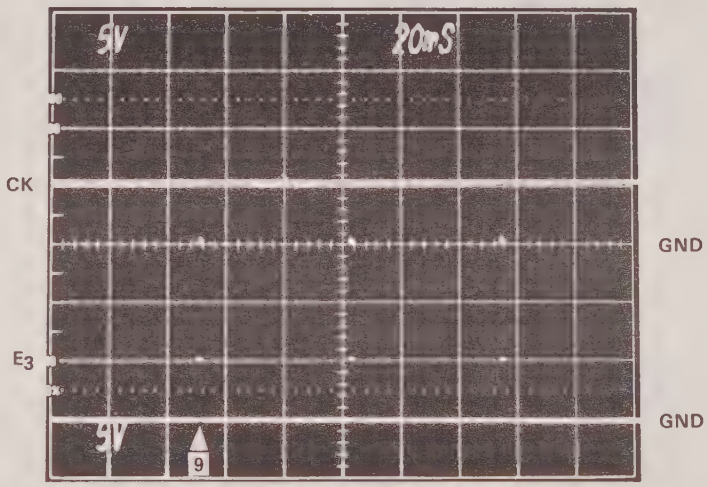
5


5V
20mS
CK
GND
BIT
NO
PROG
GND
5V
7

6


5V
20mS
50µS
CK
tww
GND
BIT
NO
PROG
GND
5V
1037mS

7


5V
20mS
CK
GND
E3
GND
5V
9

8

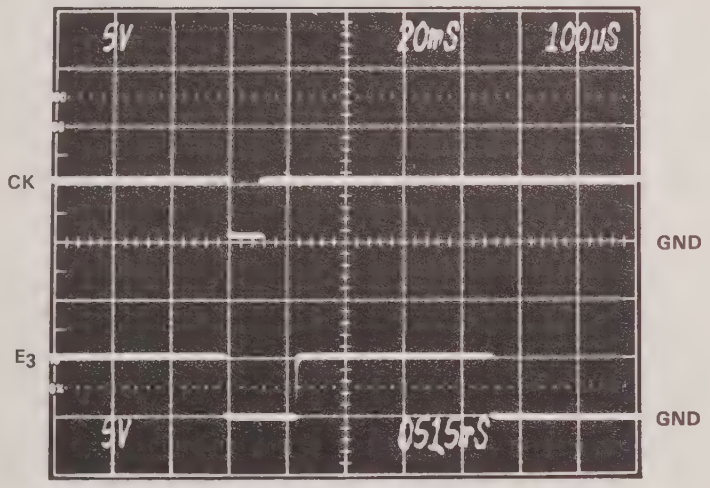
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTS	3/84

TIMING DIAGRAM

FAMILY CODES 51, 52

DATA I/O



9

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10-950-0059

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

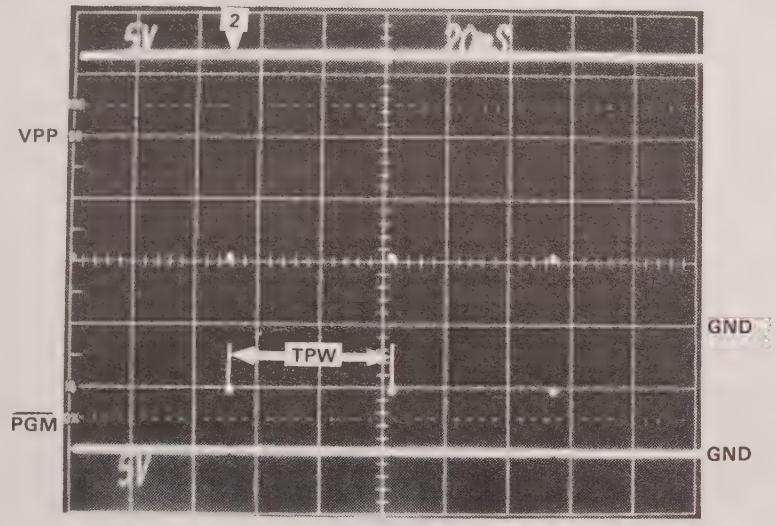
Sheet 3 of 3

TIMING DIAGRAM

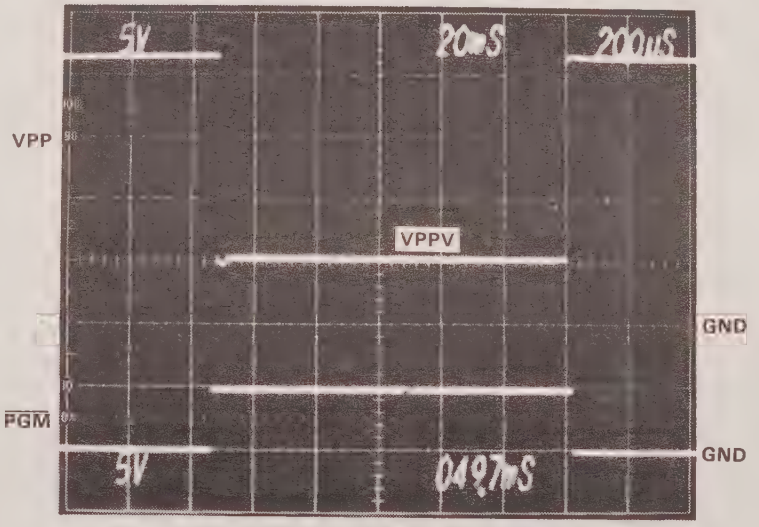
FAMILY CODES 51, 52

DATA I/O

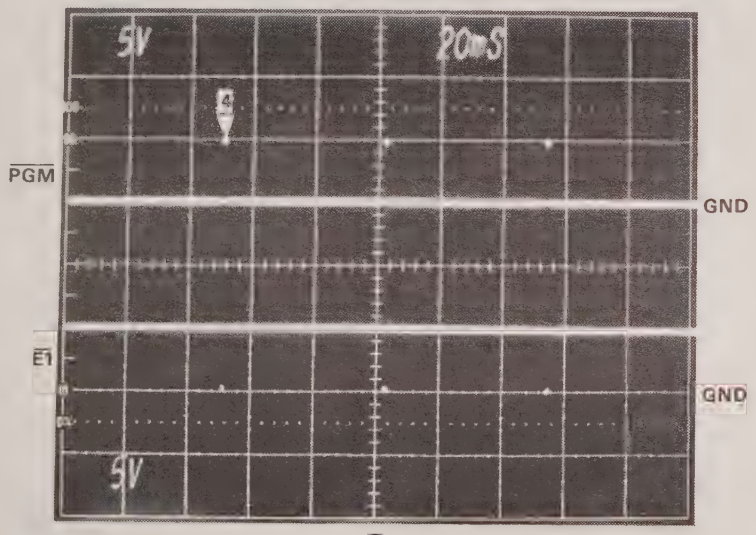
0526/1282



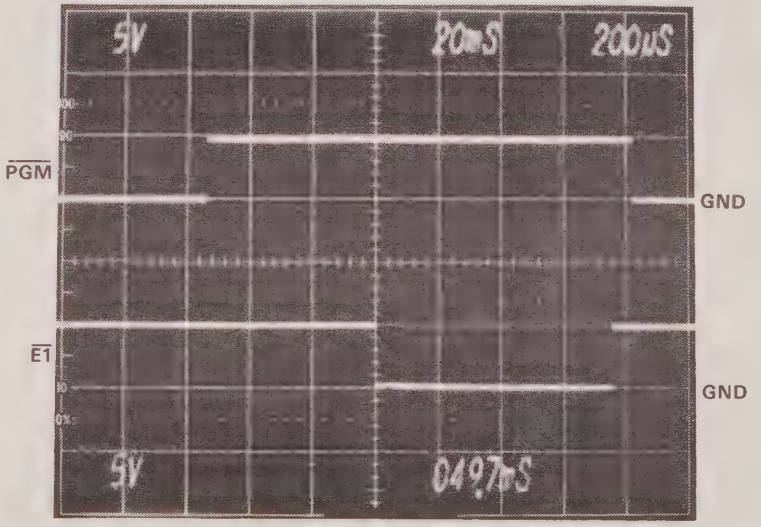
1



2



3



4

10-950-0059

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 53.*
2. *Load RAM with hex 01 for Family 54 and bit-to-prog waveform becomes bit-no-prog waveform.*

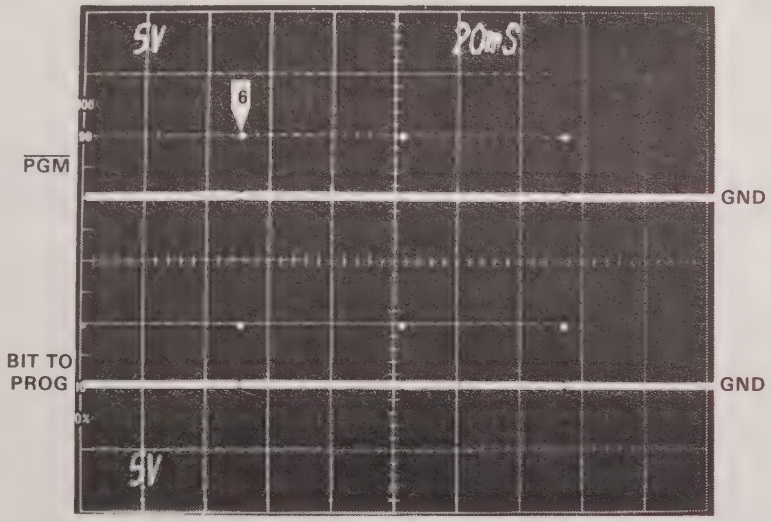
10-950-0059

REVISIONS

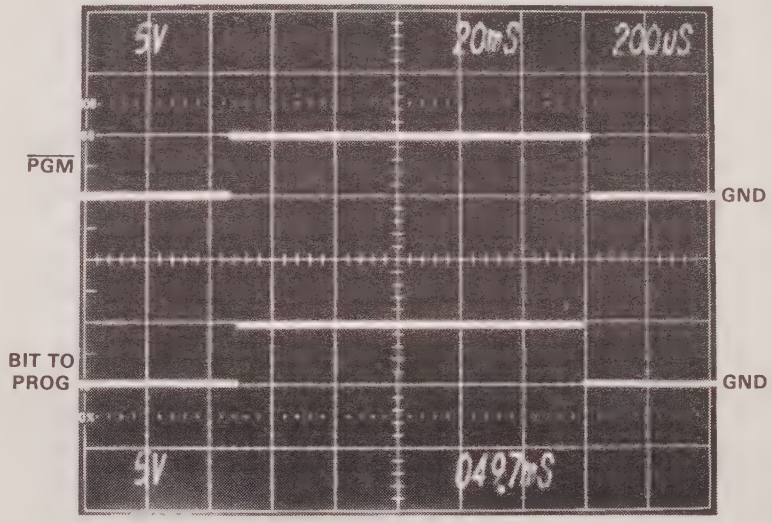
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		ZH	5/83
		ECN #5023		CDZ	3/84

DATA I/O

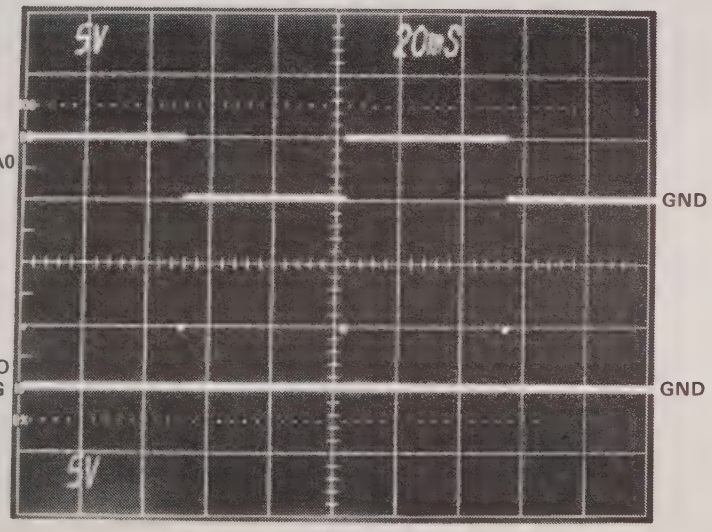
TITLE: TIMING DIAGRAM FAMILY CODES 53, 54		DRAWN BY:
		CHECKED BY: K.H
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


5V
20mS
6
PGM
GND
BIT TO PROG
GND
5V

5


5V
20mS
200uS
PGM
GND
BIT TO PROG
GND
5V
049.7mS

6

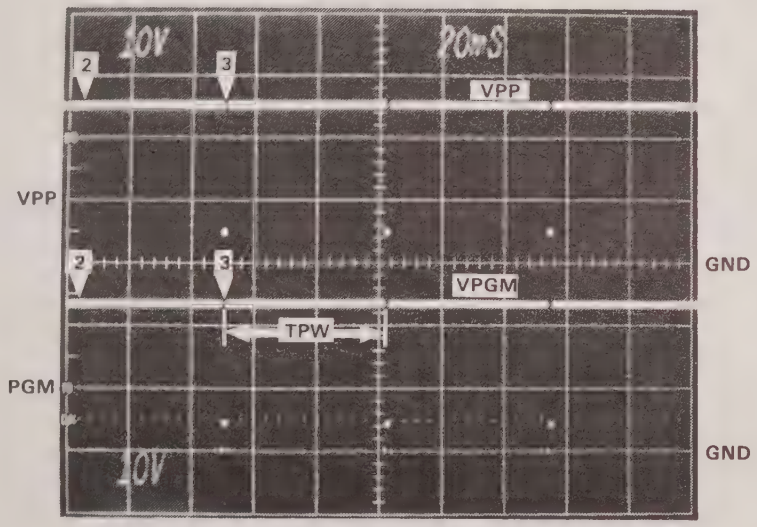

5V
20mS
A0
GND
BIT TO PROG
GND
5V

7

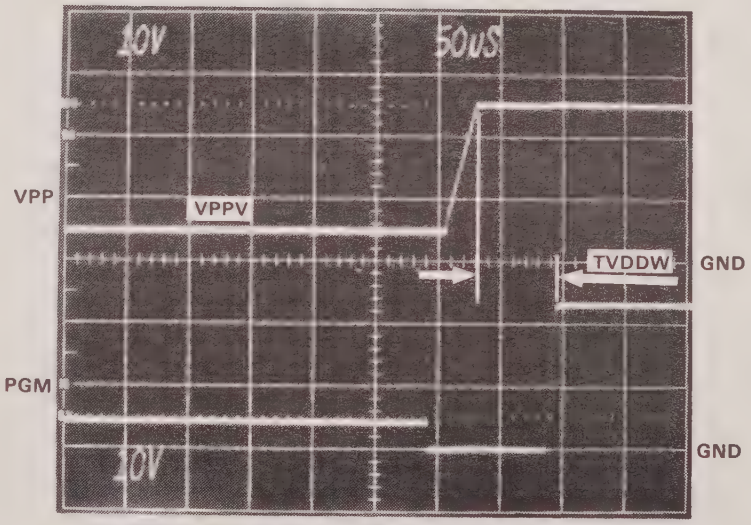
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/83
		ECN #5023		CTZ	3/84

DATA I/O

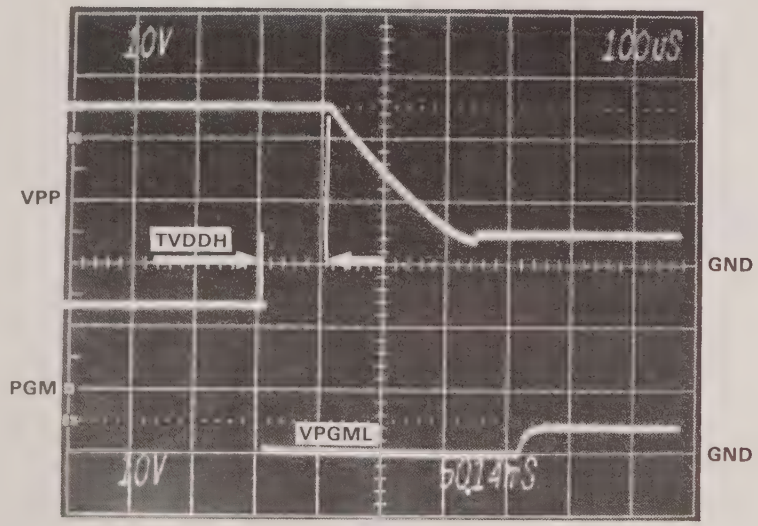
TITLE: TIMING DIAGRAM FAMILY CODES 53, 54		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


10V
20mS
2
3
VPP
VPP
2
3
GND
VPGM
TPW
PGM
GND
10V

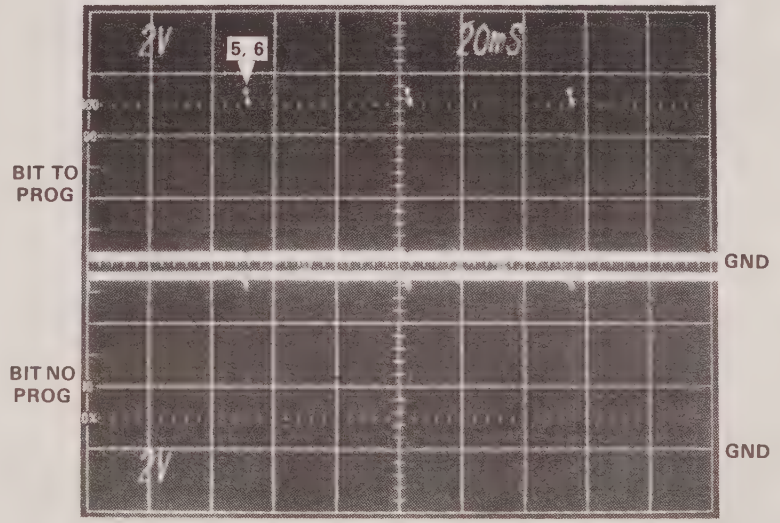
1


10V
50uS
VPP
VPPV
TVDDW
GND
PGM
GND
10V

2


10V
100uS
VPP
TVDDH
GND
PGM
VPGML
GND
10V
5Q14FS

3


2V
5, 6
20mS
BIT TO PROG
GND
BIT NO PROG
GND
2V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.9	5.0	5.1	V	Not shown
	VEA	21.5	23.0	24.5	V	Not shown
	VPP	24.0	25.0	26.0	V	
	VPPV	4.0	5.0	5.2	V	
	VPGM	21.5	23.0	24.5	V	
	VPGML		0	0.3	V	
	TVDDW	17			µs	See note 3
	TVDDH	0			µs	See note 3
	TPW	50		60	ms	
	TWW	17			µs	See note 3
	TAW	17			µs	See note 3
	TWA	17			µs	See note 3
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

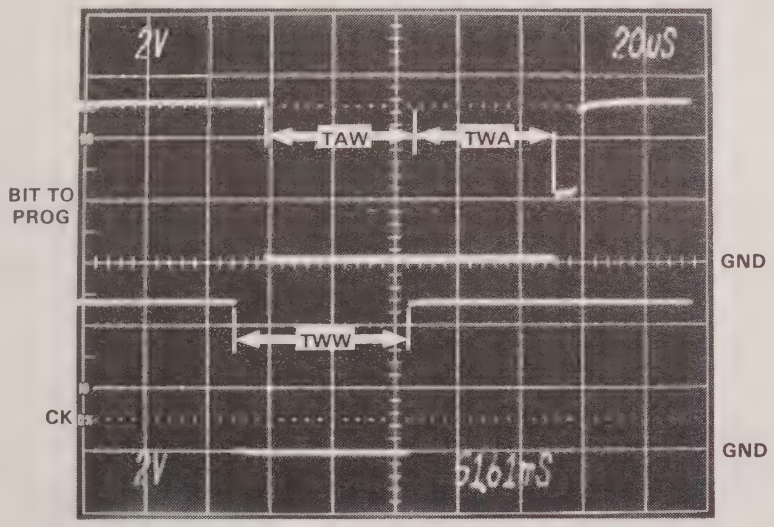
1. *Load RAM with hex FE for Family 55.*
2. *Load RAM with hex 01 for Family 56 and bit-to-prog waveform becomes bit-no-prog waveform and vice versa.*
3. *4TCY = 17 µs @ 3.579545 MHz*

REVISIONS

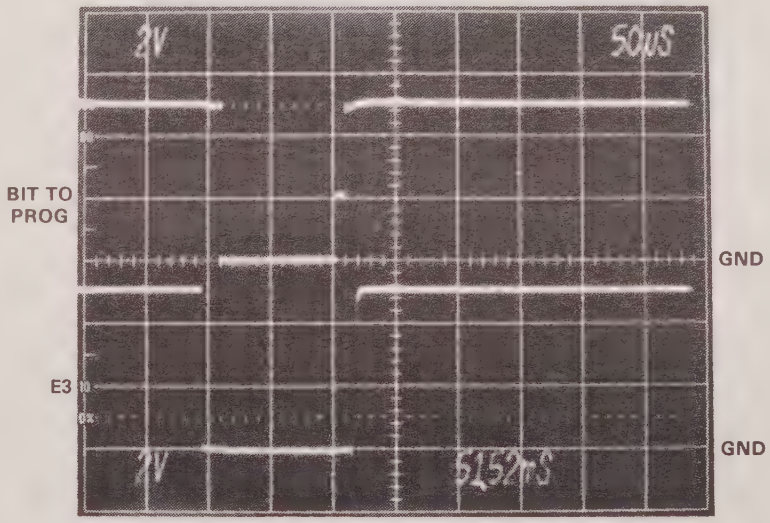
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		[illegible]	5/83
		ECN #5023		CTJ	3/84

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES 55, 56		DRAWN BY:
		CHECKED BY: [illegible]
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


2V
20uS
TAW
TWA
BIT TO PROG
GND
TWW
CK
GND
2V
5161nS

5

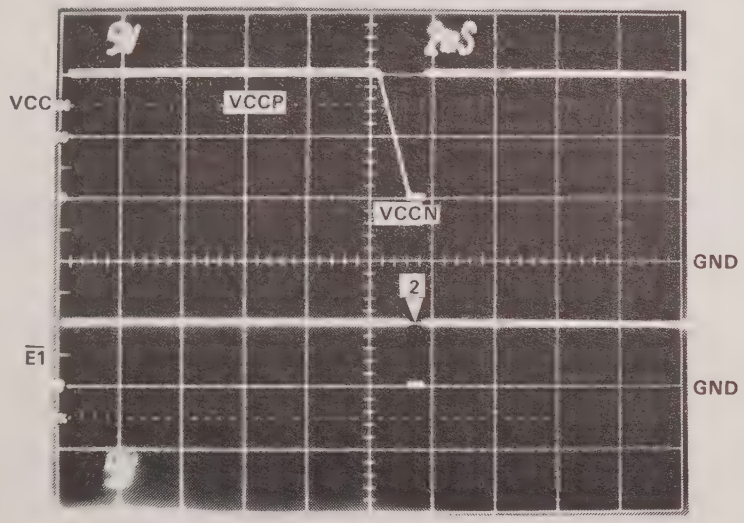

2V
50uS
BIT TO PROG
GND
E3
GND
2V
5152nS

6

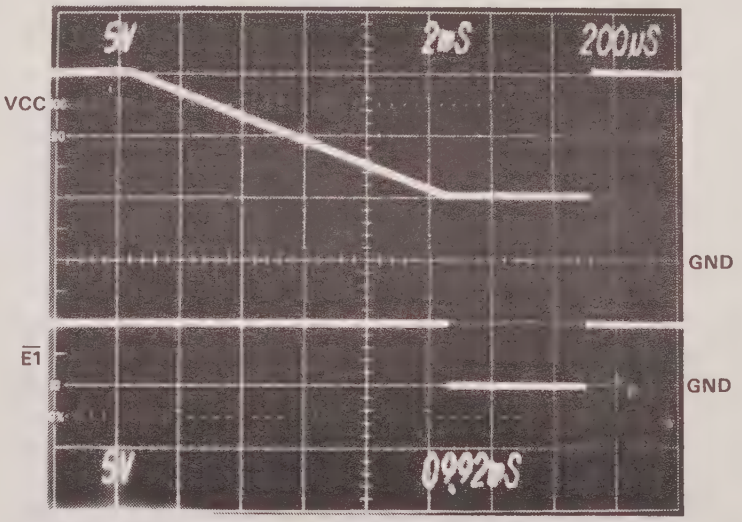
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/83

DATA I/O

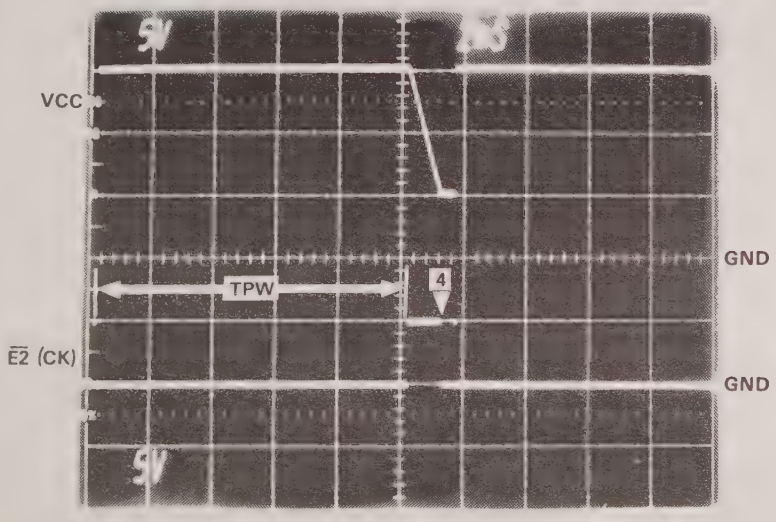
TITLE: TIMING DIAGRAM FAMILY CODES 55, 56		DRAWN BY: CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


VCC
VCCP
VCCN
GND
2
$\overline{E1}$
GND

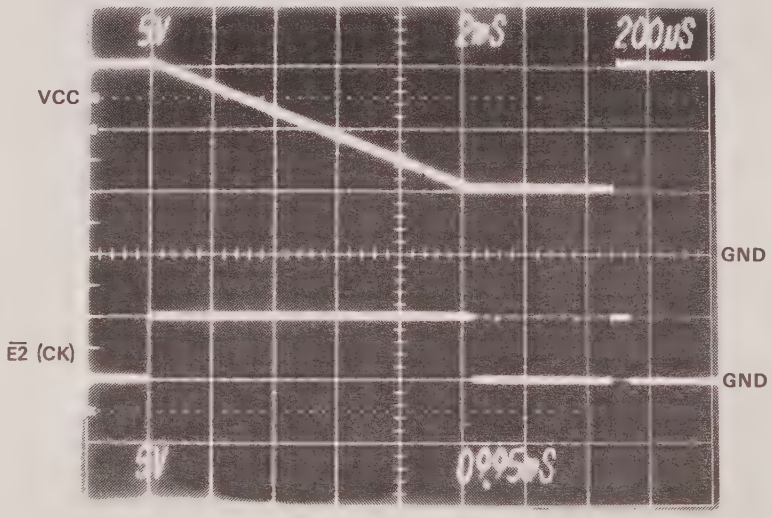
1


VCC
GND
$\overline{E1}$
GND

2


VCC
GND
TPW
4
$\overline{E2}$ (CK)
GND

3


VCC
GND
$\overline{E2}$ (CK)
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	14.0	15.0	16.0	V	
	VCCN	4.0	5.0	6.0	V	
	TPW	9.8	10.0	10.2	ms	
	TR					NA
	TF					NA
	Reject		2		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

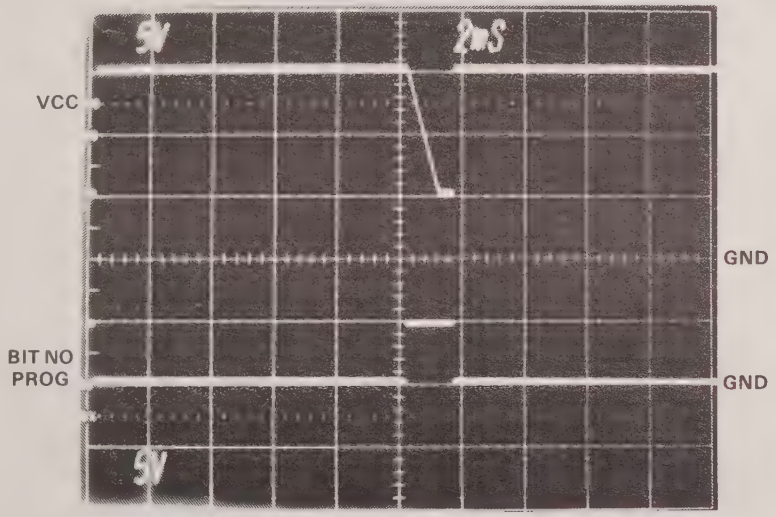
1. *Load RAM with hex FE for Family 57, and bit-no-prog waveform becomes bit-to-prog waveform.*
2. *Load RAM with hex 01 for Family 58.*
3. *Photos 7 and 89 are erase waveforms.*
4. *On the E2(CK) pin, one or two clock pulses may be seen, depending on which pulse location is observed.*
5. *Photo 5 is for Family 58. For Family 57, it is bit-to-prog.*

REVISIONS

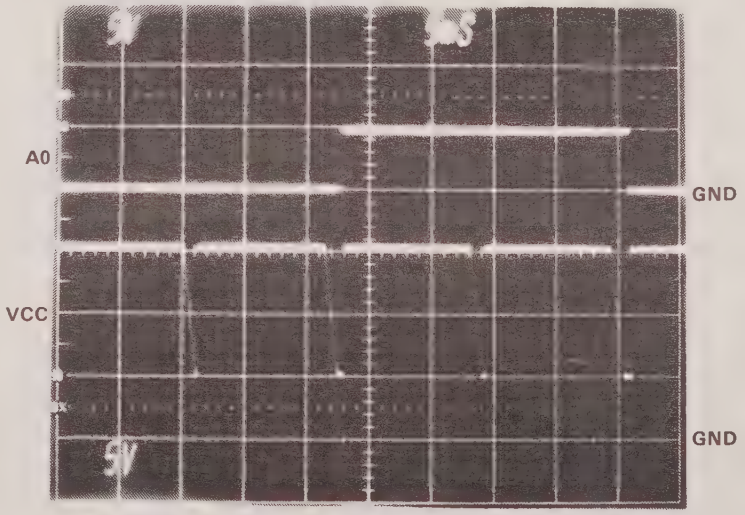
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	2/83
		ECN #5023		CTZ	3/84

DATA I/O

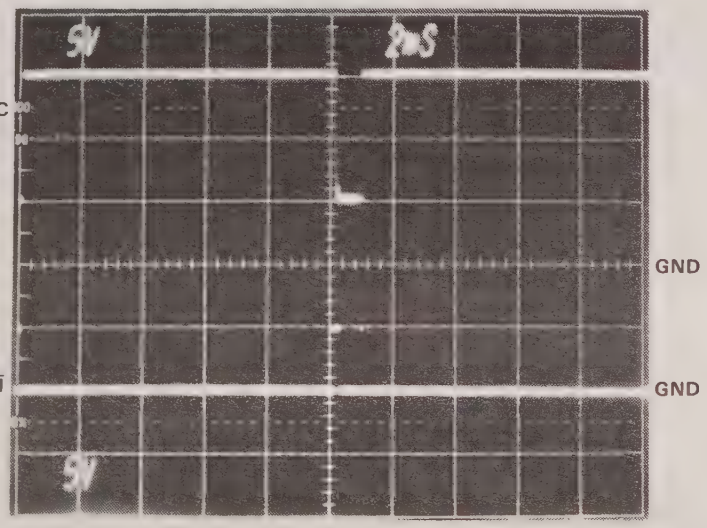
TITLE: TIMING DIAGRAM FAMILY CODES 57, 58		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2


5V
2mS
VCC
GND
BIT NO
PROG
GND
5V

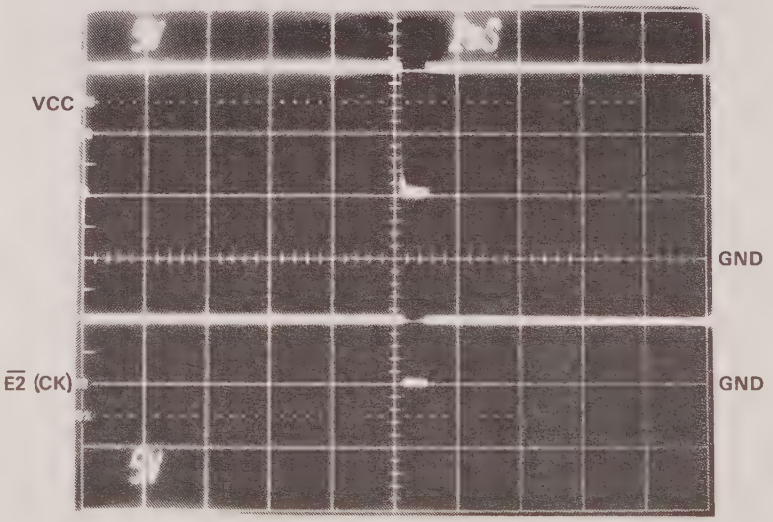
5


5V
2mS
A0
GND
VCC
GND
5V

6


5V
2mS
VCC
GND
E1
GND
5V

7

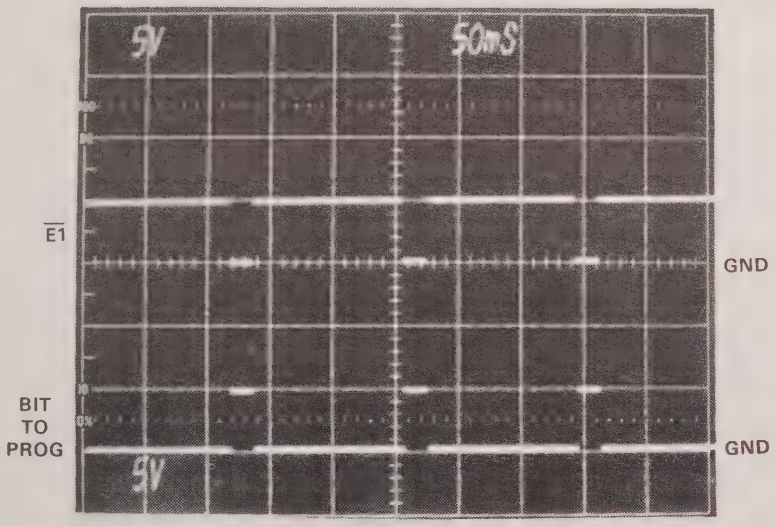

5V
2mS
VCC
GND
E2 (CK)
GND
5V

8

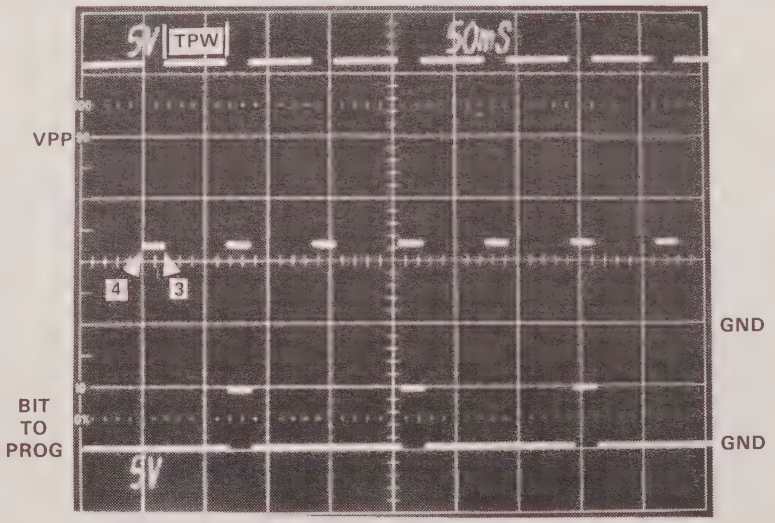
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831			

DATA I/O

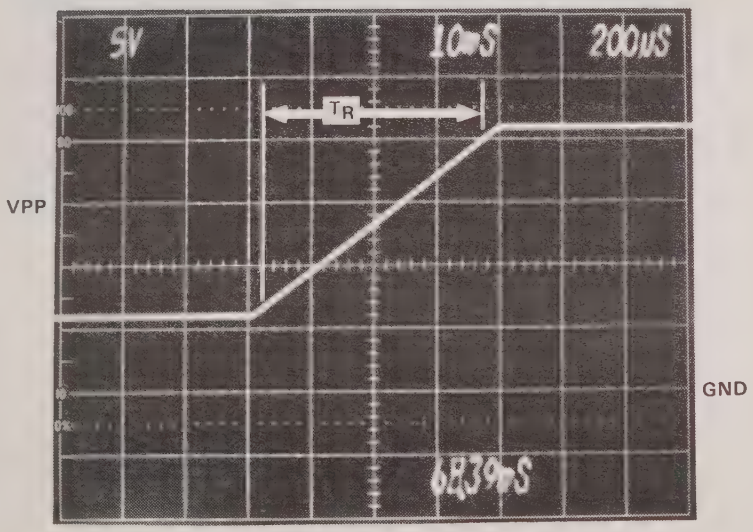
TITLE: TIMING DIAGRAM FAMILY CODES 57, 58		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


5V
50mS
E1
GND
BIT
TO
PROG
GND
5V

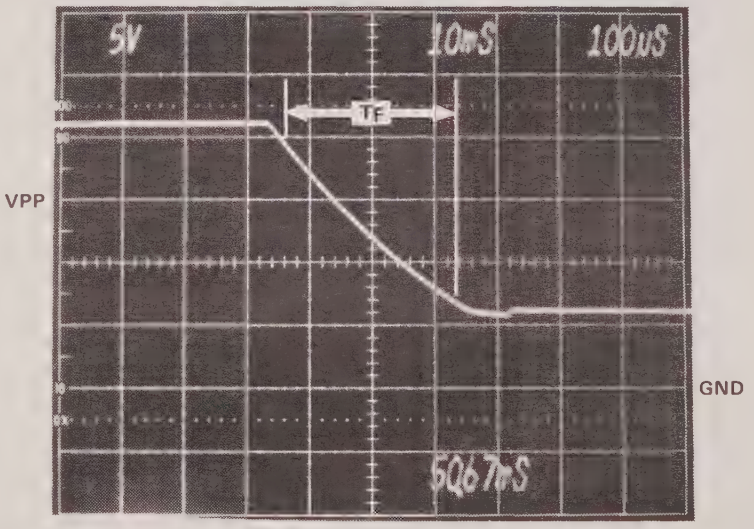
1


5V
TPW
50mS
VPP
4
3
GND
BIT
TO
PROG
GND
5V

2


5V
10mS
200uS
VPP
TR
GND
6.839mS

3


5V
10mS
100uS
VPP
TF
GND
5Q67mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.5	5.8	6.1	V	Not Shown
	VPP	20.0	20.5	21.0	V	
	VPPN	5.7	5.9	6.1	V	
	TPW	45	50	55	ms	
	T_R	50			µs	
	T_F	50			µs	
	Reject		4		Pulses	See note 3
	Overprogram		1		Pulses	See note 3
1ST PASS VERIFY	VCC	4.8	4.9	5.0	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	16.4	17.4	18.4	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	3.4	3.5	3.6	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	19.1	20.1	21.1	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 59.*
2. *Load RAM with hex 01 for Family 60, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Pulse 2 of the 4-pulse string is actually an overprogram pulse.*

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10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		OJZ	11/82
		ECN #4831		LH	5/83
		ECN #5023		CTZ	3/84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 59, 60

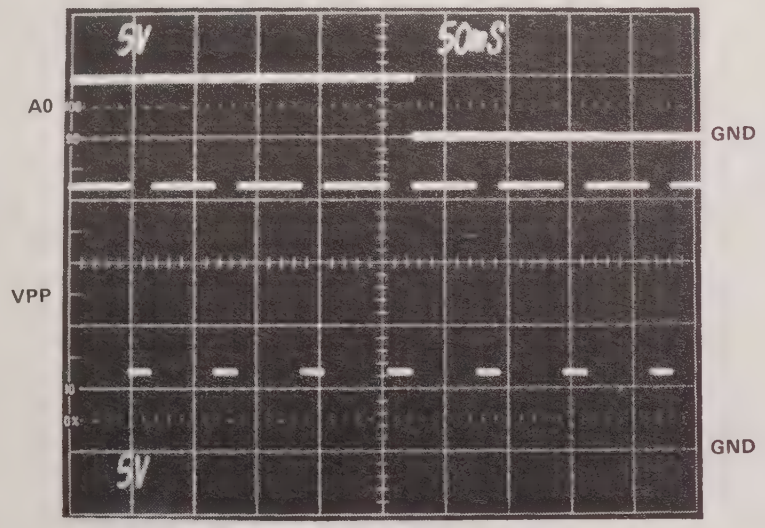
DRAWN BY:

CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2



5

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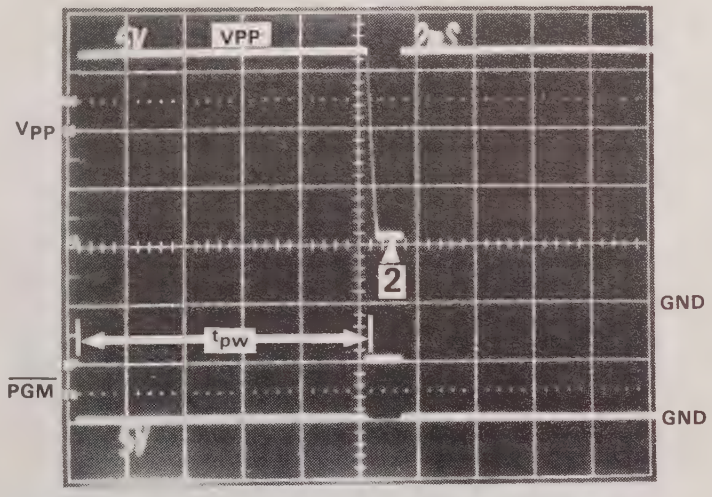
10-950-0059

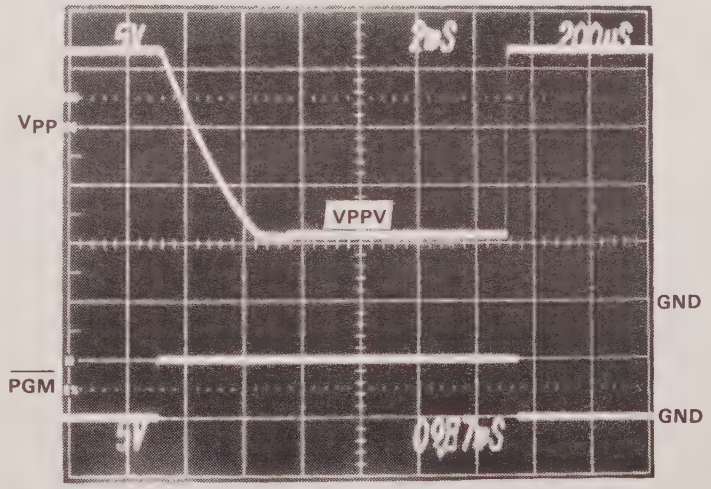
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.Y.g.	11/82
		ECN #4831		JH	5/23

DATA I/O ISSAQUAH, WA

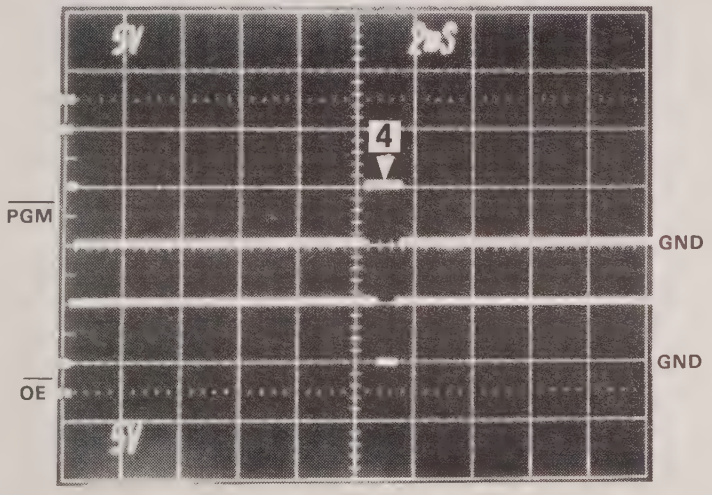
TITLE: TIMING DIAGRAM FAMILY CODES 59, 60		DRAWN BY:
		CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
VPP
2mS
VPP
2
GND
tpw
PGM
GND
5V

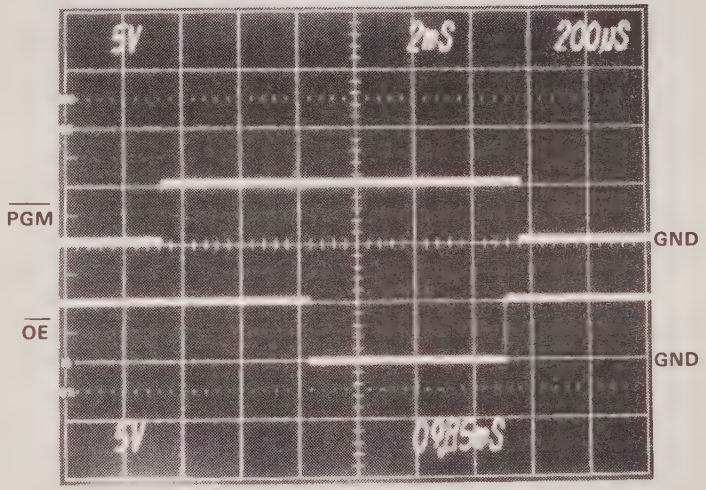
1


5V
2mS
200uS
VPP
VPPV
GND
PGM
GND
5V

2


5V
2mS
4
PGM
GND
OE
GND
5V

3


5V
2mS
200uS
PGM
GND
OE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	20.5	21.0	21.5	V	
	V_{PPV}	4.75	5.0	5.25	V	
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 63.*
2. *Photos 7 and 8 are for Pinout 24.*

REVISIONS

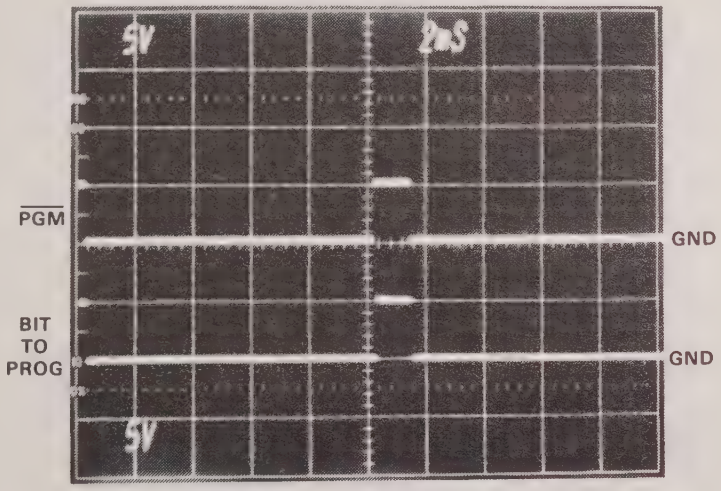
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

Sheet 1 of 2

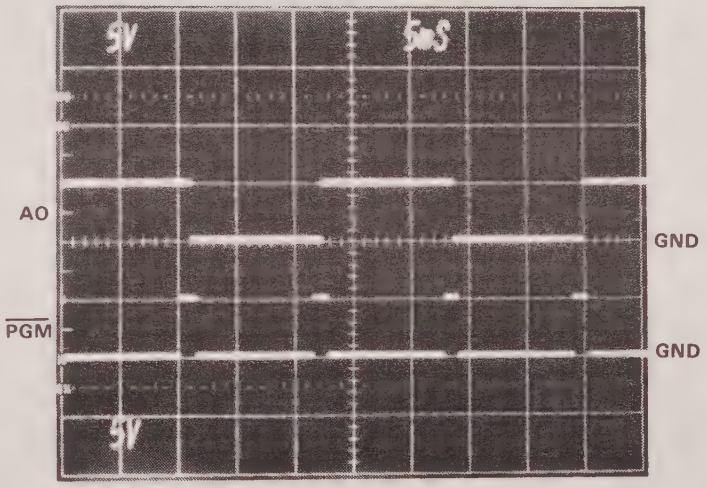
TIMING DIAGRAM

FAMILY CODES 63, 64

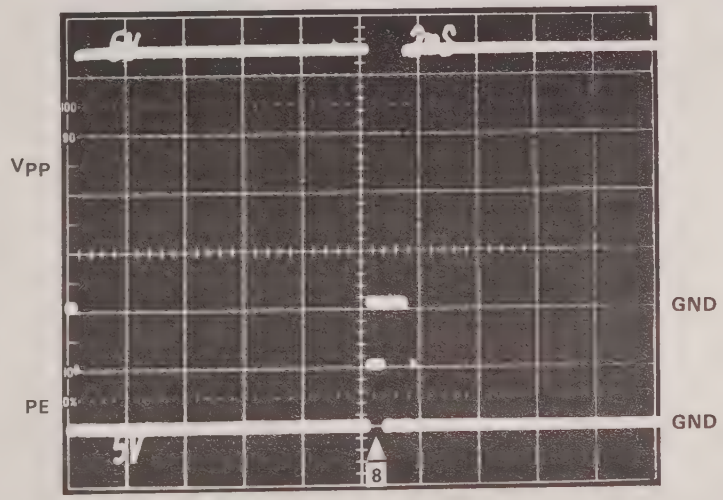
DATA I/O


5V
2mS
PGM
GND
BIT
TO
PROG
GND
5V

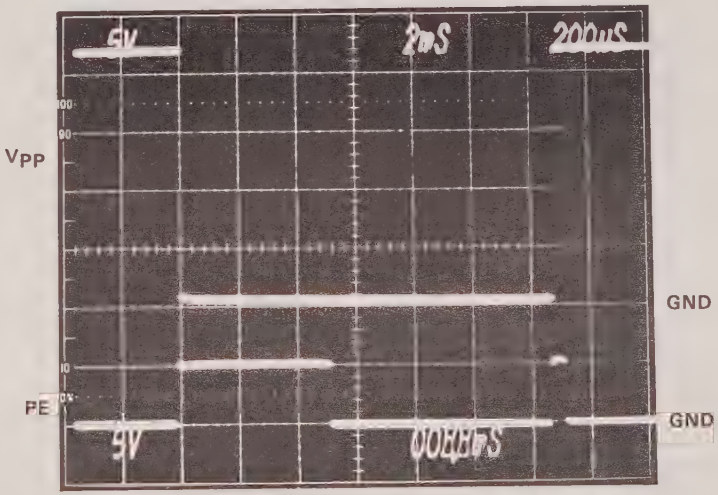
5


5V
5mS
AO
GND
PGM
GND
5V

6


5V
2mS
VPP
GND
PE
GND
5V
8

7


5V
2mS
200uS
VPP
GND
PE
GND
5V

8

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10-950-0059

REVISIONS

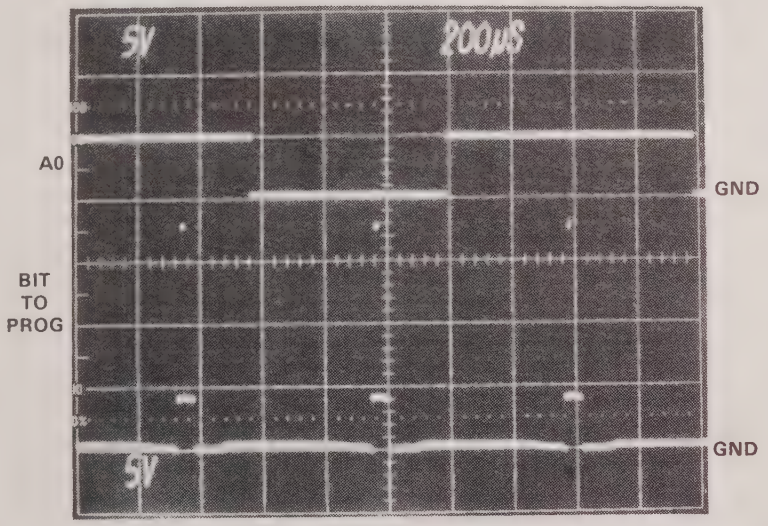
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

Sheet 2 of 2

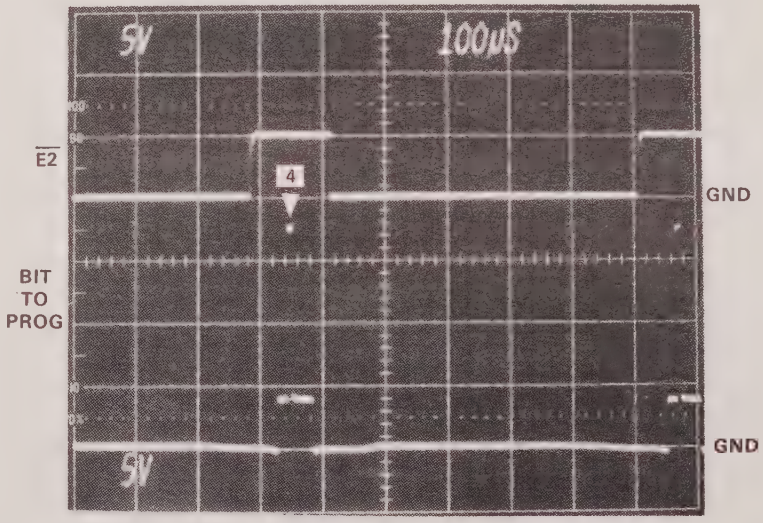
TIMING DIAGRAM

FAMILY CODES 63, 64

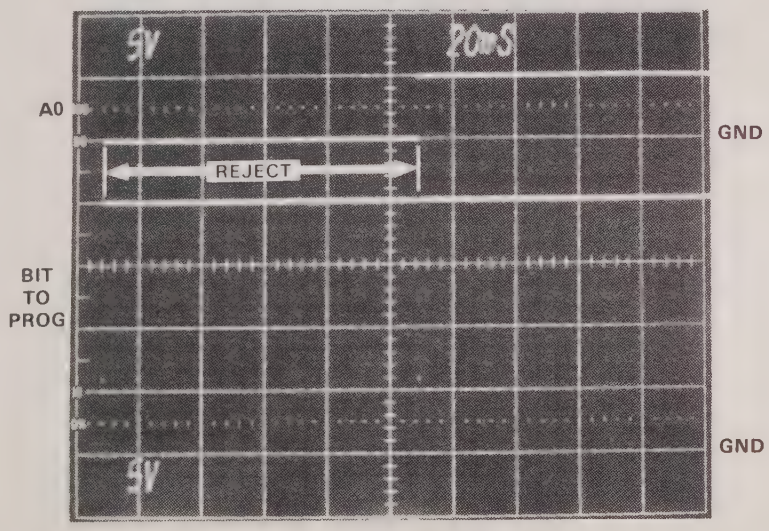
DATA I/O


5V
200µS
A0
GND
BIT
TO
PROG
GND
5V

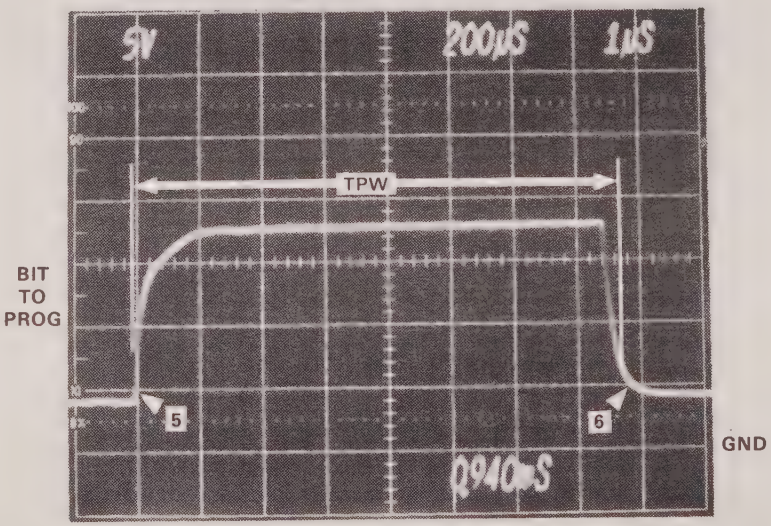
1


5V
100µS
E2
4
GND
BIT
TO
PROG
GND
5V

2


5V
20mS
A0
GND
REJECT
BIT
TO
PROG
GND
5V

3


5V
200µS
1µS
TPW
BIT
TO
PROG
5
6
GND
Q940mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not Shown
	VOP					NA
	VOP	19.0	19.5	20.0	V	
	TPW	7.1	7.5	7.9	µs	See Note 2
	TR	0.16		1.1	µs	
	TF	0.16		1.1	µs	
	Overprogram		1		Pulses	
	Reject		10,000		Pulses	See Note 3
	Duty Cycle	70			%	
1ST PASS VERIFY	VCC	4.5	4.6	4.7	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.5	26.0	26.5	V	701-1655/TP4
	Low Load	25.5	26.0	26.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.5	6.6	6.7	V	
	VREF	4.4	4.5	4.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.7	7.2	7.7	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 65.*
2. *Load RAM with hex 01 for Family 66.*
3. *Measurement taken at 9V point of 01 with a 200 Ω load.*
4. *10,000 pulses equals 100 ms, as shown in photo 3.*
5. *Do not use a wirewound load resistor.*

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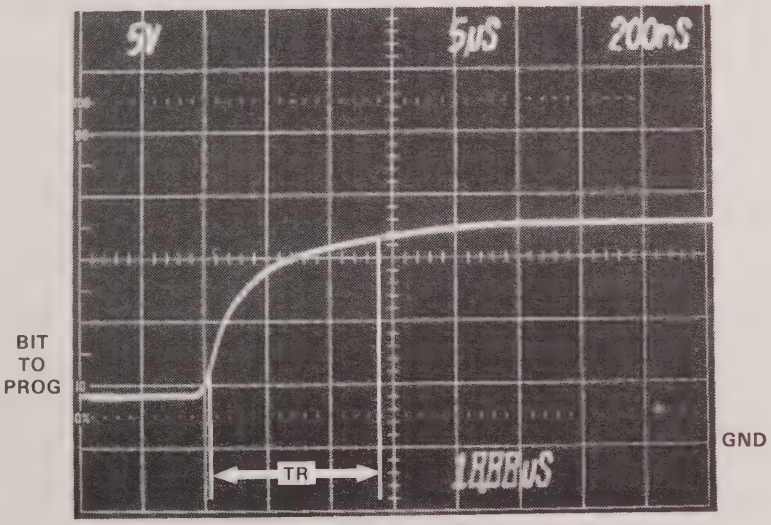
10-950-0059

REVISIONS

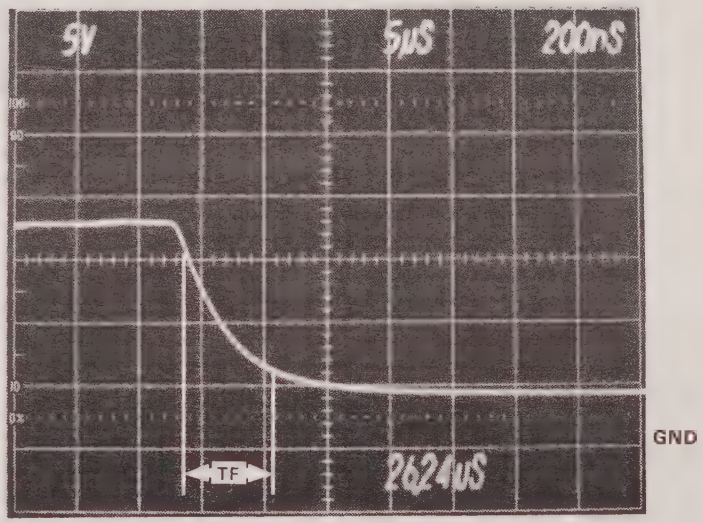
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		22	5/23
		ECN #5023		C73	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM FAMILY CODES 65, 66	DRAWN BY: PAP	
	CHECKED BY: ZH	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


5V
5µS
200nS
BIT
TO
PROG
GND
TR
1.888uS

5

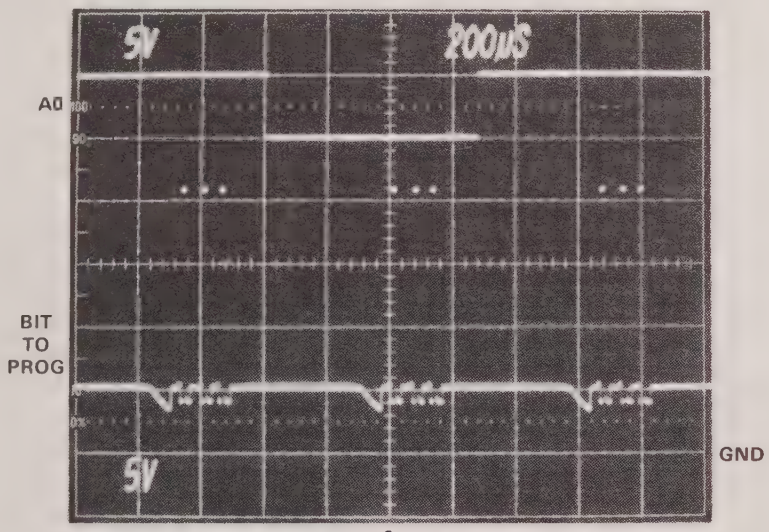

5V
5µS
200nS
GND
TF
2.624uS

6

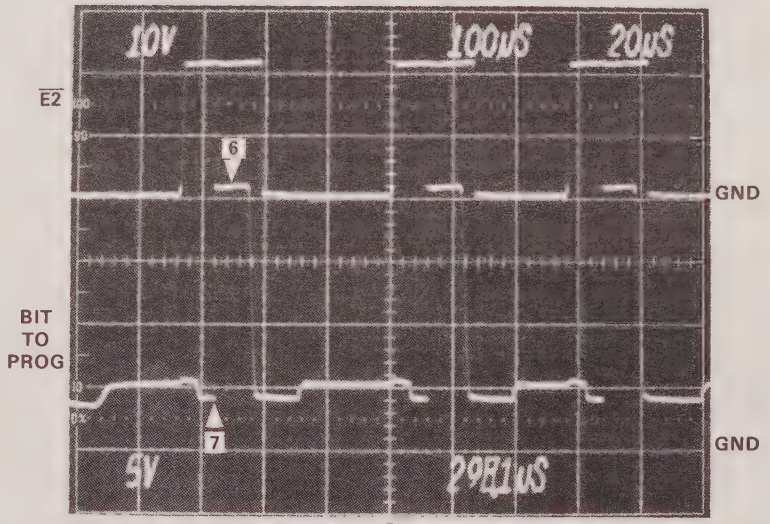
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/8

DATA I/O ISSAQUAH, WA

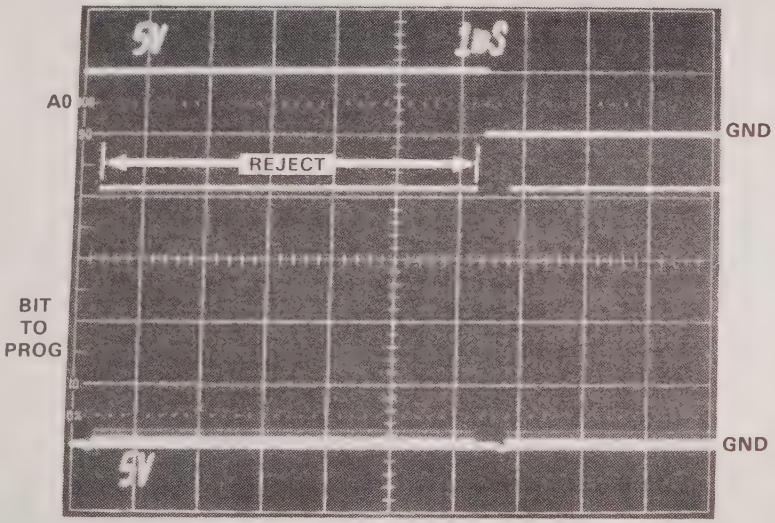
TITLE: TIMING DIAGRAM FAMILY CODES 65, 66			DRAWN BY: PAP
			CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2


5V
200µS
A0
BIT
TO
PROG
GND
5V

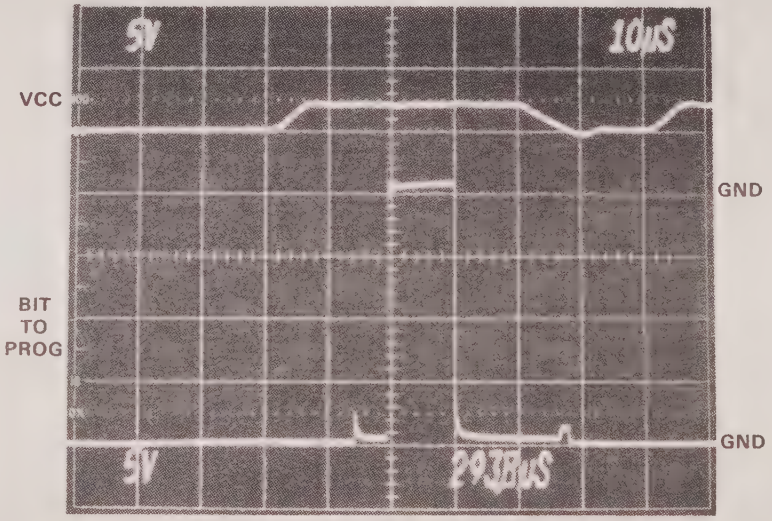
1


10V
100µS
20µS
E2
6
GND
BIT
TO
PROG
7
GND
5V
29R1µS

2


5V
1µS
A0
GND
REJECT
BIT
TO
PROG
GND
5V

3


5V
10µS
VCC
GND
BIT
TO
PROG
GND
5V
293µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	6.7	7.0	7.5	V	
	VPP	20.0	20.0	22.0	V	
	VOP	20.0	20.0	22.0	V	
	TPW	10.0	11.0	12.0	µs	See Note 2
	TR			2.0	µs	
	TF			2.0	µs	
	Overprogram		2		Pulses	
	Reject		100		Pulses	See Note 3
	Duty Cycle	15	20	25	%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.0	26.0	27.0	V	701-1655/TP4
	Low Load	25.0	26.0	27.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.9	7.0	7.1	V	
	VREF	3.9	4.0	4.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	5.6	6.6	7.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 67.*
2. *Load RAM with hex 01 for Family 68.*
3. *Measurement taken at 15V point of 01 with a 200 Ω load.*
4. *100 pulses equals 6 ms, as shown in photo 3.*
5. *V_{CC} loaded with a 330 Ω resistor, as shown in photo 5.*
6. *Do not use a wirewound load resistor.*
7. *01 is loaded with a 200 Ω resistor, as shown in photos 3-7.*

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10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CTJ	11/82
		ECN #4831			5/83
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 67, 68

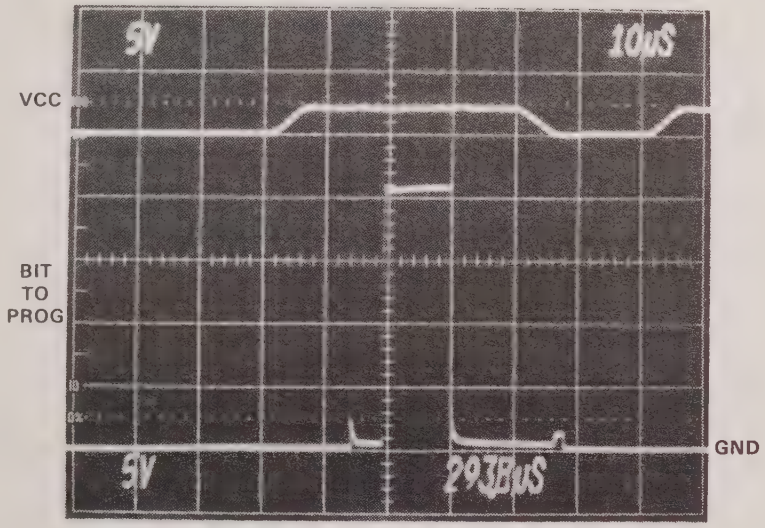
DRAWN BY: BG / PP

CHECKED BY:

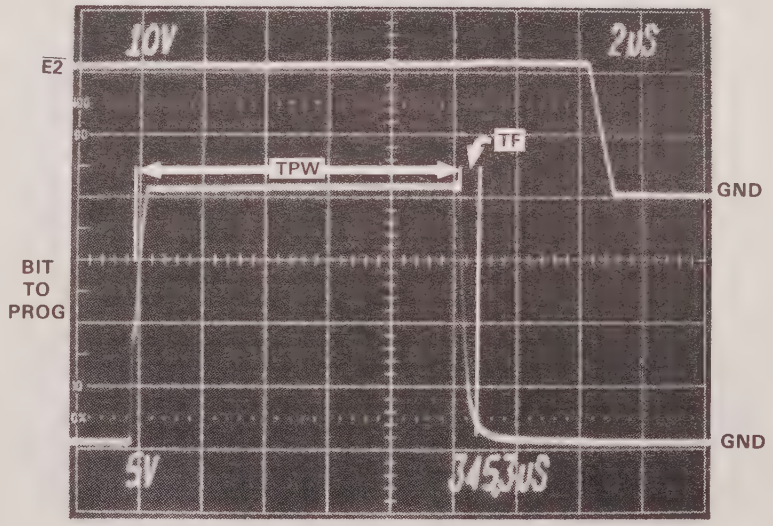
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

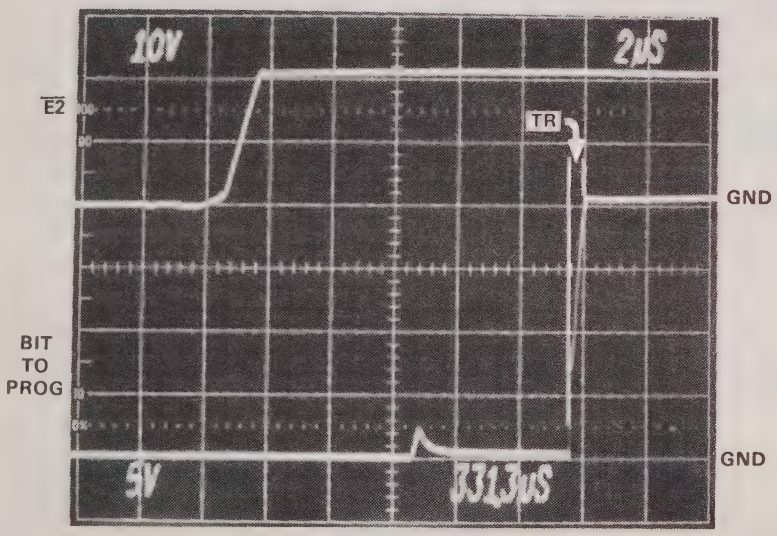
SHEET 1/2


5V
10uS
VCC
BIT
TO
PROG
GND
5V
293uS

5


10V
2uS
E2
TPW
TF
GND
BIT
TO
PROG
GND
5V
345.3uS

6


10V
2uS
E2
TR
GND
BIT
TO
PROG
GND
5V
331.3uS

7

B-123
10-950-0059

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.S.	11/82
		ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 67, 68

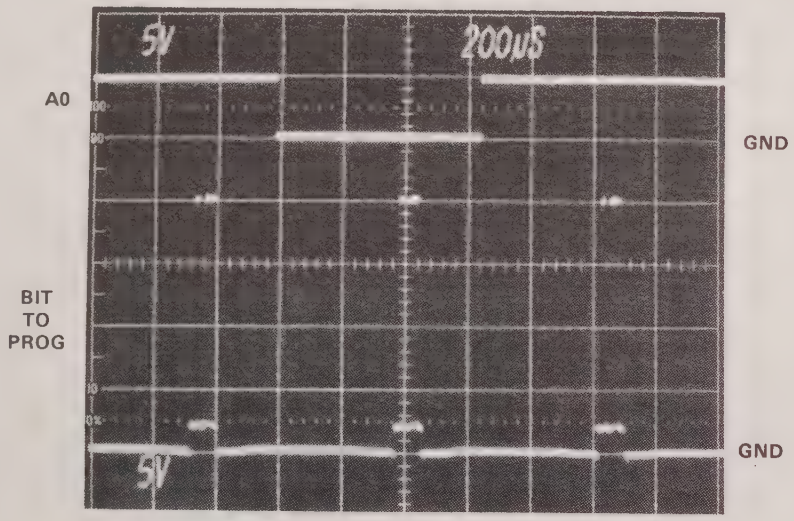
DRAWN BY: BG/PAP

CHECKED BY:

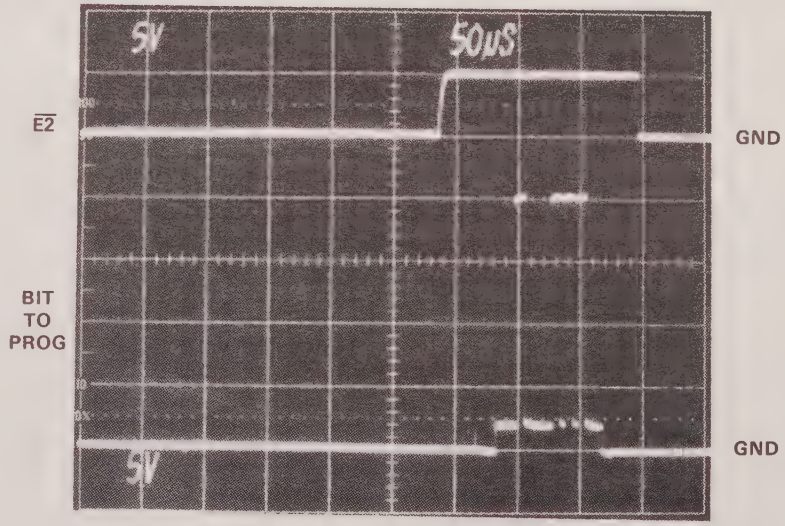
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

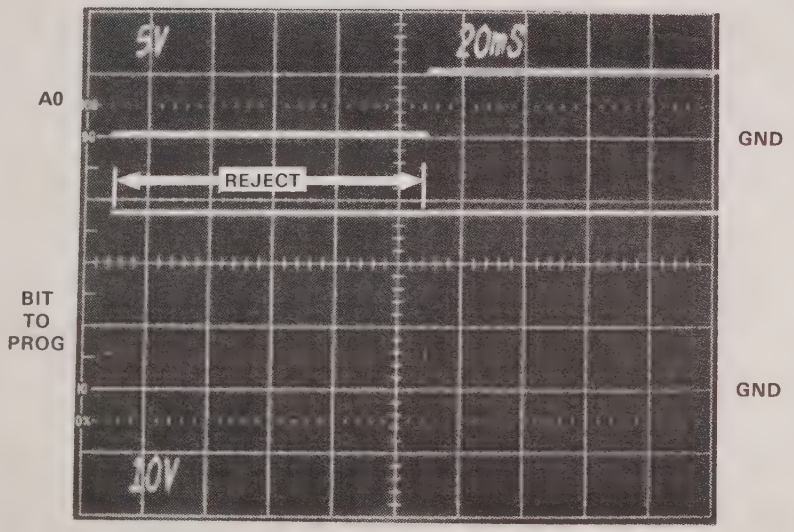
SHEET 2/2


5V
200µS
A0
GND
BIT
TO
PROG
GND
5V

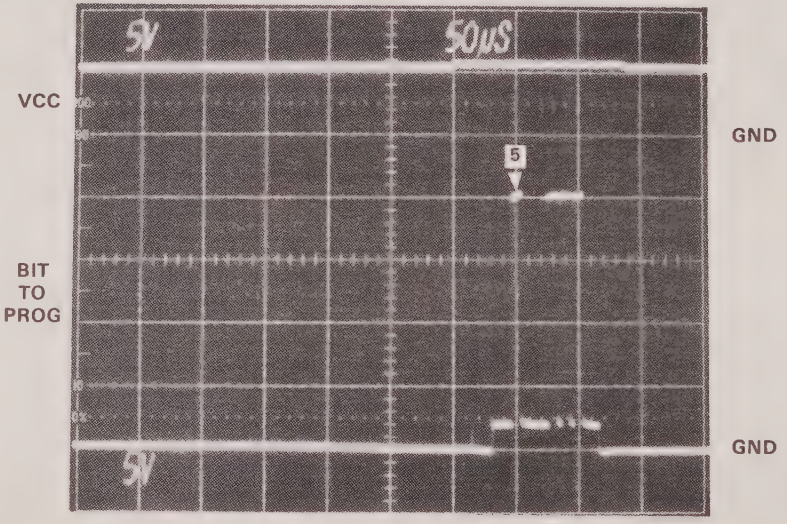
1


5V
50µS
$\overline{E2}$
GND
BIT
TO
PROG
GND
5V

2


5V
20mS
A0
GND
REJECT
BIT
TO
PROG
GND
10V

3


5V
50µS
VCC
GND
5
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.00	5.20	5.40	V	
	VPP					NA
	VOP	27.5	28.0	28.5	V	
	TPW	7.0	7.5	8.0	µs	See Note 2
	T_R	0.21		0.30	µs	
	T_F	0.21		0.30	µs	
	Overprogram		4		Pulses	
	Reject		10,000		Pulses	See Note 3
	Duty Cycle	70	75	80	%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.0	26.0	27.0	V	701-1655/TP4
	Low Load	25.0	26.0	27.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	6.9	7.0	7.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	8.6	9.6	10.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 69.*
2. *Load RAM with hex 01 for Family 70.*
3. *Measurement taken at 10V point of 01 with a 100 Ω load.*
4. *10,000 pulses equals 100 ms, as shown in photo 3.*
5. *Do not use a wirewound load resistor.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.F.J.	11/82
		ECN #4831		[illegible]	[illegible]
		ECN #5023		C.F.J.	3/84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 69, 70

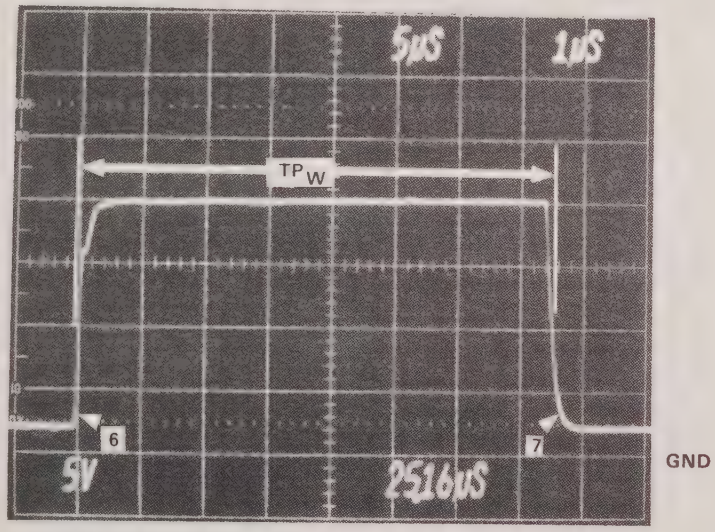
DRAWN BY:

CHECKED BY:

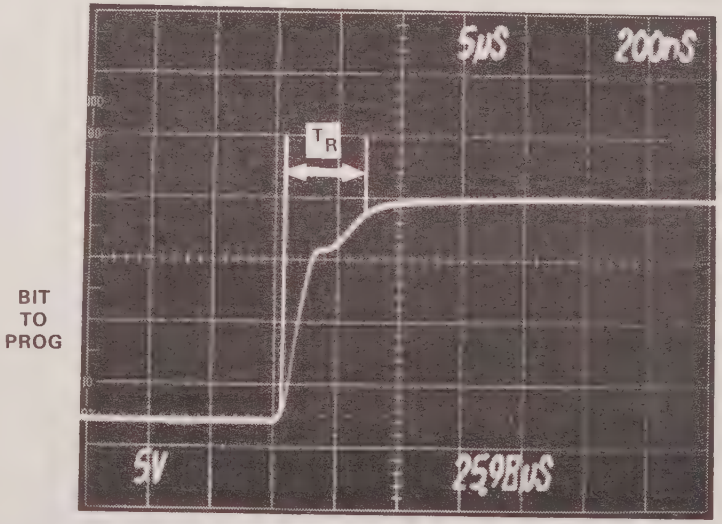
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

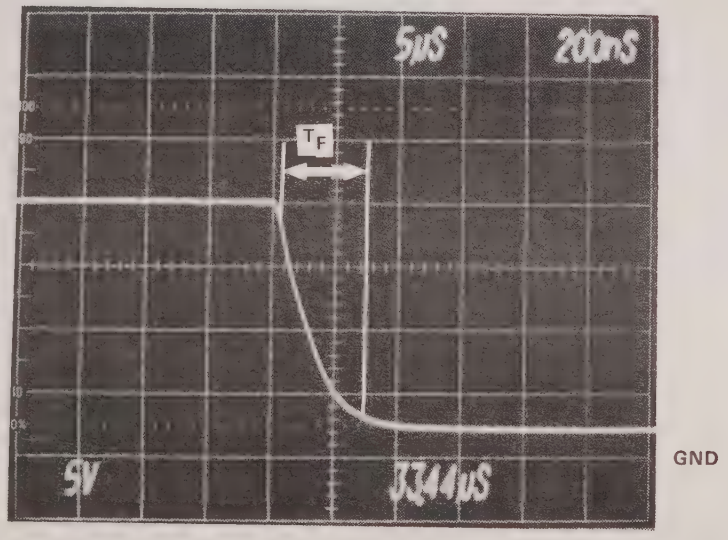
SHEET 1/2


5uS
1uS
TP W
BIT
TO
PROG
6
7
5V
2516uS
GND

5


5uS
200nS
T R
BIT
TO
PROG
5V
2598uS
GND

6


5uS
200nS
T F
BIT
TO
PROG
5V
3344uS
GND

7

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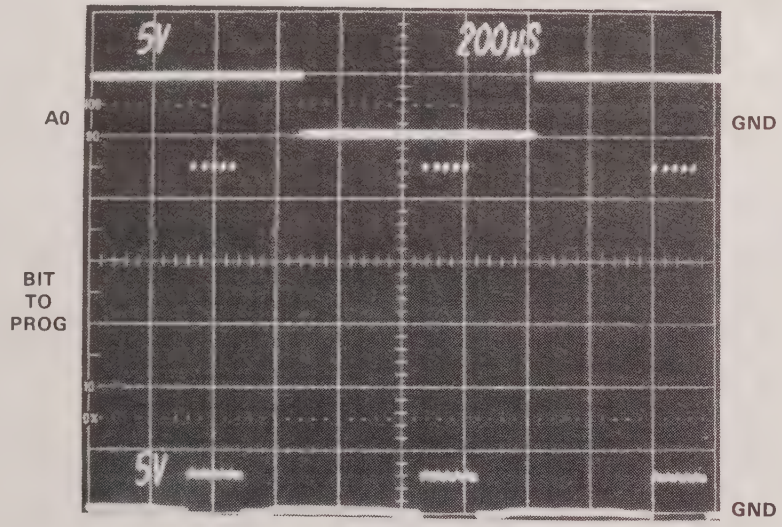
10-950-0059

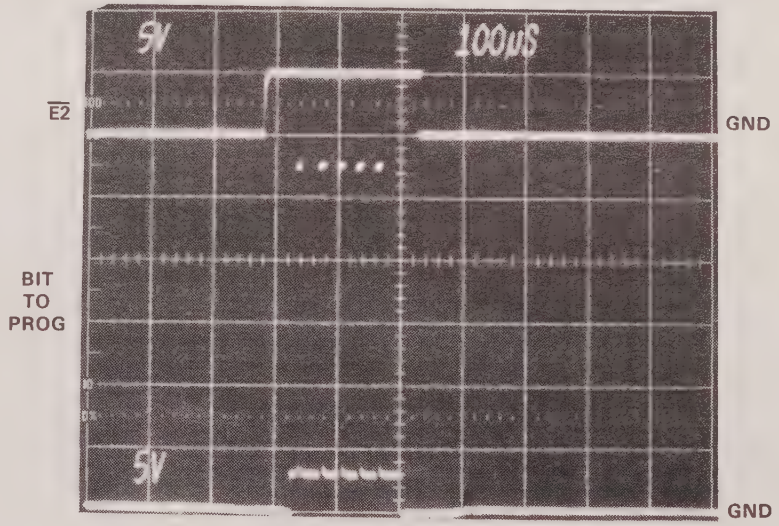
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.T.Z.	11/82
		ECN #4831		JF	5/83

DATA I/O ISSAQUAH, WA

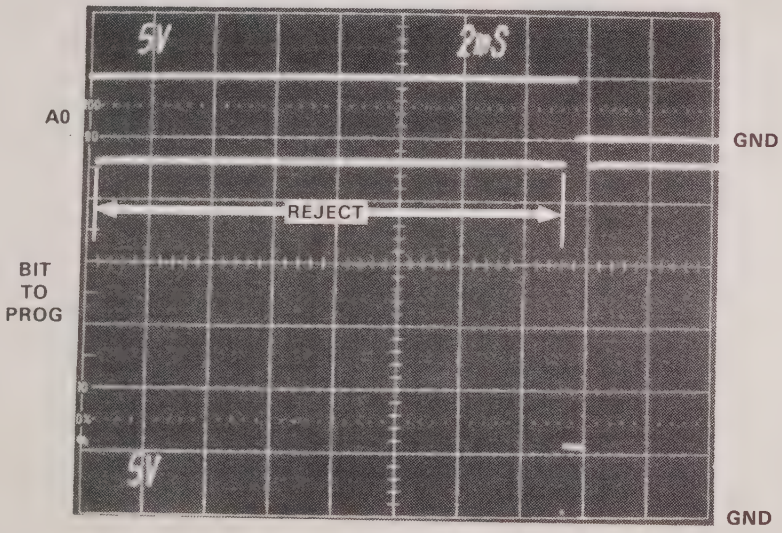
TITLE: TIMING DIAGRAM FAMILY CODES 69, 70			DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059	
SCALE			SHEET 2/2


5V
200µS
A0
GND
BIT
TO
PROG
5V
GND

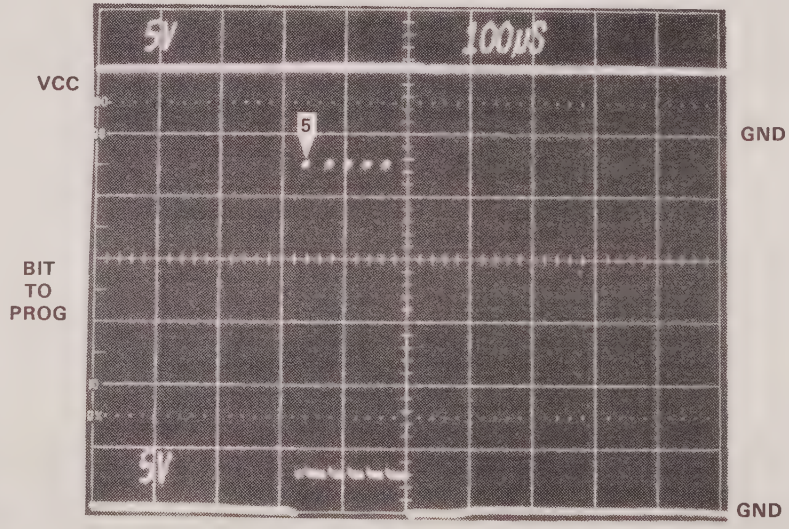
1


5V
100µS
E2
GND
BIT
TO
PROG
5V
GND

2


5V
2mS
A0
GND
REJECT
BIT
TO
PROG
5V
GND

3


5V
100µS
VCC
5
GND
BIT
TO
PROG
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.90	5.10	5.30	V	
	VPP					NA
	VOP	27.5	28.0	28.5	V	
	TPW	7.0	7.5	8.0	µs	See Note 2
	T_R	0.28			µs	
	T_F	0.28			µs	
	Overprogram		4		Pulses	
	Reject		1,000		Pulses	See Note 3
	Duty Cycle	70			%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.5	26.0	26.5	V	701-1655/TP4
	Low Load	25.5	26.0	26.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	3.9	4.0	4.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.2	6.7	7.2	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 71*
2. *Load RAM with hex 01 for Family 72.*
3. *Measurement taken at 15V point of 01 with 1 150 Ω load.*
4. *1,000 pulses equals 10 ms, as shown in photo 3.*
5. *Do not use a wirewound load resistor.*

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10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		KH	4/85
		ECN #5023		CTZ	3/87

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 71, 72

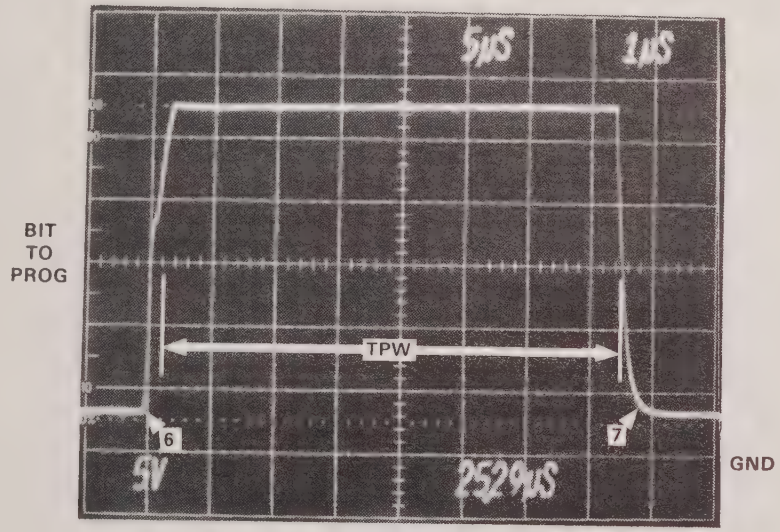
DRAWN BY: PP

CHECKED BY: KH

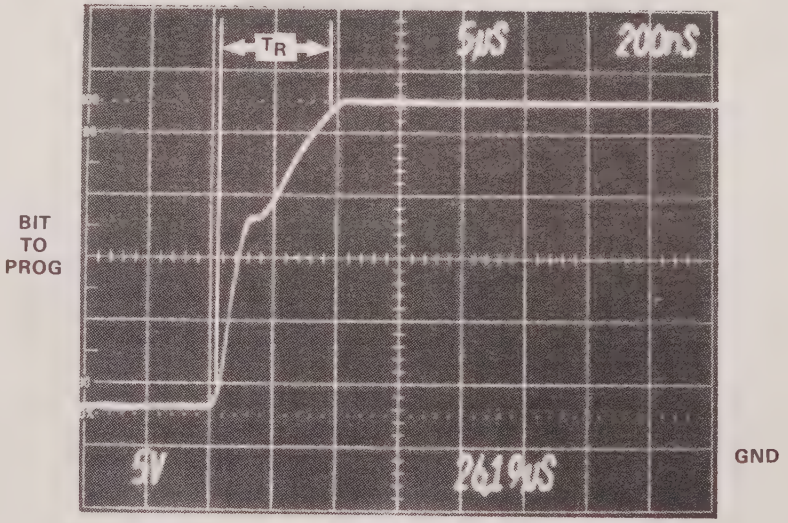
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

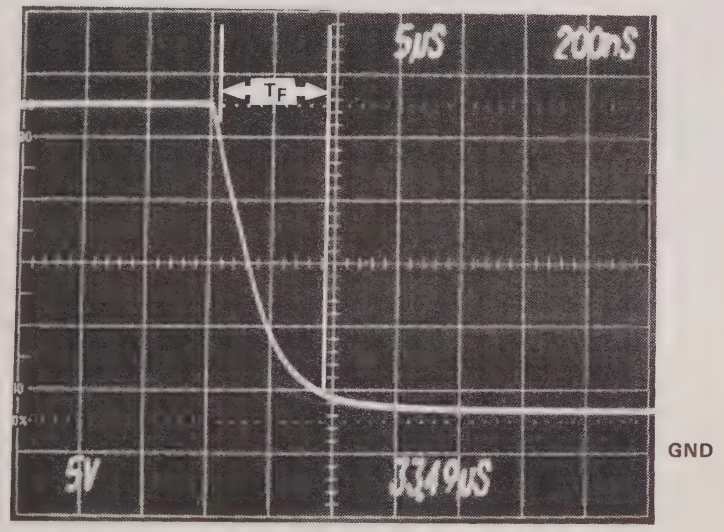
SHEET 1/2


5µS
1µS
BIT
TO
PROG
TPW
6
7
5V
2529µS
GND

5


TR
5µS
200nS
BIT
TO
PROG
5V
2619µS
GND

6

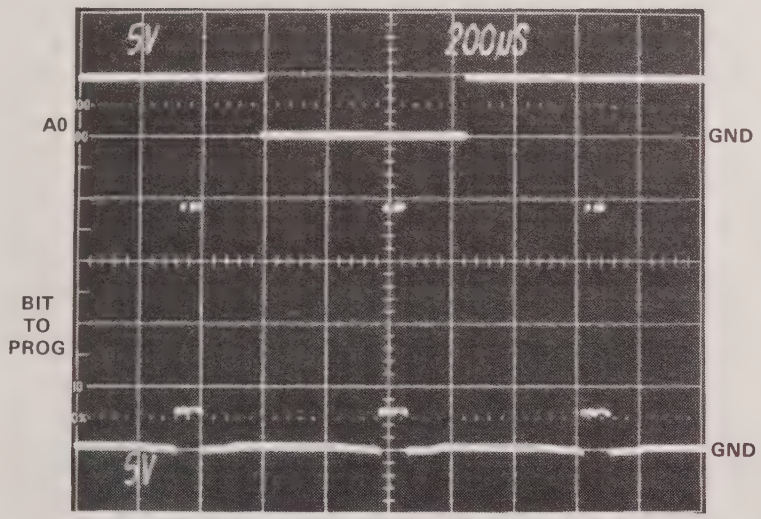

5µS
200nS
TF
BIT
TO
PROG
5V
3319µS
GND

7

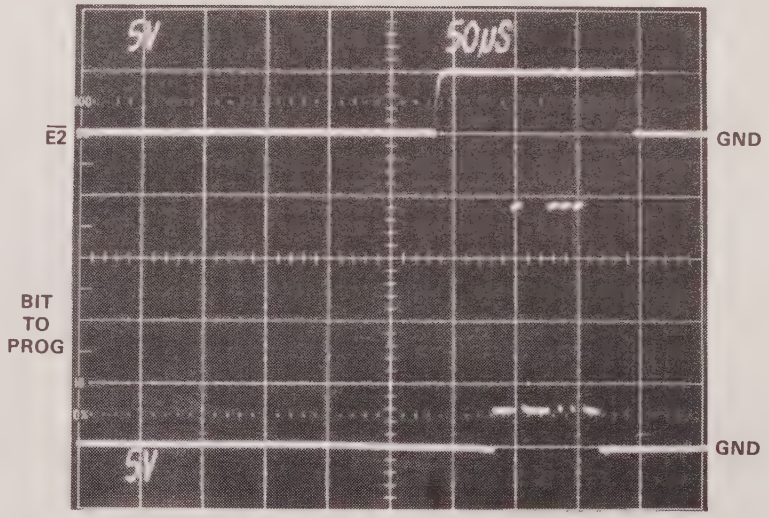
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/23

DATA I/O ISSAQUAH, WA

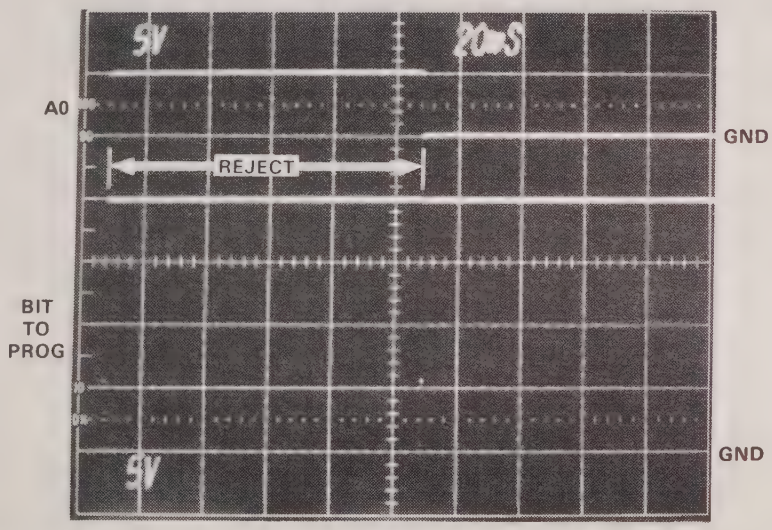
TITLE: TIMING DIAGRAM FAMILY CODES 71, 72		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
200µS
A0
GND
BIT
TO
PROG
GND
5V

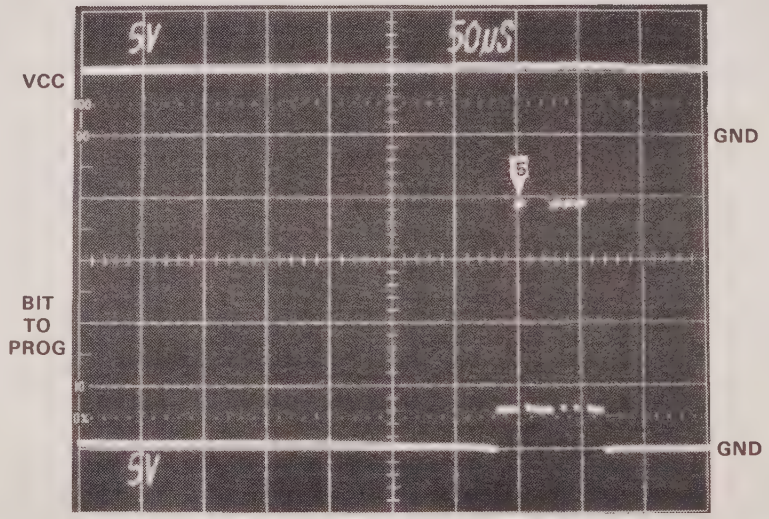
1


5V
50µS
$\overline{E2}$
GND
BIT
TO
PROG
GND
5V

2


5V
20mS
A0
GND
REJECT
BIT
TO
PROG
GND
5V

3


5V
50µS
VCC
GND
5
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.90	5.10	5.30	V	
	VPP					NA
	VOP	19.6	20.0	20.0	V	
	TPW	7.1	7.5	7.9	µs	See Note 2
	TR	180			ns	
	TF	180			ns	
	Overprogram		4		Pulses	
	Reject		10,000		Pulses	See Note 3
	Duty Cycle	70			%	
1ST PASS VERIFY	VCC	4.5	4.6	4.7	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.5	26.0	26.5	V	701-1655/TP4
	Low Load	25.5	26.0	26.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.5	6.6	6.7	V	
	VREF	4.4	4.5	4.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.7	7.2	7.7	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 73.*
2. *Load RAM with hex 01 for Family 74.*
3. *Measurement taken at 10V point of 01 with a 150 Ω load.*
4. *10,000 pulses equals 100 ms, as shown in photo 3.*
5. *Do not use a wirewound load resistor.*
6. *For Pinouts 16 and 21, E2 is seen on E1.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		CH	3/8
		ECN #5023		E73	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 73, 74

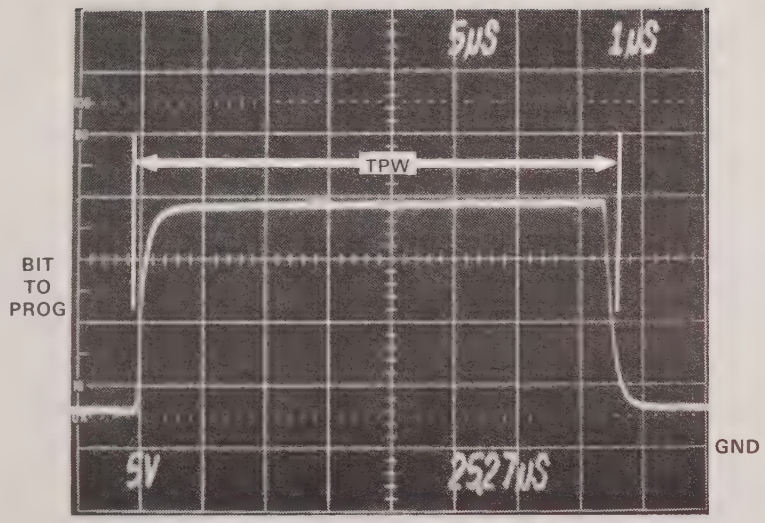
DRAWN BY: EE

CHECKED BY: CH

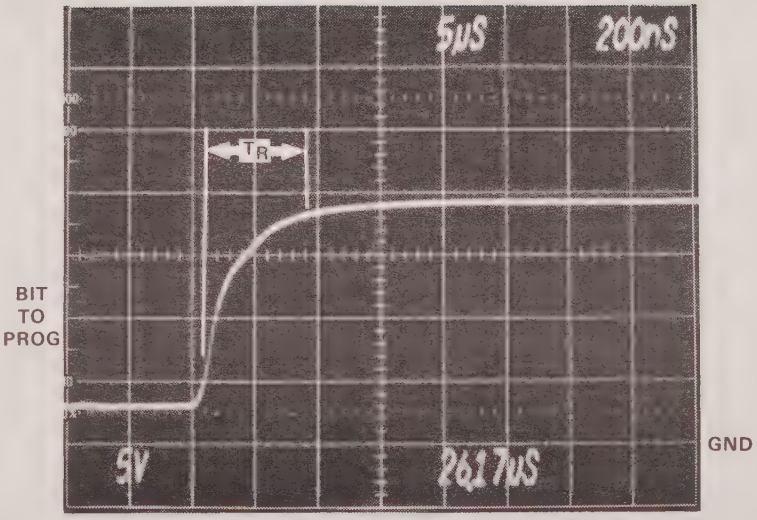
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

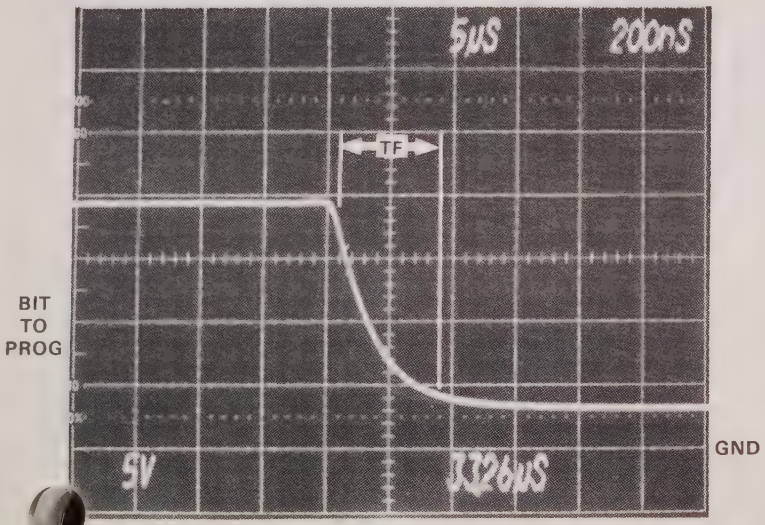
SHEET 1/2


5µS
1µS
TPW
BIT
TO
PROG
GND
5V
25.27µS

5


5µS
200nS
TR
BIT
TO
PROG
GND
5V
26.17µS

6

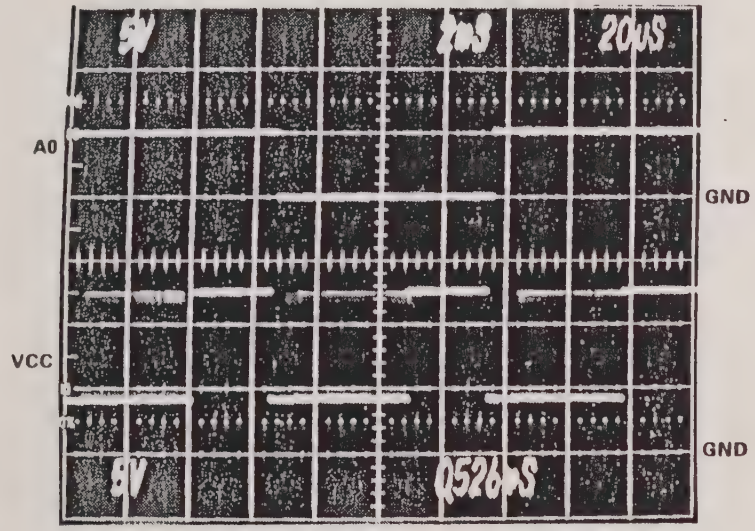

5µS
200nS
TF
BIT
TO
PROG
GND
5V

7

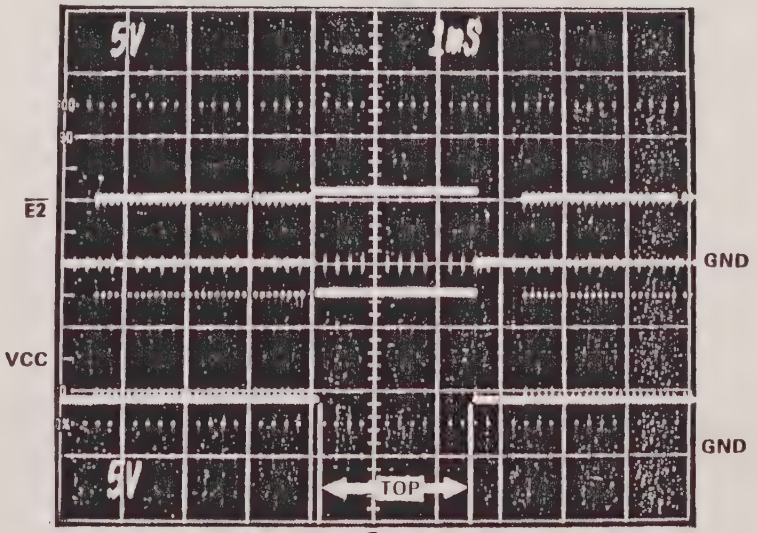
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

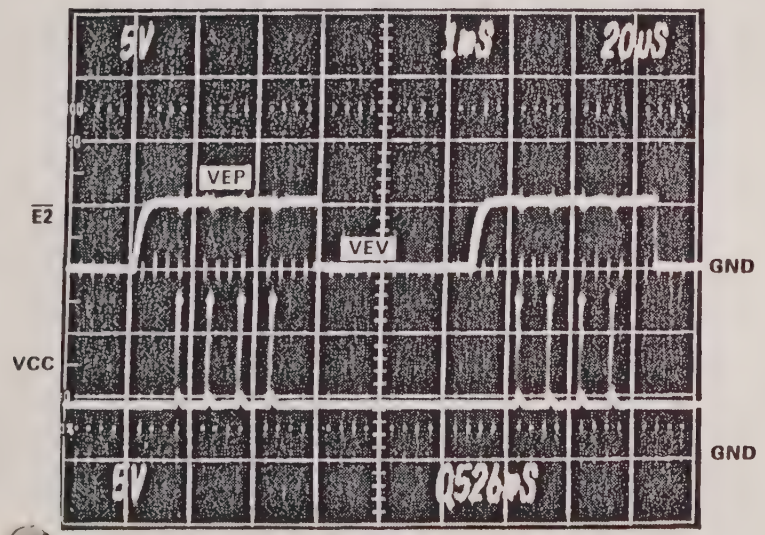
TITLE: TIMING DIAGRAM FAMILY CODES 73, 74		DRAWN BY: EE CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
2mS
20uS
A0
GND
VCC
GND
5V
0526mS

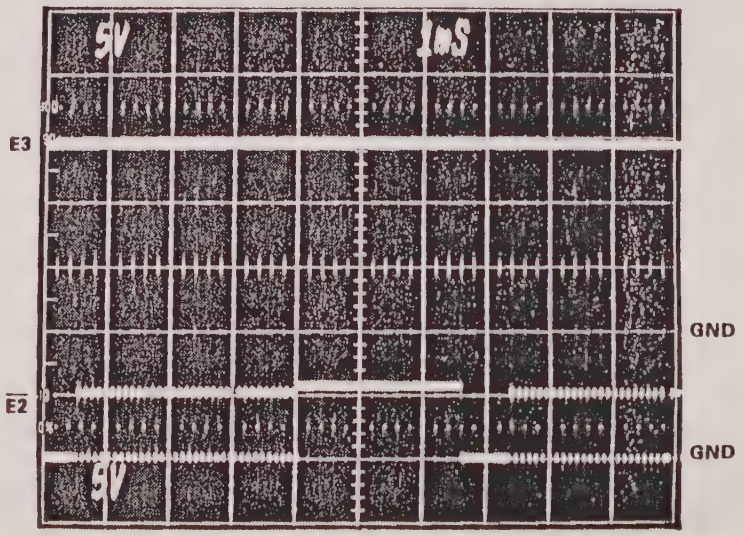
1


5V
1mS
E2
GND
VCC
GND
5V
TOP

2


5V
1mS
20uS
VEP
E2
VEV
GND
VCC
GND
5V
0526mS

3


5V
1mS
E3
GND
E2
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	12.0	12.5	13.0	V	See Note 6
	VCCV	4.25	4.5	4.75	V	
	VEP	3.0	5.0	5.5	V	
	VEV	0.0	0.2	0.4	V	
	TPWB	140	200	260	ns	See Note 4
	TPWE	7.2	8.0	8.8	µs	See Note 4
	TR	320	400	480	ns	See Note 5
	TF	50	100	200	ns	See Note 5
	Reject	780	800	820	ms	
	TOP	2.2	2.5	2.8	ms	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.4	0.5	0.6	V	701-1655/TP2
	High Load	17.5	18.5	19.5	V	701-1655/TP4
	Low Load	17.5	18.5	19.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.2	2.3	2.4	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	6.9	7.9	8.9	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 75.*
2. *Load RAM with hex 01 for Family 76.*
3. *To observe waveforms, load 01 with a 100 Ω, 2-watt resistor. Do not use a wirewound resistor.*
4. *V_{CC} pulse width ramps linearily from TPWB to TPWE. This is visible only with no load on 01. TPW is measured at 12V.*
5. *TR and TF are measured from 5V to 12V.*
6. *Photos 5 and 6 were taken with V_{CC} loaded with a 50 Ω, 5-watt resistor. Do not use a wirewound resistor.*

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10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4772		XH	1/83
		ECN #4831		XH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM

FAMILY CODES 75, 76

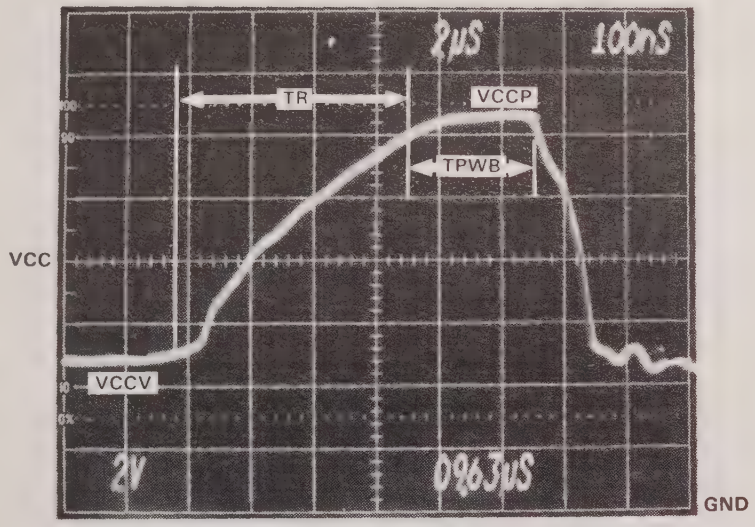
DRAWN BY: BG

CHECKED BY:

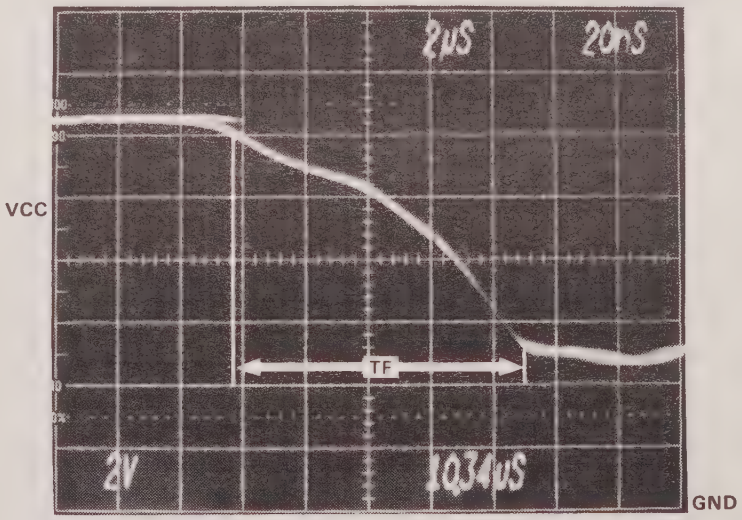
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


2µS
100nS
TR
VCCP
TPWB
VCC
VCCV
2V
0963µS
GND

5

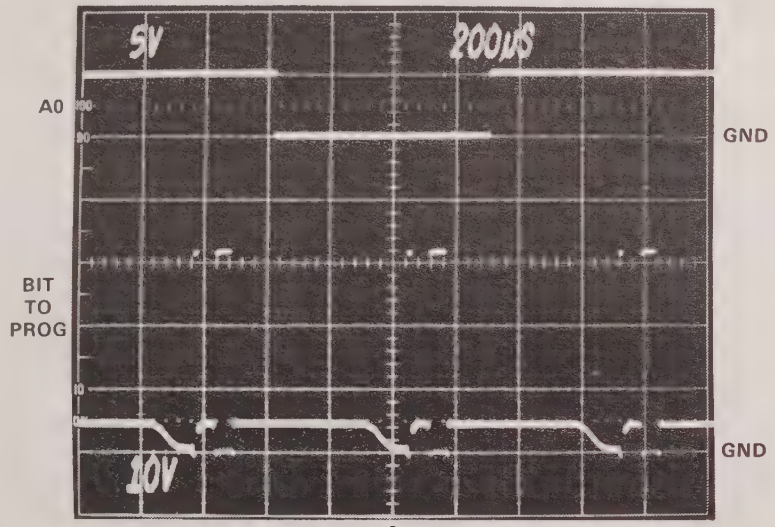

2µS
20nS
VCC
TF
2V
1034µS
GND

6

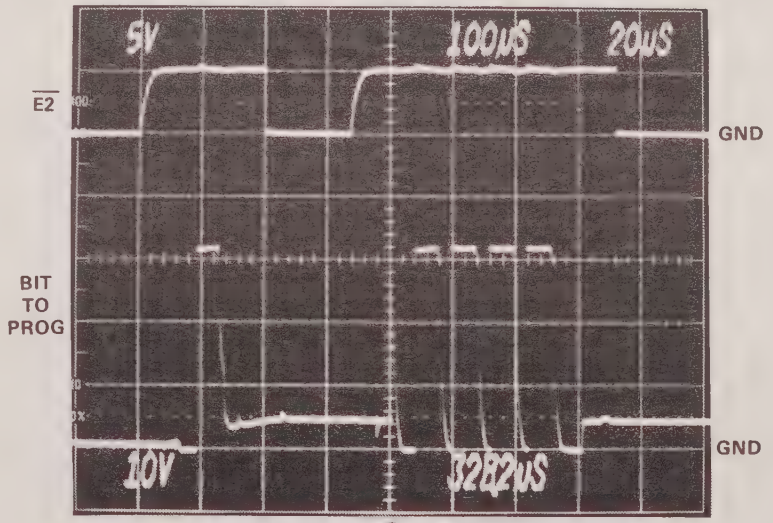
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.B.	11/82
		ECN #4831		KH	5/83

DATA I/O ISSAQUAH, WA

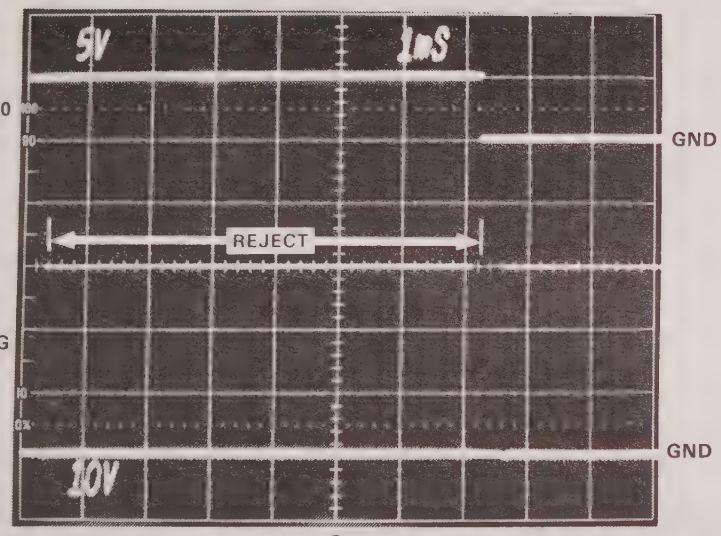
TITLE: TIMING DIAGRAM FAMILY CODES 75, 76	DRAWN BY: BCJ KH	CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
200µS
A0
GND
BIT
TO
PROG
GND
10V

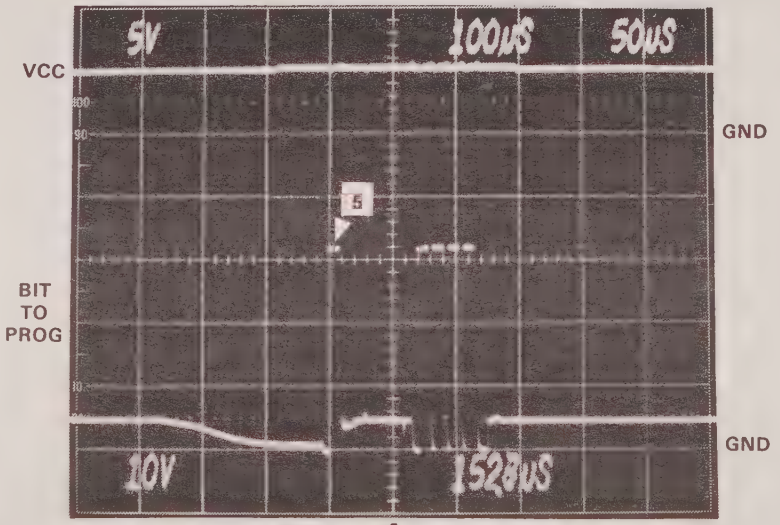
1


5V
100µS
20µS
E2
GND
BIT
TO
PROG
GND
10V
32.2µS

2


5V
1mS
A0
GND
REJECT
BIT
TO
PROG
GND
10V

3


5V
100µS
50µS
VCC
GND
5
BIT
TO
PROG
GND
10V
152µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.00	5.20	5.40	V	
	VPP					NA
	VOP	31.5	31.7	32.0	V	
	TPN	7.2	7.5	7.8	µs	See Note 2
	TR	0.34		0.68	µs	
	TF	0.34		0.48	µs	
	Overprogram		4		Pulses	
	Reject		100		Pulses	See Note 3
	Duty Cycle	11			%	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	7.8	8.8	9.8	V	701-1655/TP4
	Low Load	7.8	8.8	9.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	3.9	4.0	4.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	5.6	6.6	7.6	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 77.*
2. *Load RAM with hex 01 for Family 78.*
3. *Measurement taken at 15V point of 01 with 150 Ω load.*
4. *100 pulses equals 6.8 ms, as shown in photo 3, with 150 Ω load.*
5. *Do not use a wirewound load resistor.*
6. *Photos 1, 2, and 4 have 01 loaded with 3.3K Ω.*

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10-950-0059

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4772		KA	1/83
		ECN #4831		ZZ	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 77, 78

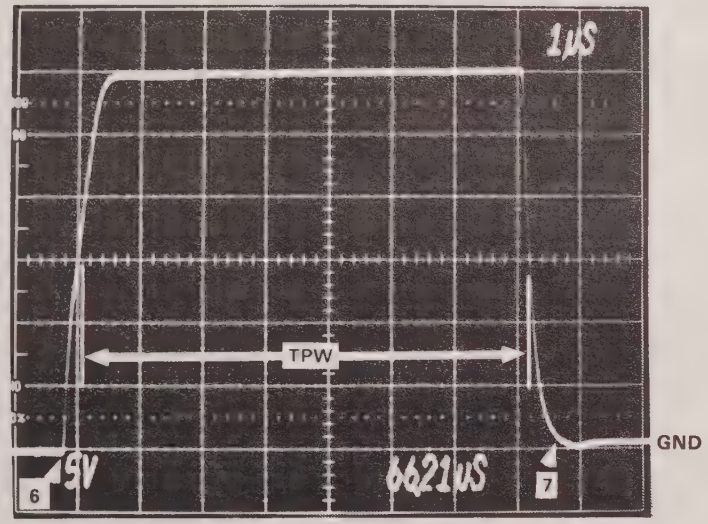
DRAWN BY: EE

CHECKED BY:

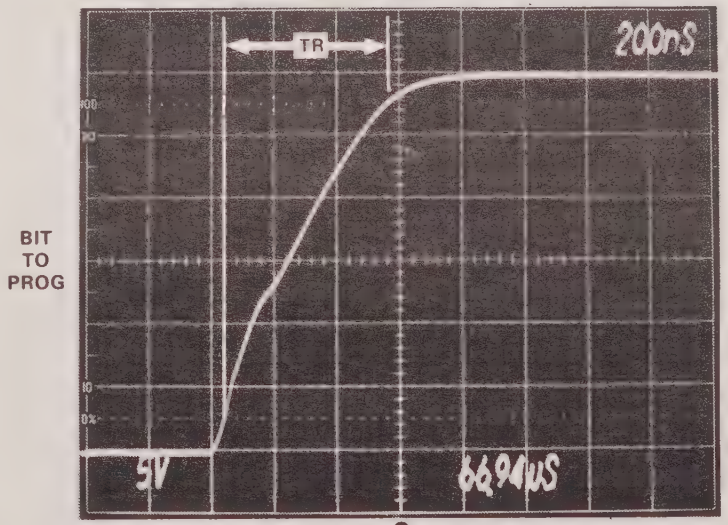
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

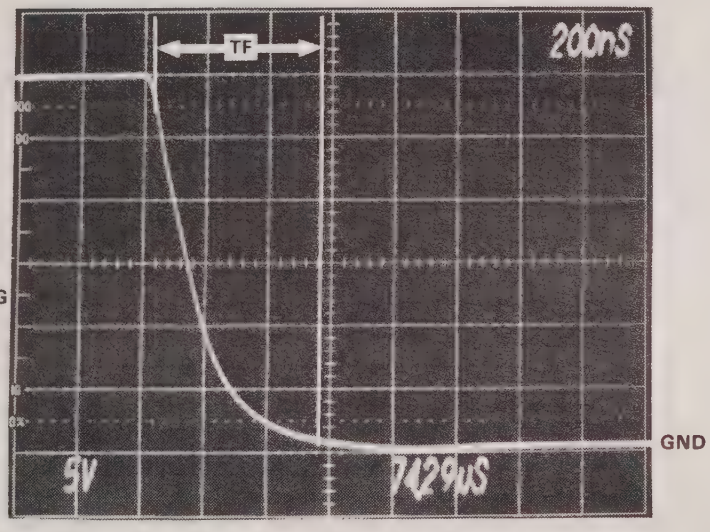
SHEET 1/2


1µS
BIT
TO
PROG
TPW
GND
5V
6
6621µS
7

5


TR
200nS
BIT
TO
PROG
GND
5V
6694µS

6


TF
200nS
BIT
TO
PROG
GND
5V
7429µS

7

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		ZH	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 77, 78

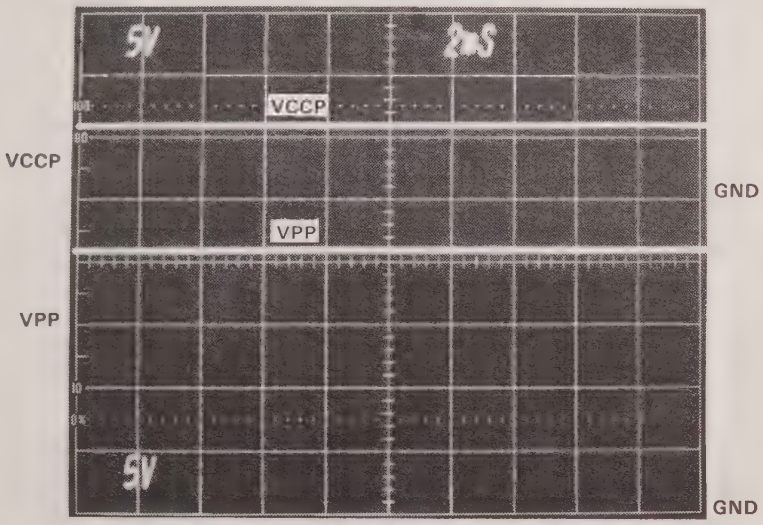
DRAWN BY: EE

CHECKED BY:

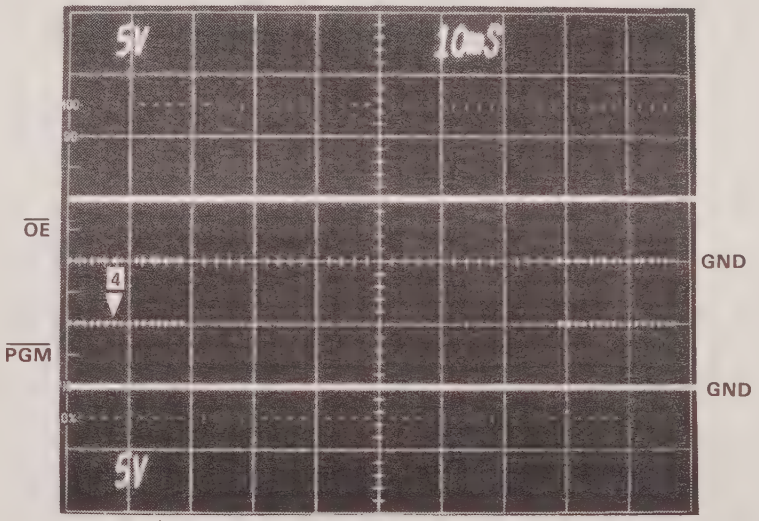
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

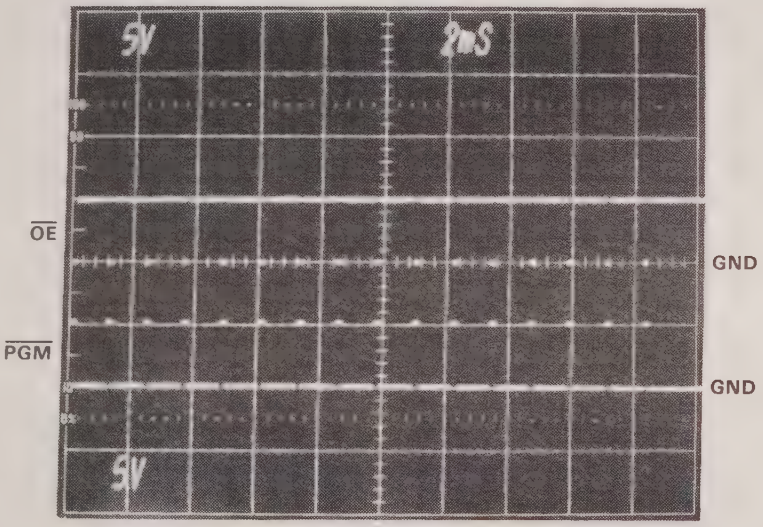
SHEET 2/2


5V
2mS
VCCP
VPP
VCCP
VPP
GND
5V
GND

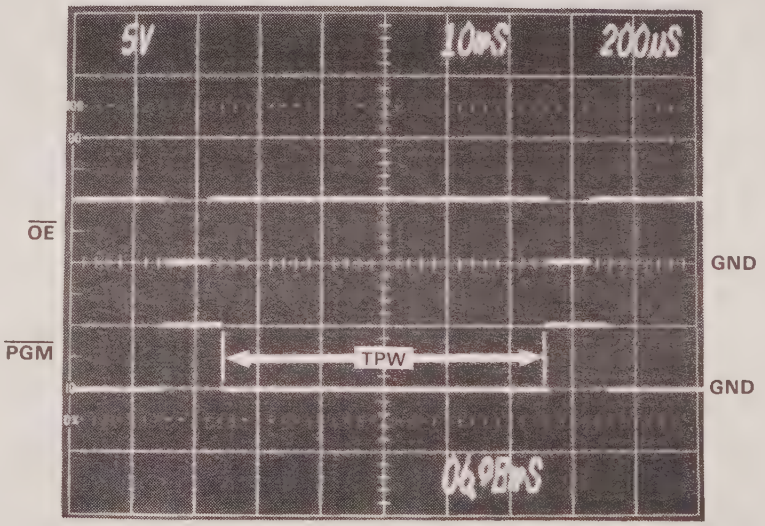
1


5V
10mS
OE
4
PGM
GND
GND
5V

2


5V
2mS
OE
PGM
GND
GND
5V

3


5V
10mS
200uS
OE
PGM
TPW
GND
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV					NA
	TPW	0.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		15		Pulses	
	Overprogram		1		Pulses	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 79.*
2. *Load RAM with hex 01 for Family 80, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse follows the reject pulses and its length is the number of reject pulses multiplied by 4 ms.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		KH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 79, 80

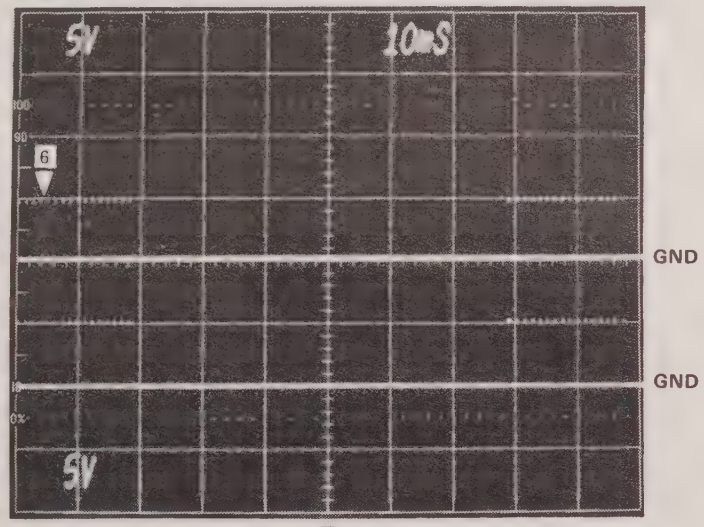
DRAWN BY: BG KC

CHECKED BY:

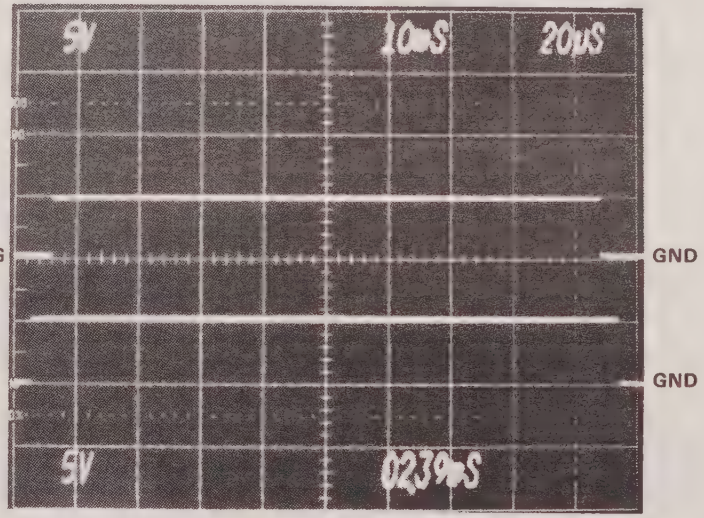
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

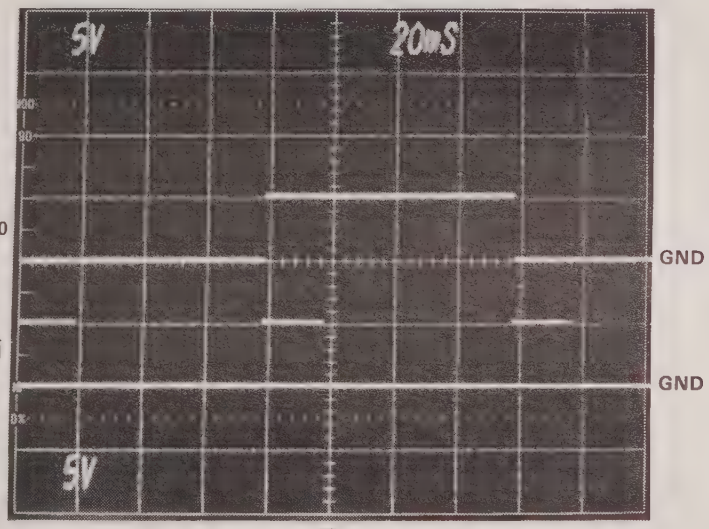
SHEET 1/2


5V
10mS
6
BIT
TO
PROG
GND
PGM
GND
5V

5


5V
10mS
20μS
BIT
TO
PROG
GND
PGM
GND
5V
0239mS

6


5V
20mS
A0
GND
PGM
GND
5V

7

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.S.	11/82
		ECN #4831		XN	5/85

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 79, 80

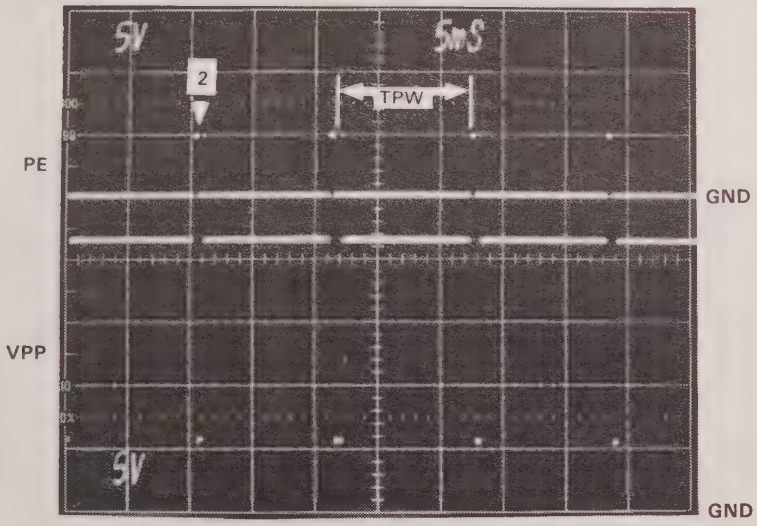
DRAWN BY: BG/KC

CHECKED BY:

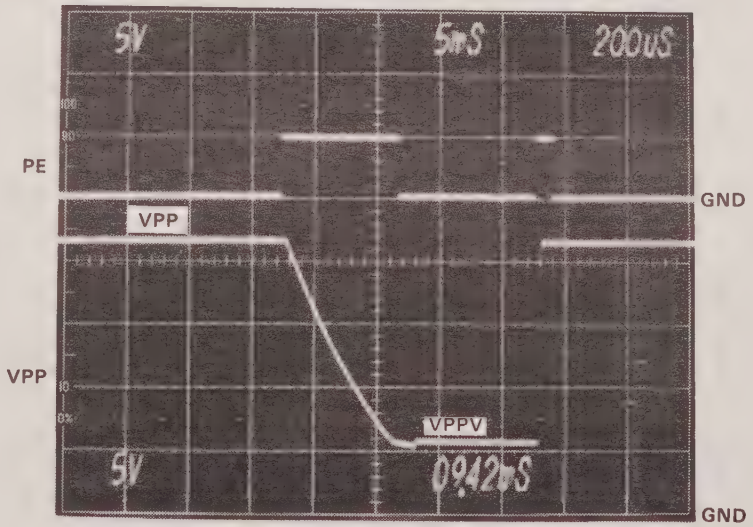
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

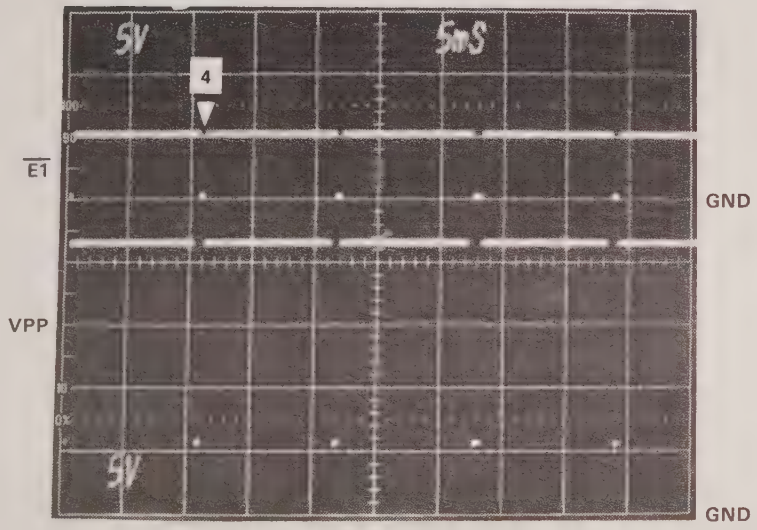
SHEET 2/2


5V
5mS
2
TPW
PE
GND
VPP
5V
GND

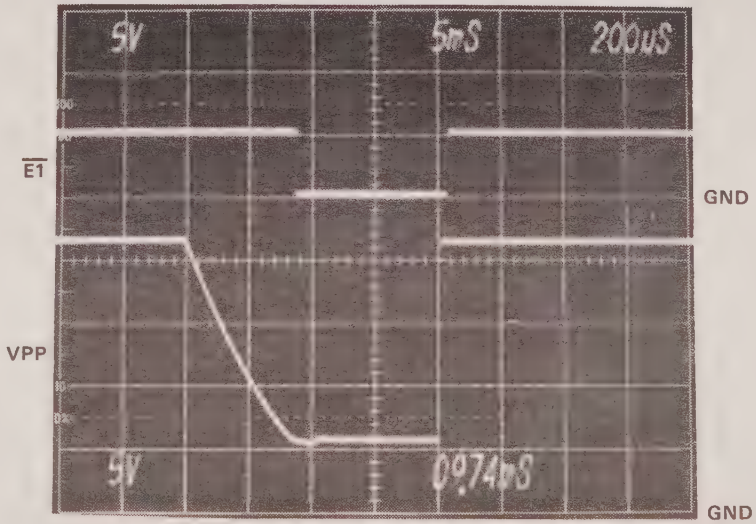
1


5V
5mS
200uS
PE
GND
VPP
VPP
VPPV
5V
0.942mS
GND

2


5V
5mS
4
E1
GND
VPP
5V
GND

3


5V
5mS
200uS
E1
GND
VPP
5V
0.974mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	9.8	10.0	10.2	ms	
	TR	1			µs	
	TF	1			µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 81.*
2. *Load RAM with hex 01 for Family 82, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 13 through 18 are Byte erase waveforms.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		KH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 81, 82

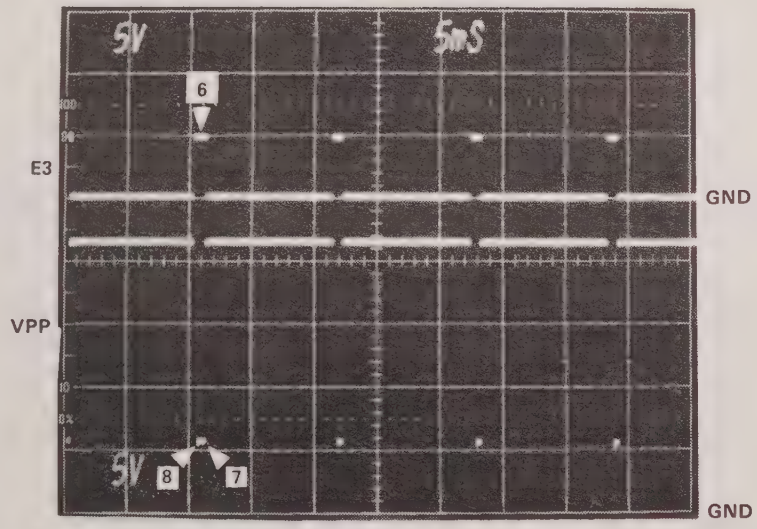
DRAWN BY:

CHECKED BY:

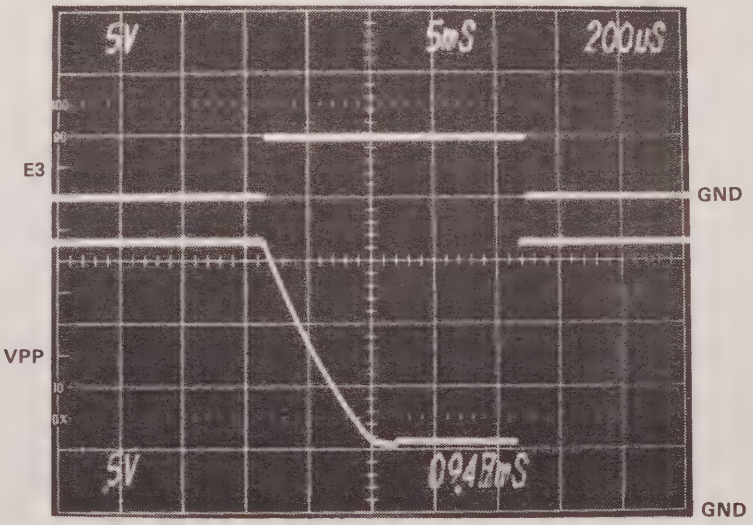
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

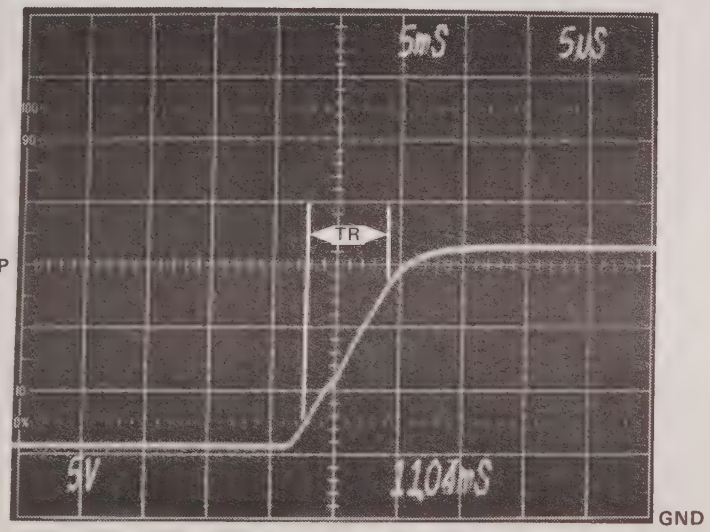
SHEET 1/4


5V
5mS
6
E3
GND
VPP
5V
8
7
GND

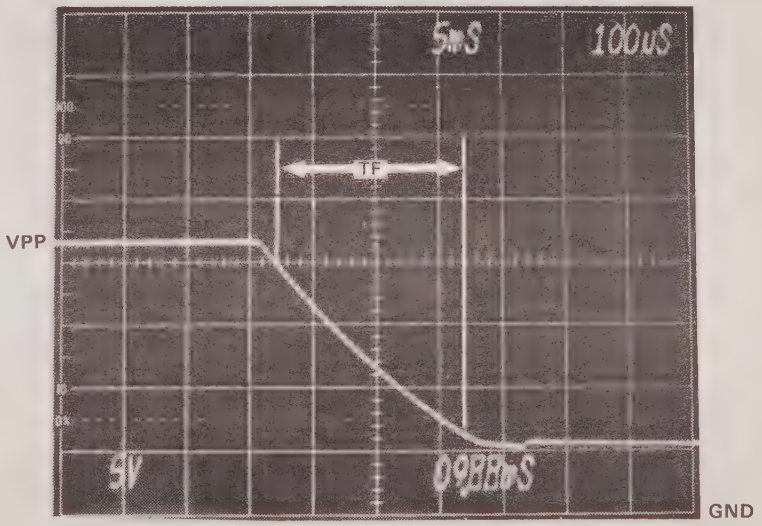
5


5V
5mS
200uS
E3
GND
VPP
5V
GND

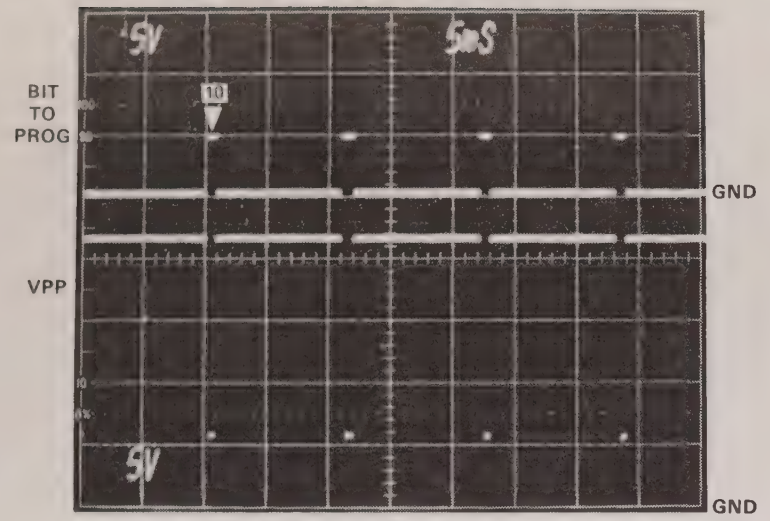
6


5mS
5uS
VPP
TR
5V
GND

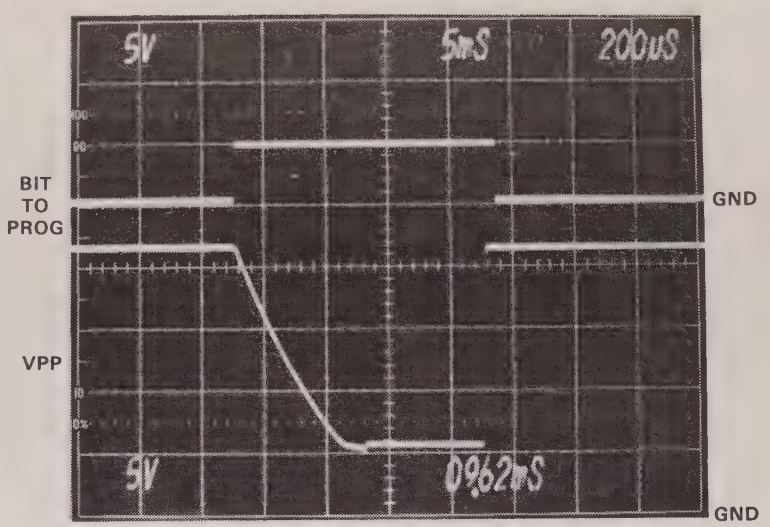
7


5mS
100uS
TF
VPP
5V
GND

8



9



10

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		E.J.Z.	11/82
		ECN #4831		[illegible]	5/83

DATA I/O ISSAQUAH, WA

TITLE TIMING DIAGRAM

FAMILY CODES 81, 82

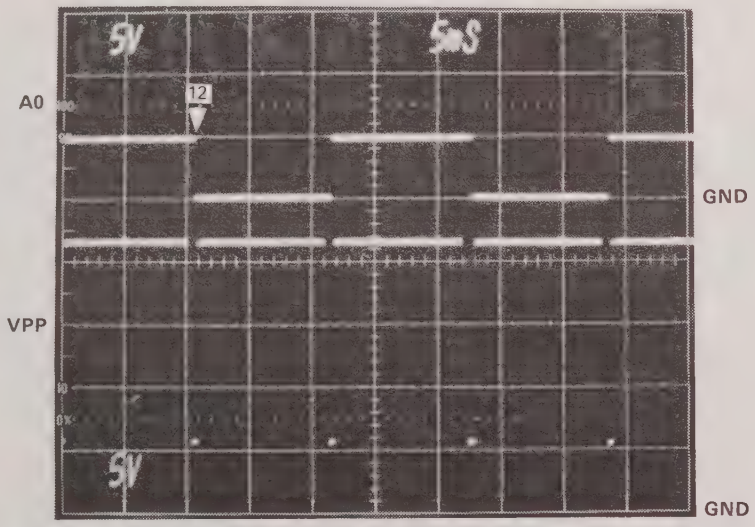
DRAWN BY: [illegible]

CHECKED BY:

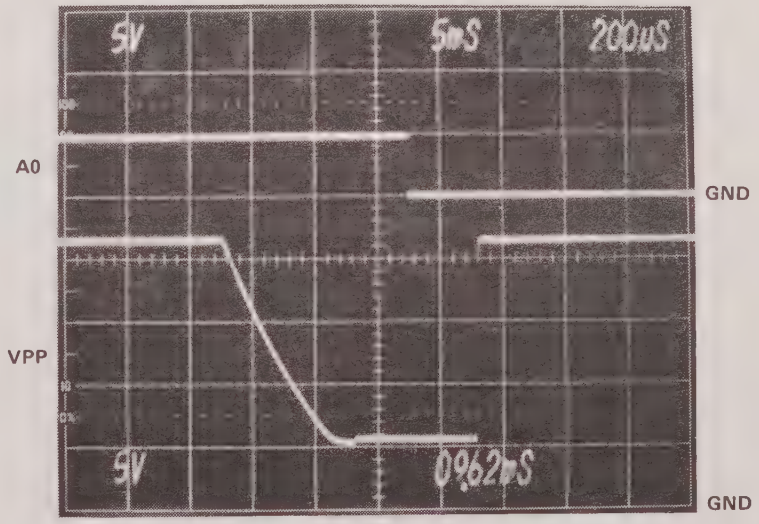
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

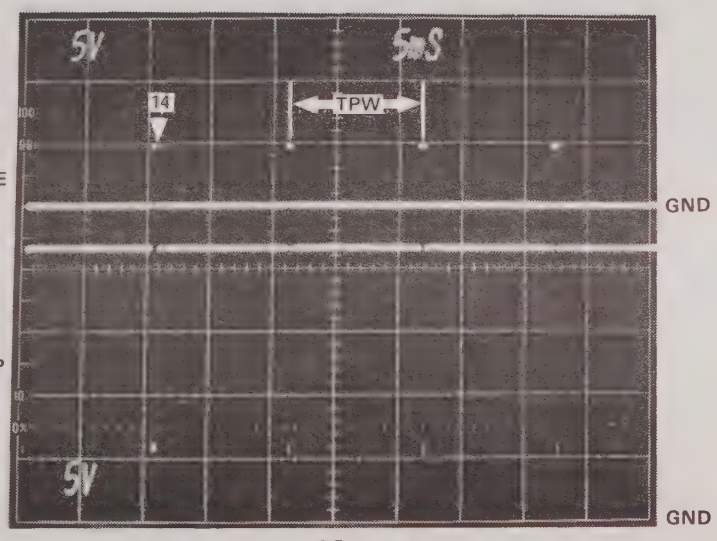
SHEET 2/4


5V
5mS
A0
12
GND
VPP
5V
GND

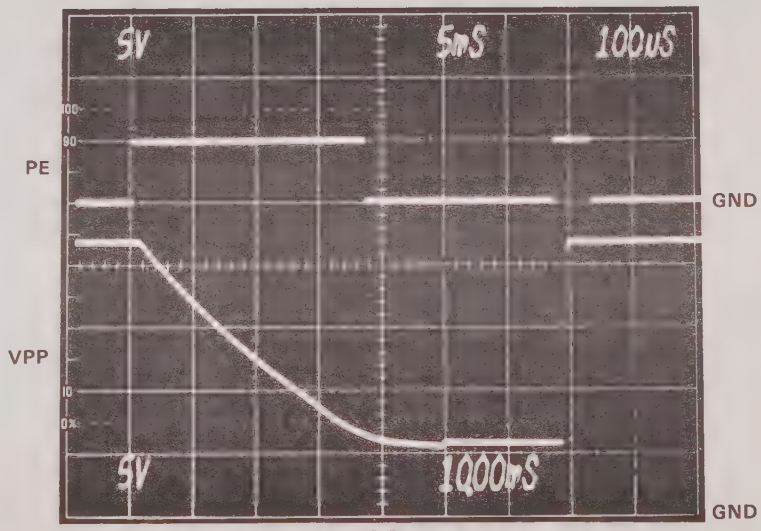
11


5V
5mS
200uS
A0
GND
VPP
5V
0%62mS
GND

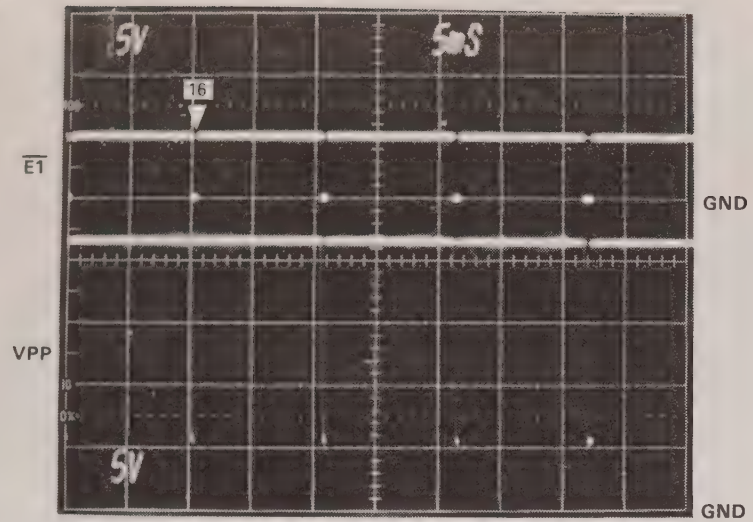
12


5V
5mS
14
TPW
PE
GND
VPP
5V
GND

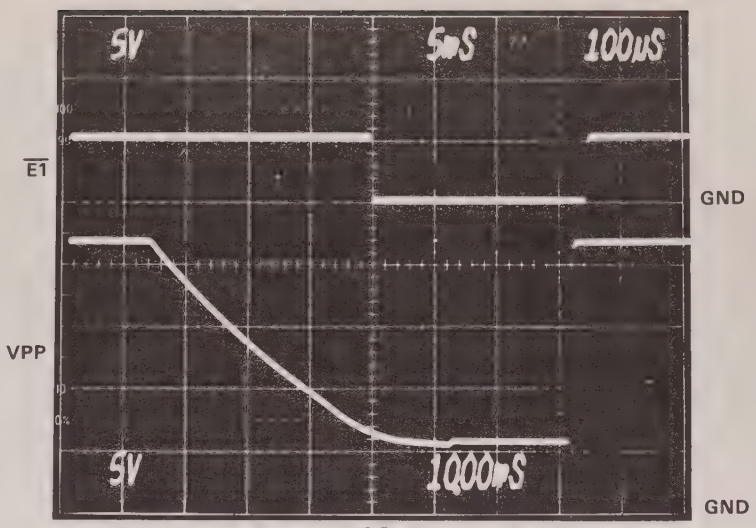
13


5V
5mS
100uS
PE
GND
VPP
5V
1Q00mS
GND

14



15



16

B-153
10-950-0059

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ.	11/82
		ECN #4831		XN	3/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 81, 82

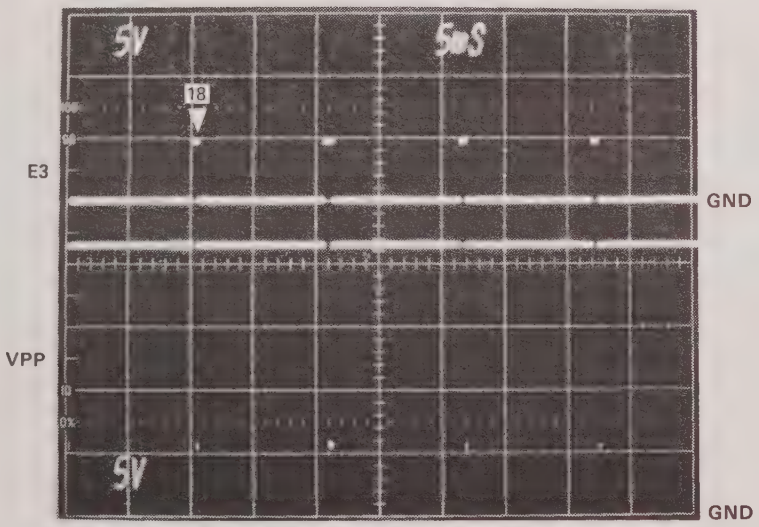
DRAWN BY:

CHECKED BY:

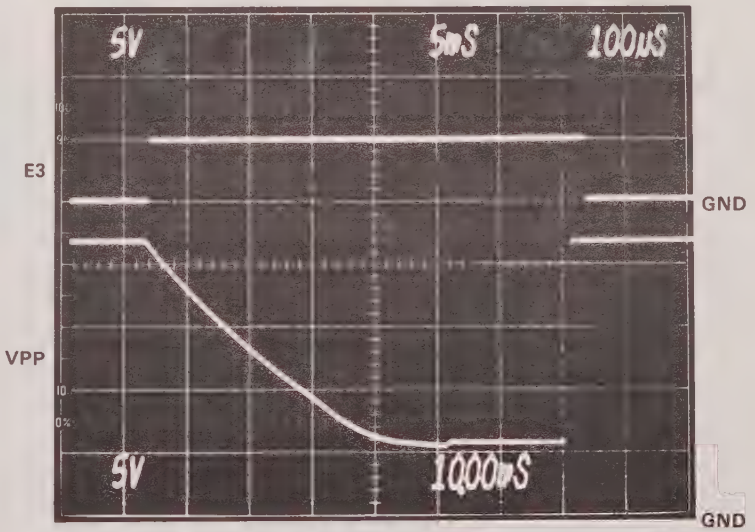
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 3/4



17

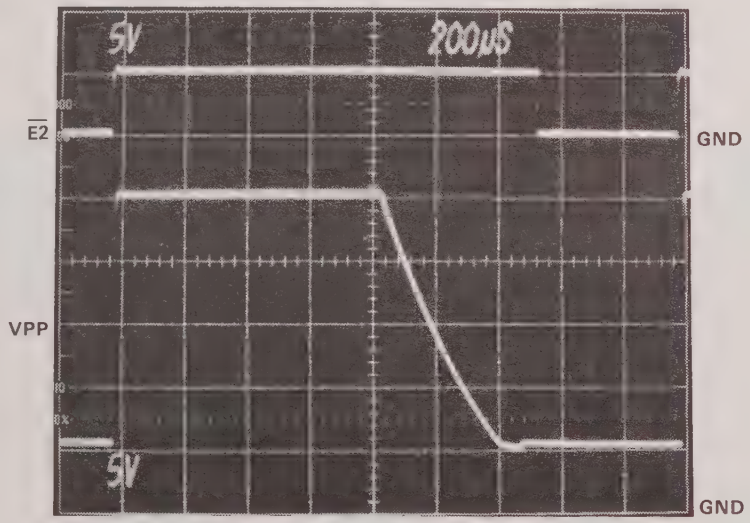


18

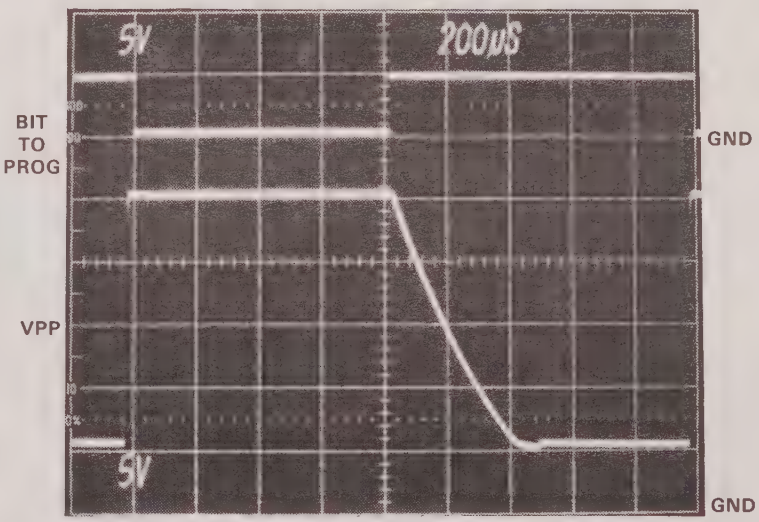
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		??	??/??
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

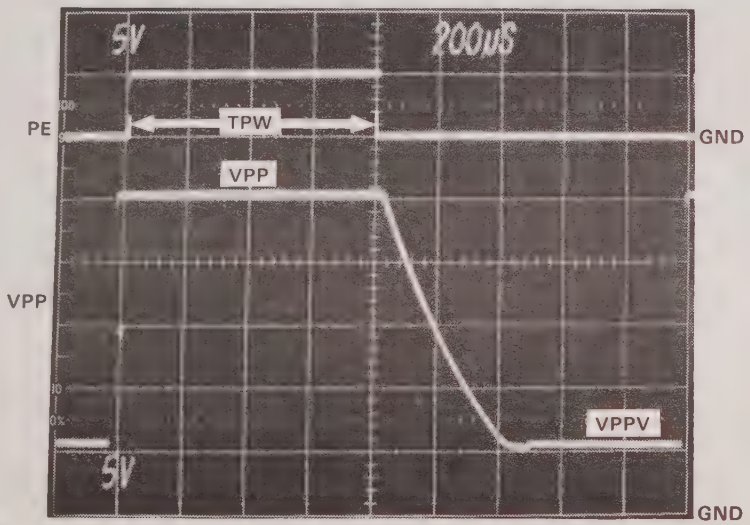
TITLE: TIMING DIAGRAM FAMILY CODES 81, 82		DRAWN BY: KC CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 4/4


5V
200uS
E2
GND
VPP
5V
GND

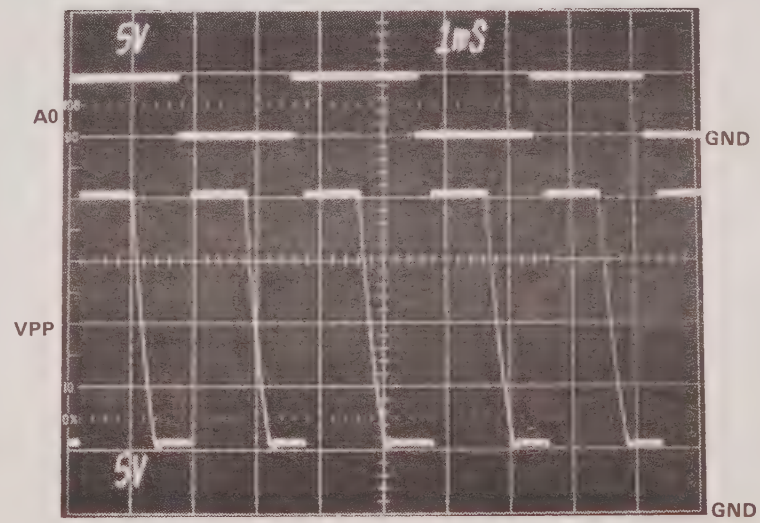
1


5V
200uS
BIT
TO
PROG
GND
VPP
5V
GND

2


5V
200uS
PE
TPW
GND
VPP
VPP
VPPV
5V
GND

3


5V
1mS
A0
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	800			µs	
	TR	5			ns	
	TEP	1			sec	
	TF	5			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 83.*
2. *Load RAM with hex 01 for Family 84, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photo 7 is the erase waveform.*

REVISIONS

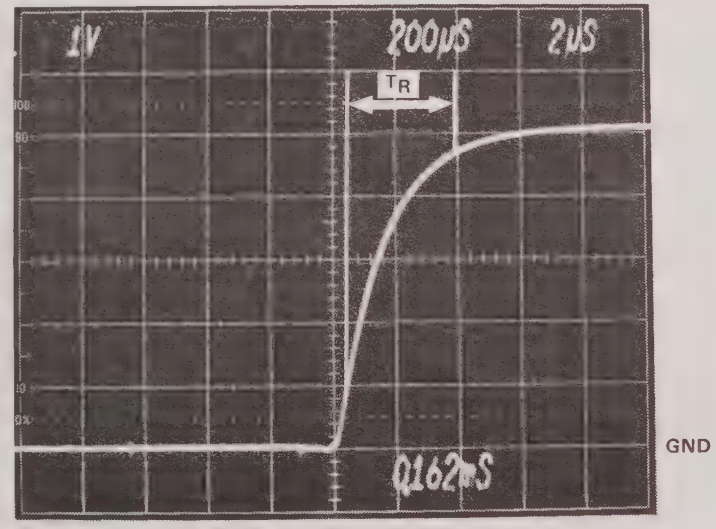
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		XA	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

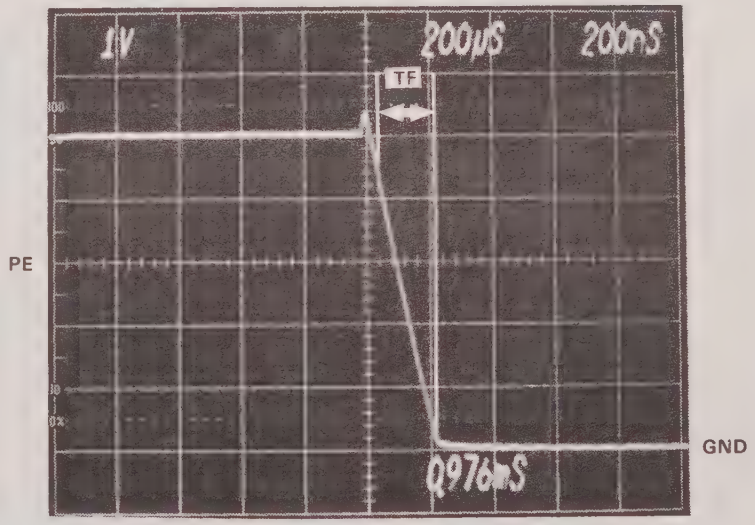
TITLE: TIMING DIAGRAM	DRAWN BY:
FAMILY CODES 83, 84	CHECKED BY:

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

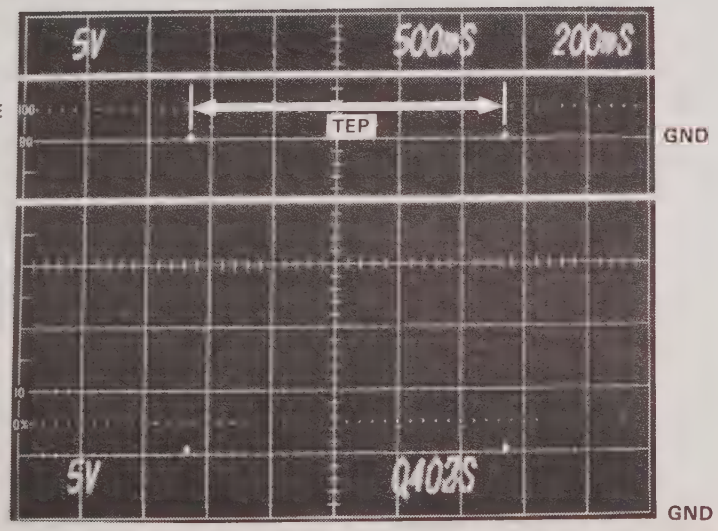
SCALE | SHEET 1/2


1V
200μS
2μS
TR
PE
GND

5


1V
200μS
200nS
TF
PE
GND

6

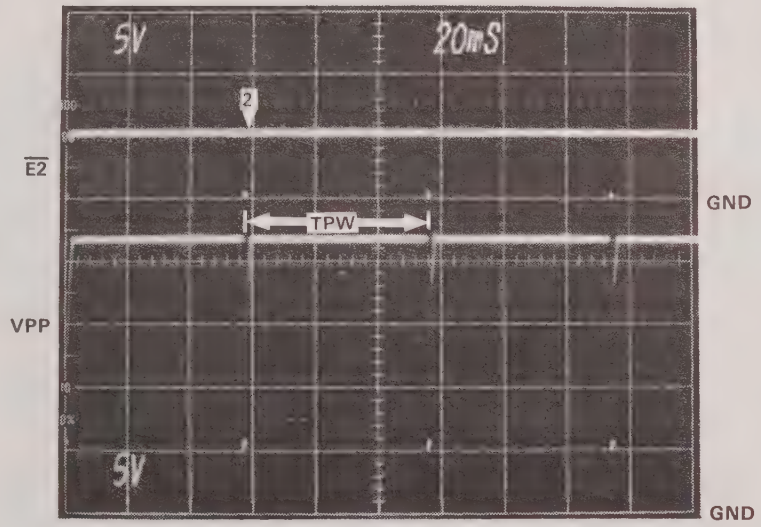

5V
500mS
200mS
TEP
PE
GND
VPP
5V
GND

7

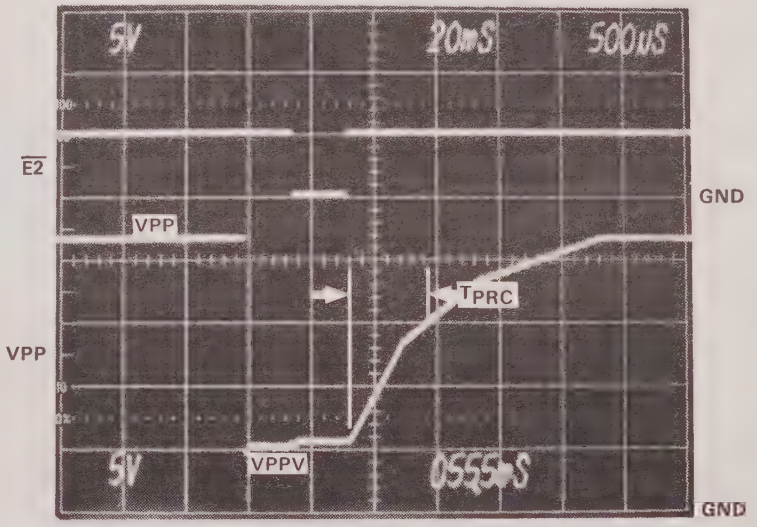
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		E.T.3.	11/82
		ECN #4831		XH	5/83

DATA I/O ISSAQUAH, WA

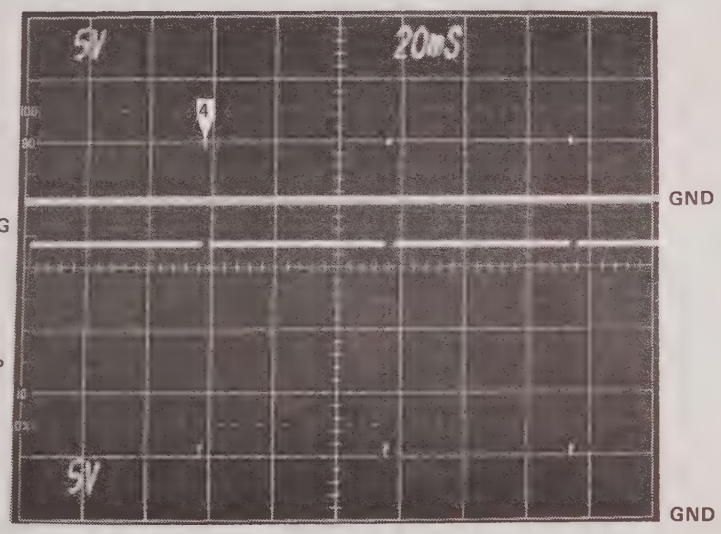
TITLE: TIMING DIAGRAM FAMILY CODES 83, 84		DRAWN BY: CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
20mS
2
$\overline{E2}$
GND
TPW
VPP
5V
GND

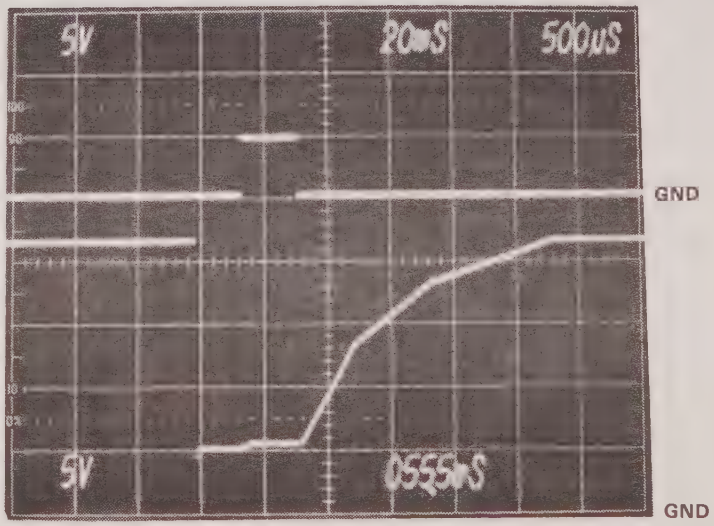
1


5V
20mS
500uS
$\overline{E2}$
GND
VPP
TPRC
VPP
VPPV
5V
GND

2


5V
20mS
4
BIT
TO
PROG
GND
VPP
5V
GND

3


5V
20mS
500uS
BIT
TO
PROG
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.0	5.0	6.0	V	
	VEE	9.0		15.0	V	
	TPW	50		70	ms	
	T_{PRC}	450	600	750	µs	See note 3
	T_F			100	µs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.3	5.3	6.3	V	701-1655/TP4
	Low Load	4.3	5.3	6.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	3.8	4.8	5.8	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 85.*
2. *Load RAM with hex 01 for Family 86, and bit-to-prog waveform becomes bit-no-prog.*
3. *TPRC is measured from 6V to 15.5V.*
4. *Photos 8 and 9 are erase waveforms.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		KH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE **TIMING DIAGRAM**

FAMILY CODES 85, 86

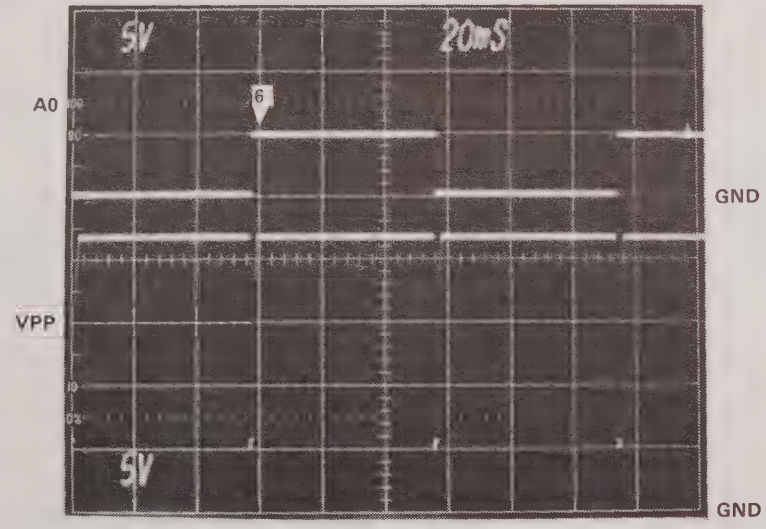
DRAWN BY:

CHECKED BY:

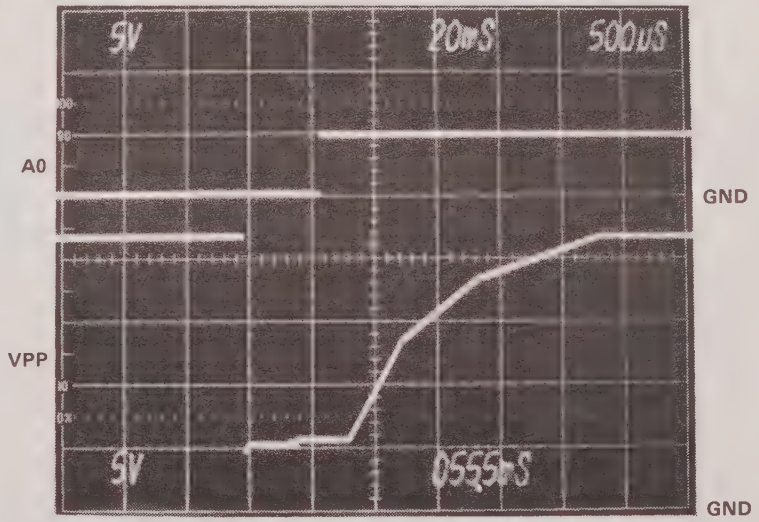
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

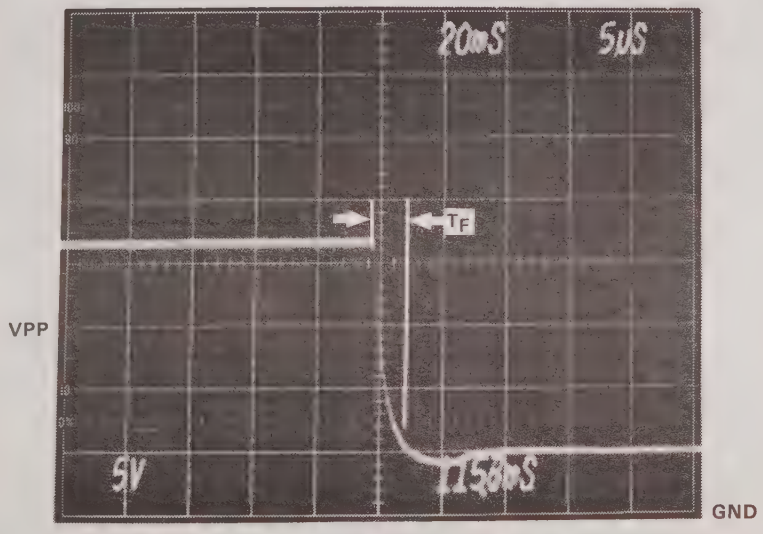
SHEET 1/2


5V
20mS
A0
6
GND
VPP
5V
GND

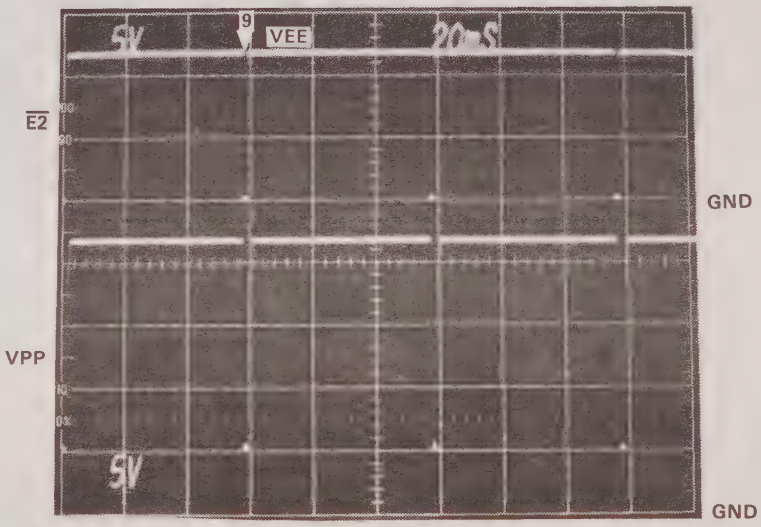
5


5V
20mS
500uS
A0
GND
VPP
5V
GND

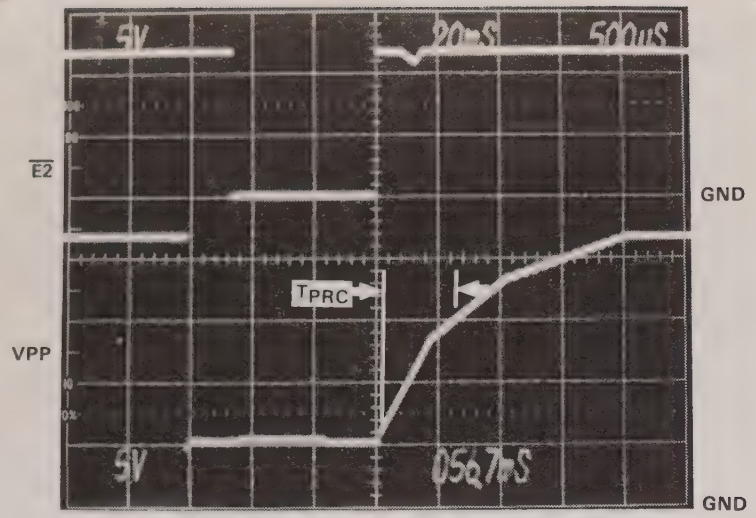
6


20mS
5uS
TF
VPP
5V
GND

7


5V
9
VEE
20mS
E2
GND
VPP
5V
GND

8



9

B-163
10-950-0059

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		E.J.Z.	11/82
		ECN #4831		XX	5/83
		ECN #5023		EJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE **TIMING DIAGRAM**

FAMILY CODES 85, 86

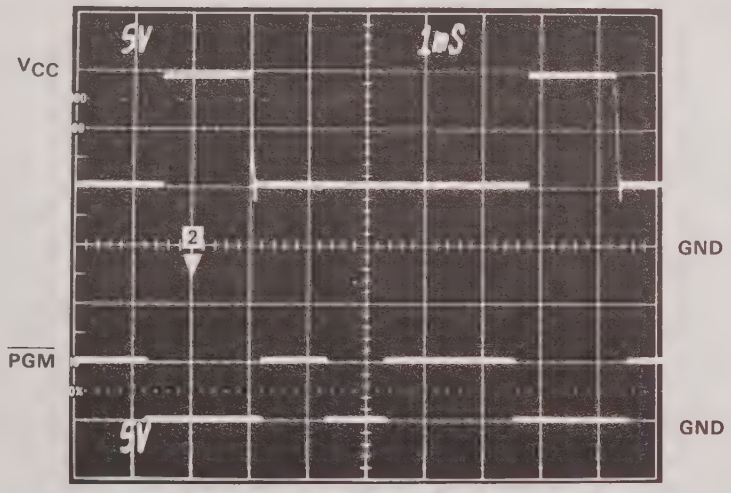
DRAWN BY:

CHECKED BY:

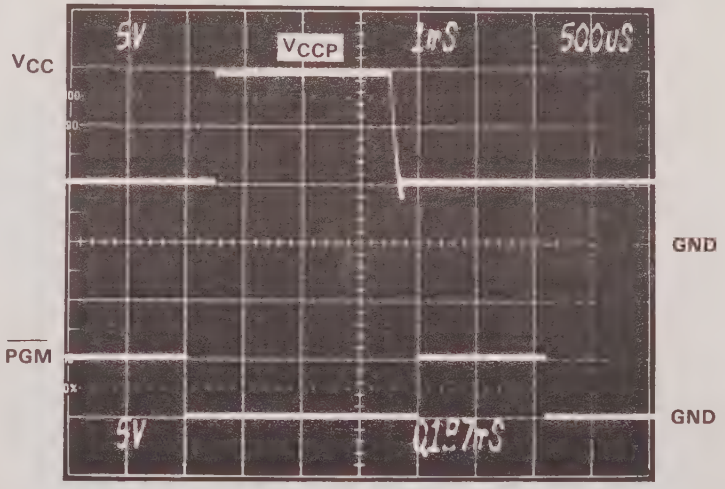
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

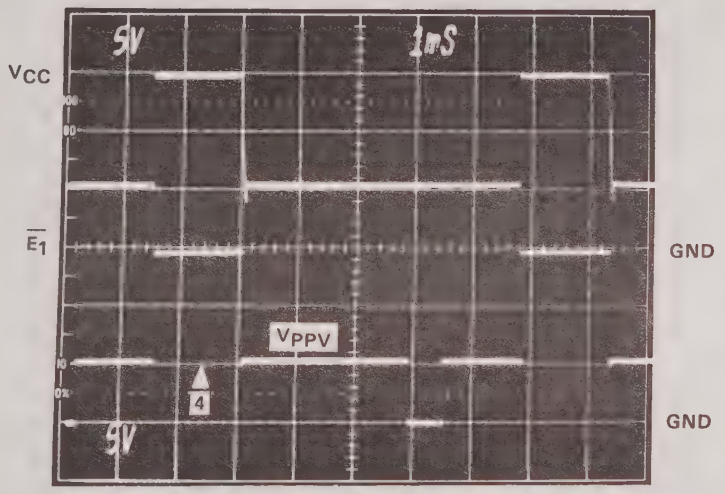
SHEET 2/2


5V
1mS
VCC
2
GND
PGM
GND
5V

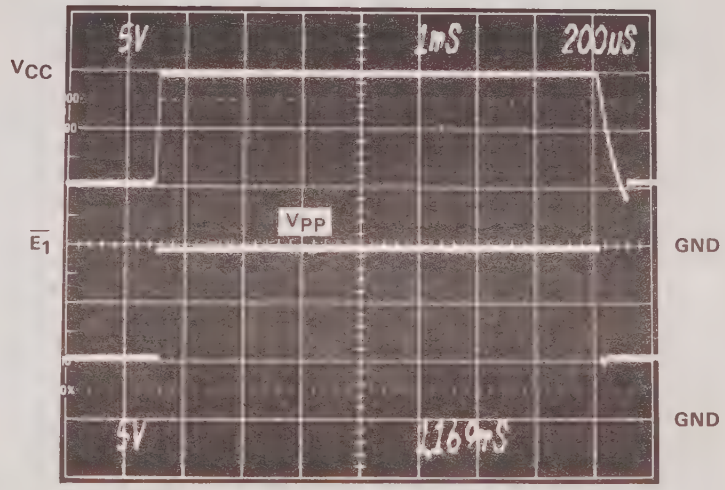
1


5V
VCCP
1mS
500uS
VCC
GND
PGM
GND
5V

2


5V
1mS
VCC
E1
GND
VPPV
4
GND
5V

3


5V
1mS
200uS
VCC
E1
VPP
GND
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	13.5	14.0	14.0	V	
	V_{OP}	12.0	14.0	14.3	V	
	V_{PP}	12.0	14.0	14.3	V	
	V_{PPV}	4.75	5.0	5.25	V	
	t_{pw}	0.9	1	1.1	ms	
	t_r					N.A.
	t_{cp}	475	500	525	μs	
	t_f					N.A.
	Reject		8		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	3.9	4.0	4.1	V	
	V_{REF}	0.3	0.4	0.5	V	701-1655/TP2
	HIGH LOAD	6.2	6.7	7.2	V	701-1655/TP4
	LOW LOAD	6.2	6.7	7.2	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	7.5	8.0	8.5	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 88.*
2. *Load RAM with hex 01 for Family 87.*
3. *Photo 8 shows reject count.*

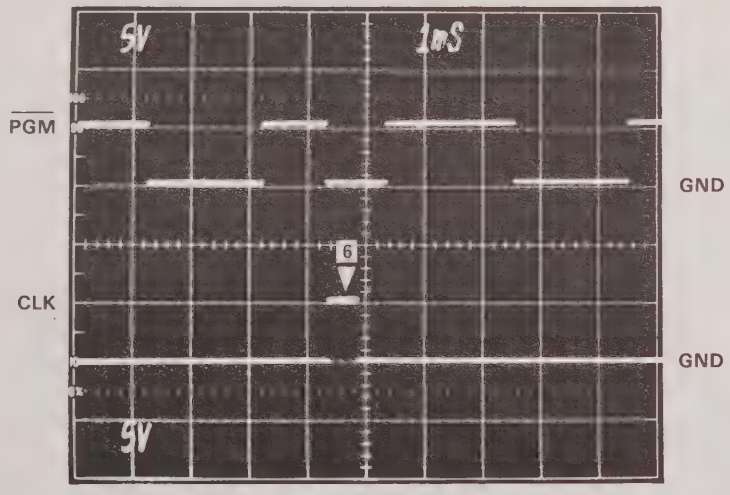
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

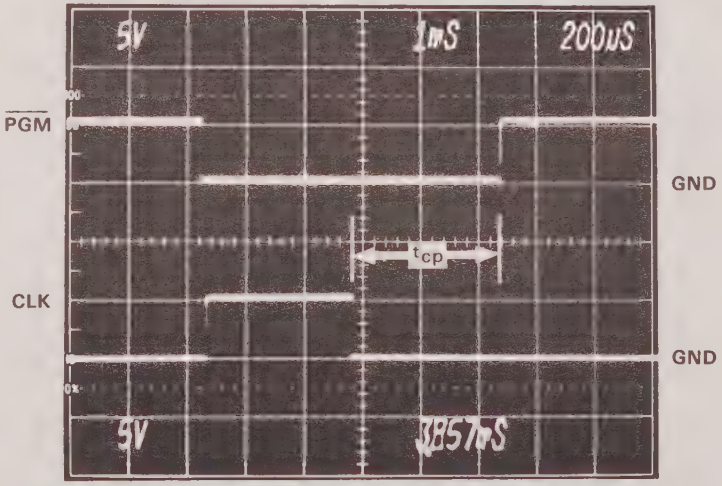
TIMING DIAGRAM

FAMILY CODES 87, 88

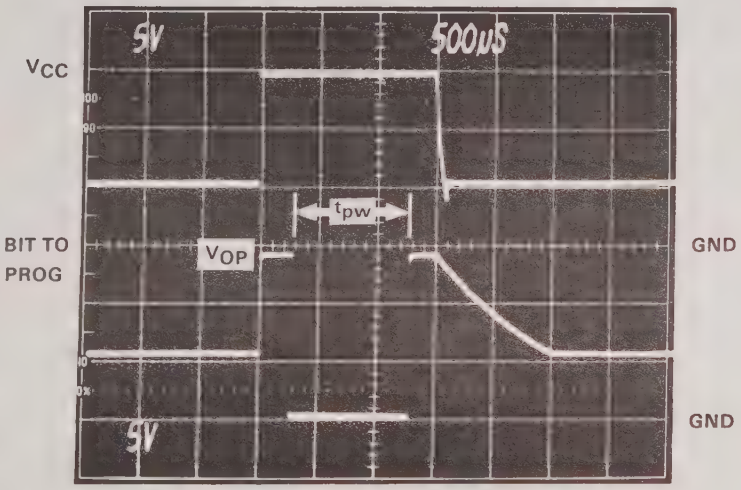
DATA I/O


5V
1mS
PGM
GND
6
CLK
GND
5V

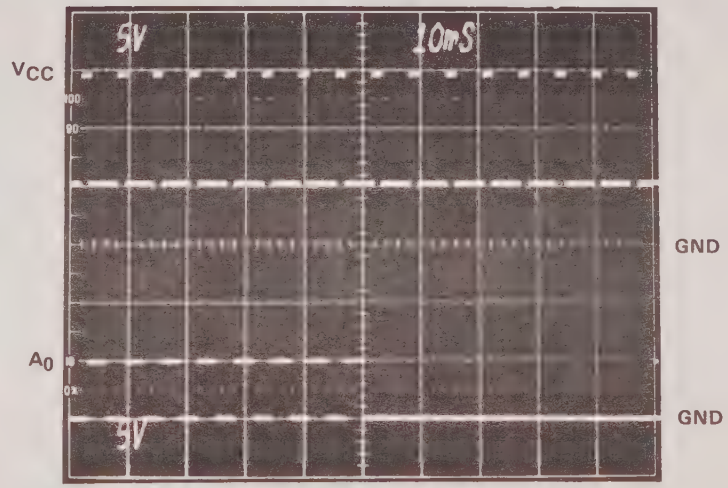
5


5V
1mS
200µS
PGM
GND
tcp
CLK
GND
5V
3857mS

6


5V
500µS
VCC
tpw
BIT TO
PROG
VOP
GND
GND
5V

7


5V
10mS
VCC
GND
A0
GND
5V

8

B-167
10-950-0059

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

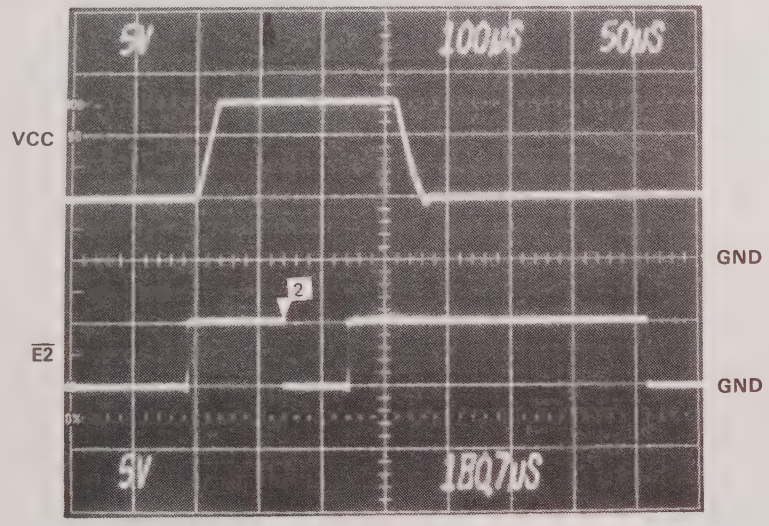
Sheet 2 of 2

TIMING DIAGRAM

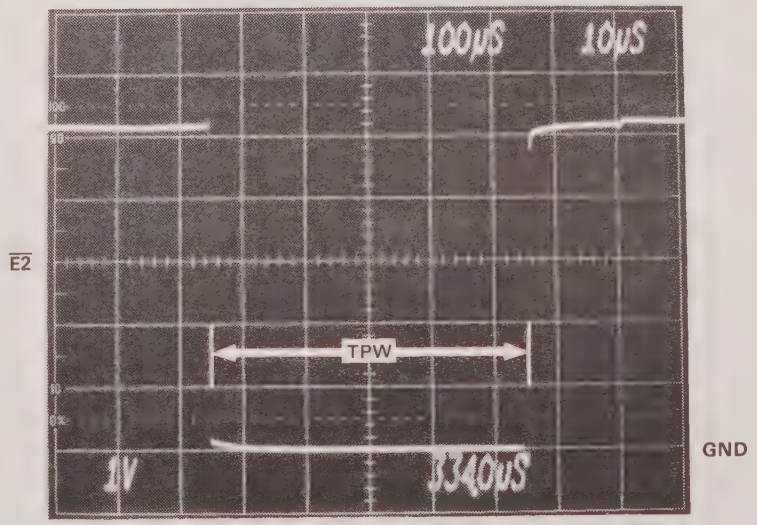
FAMILY CODES 87, 88

DATA I/O

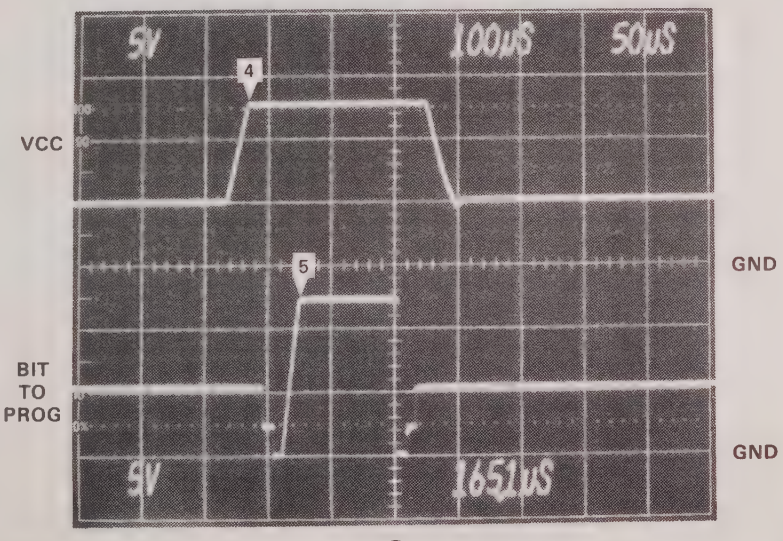
0526/1282


5V
100µS
50µS
VCC
GND
2
E2
GND
5V
1807µS

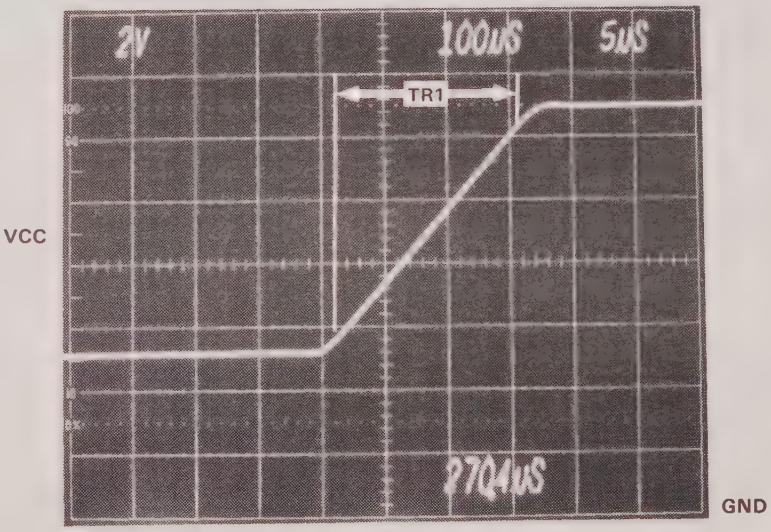
1


100µS
10µS
E2
TPW
GND
1V
3340µS

2


5V
100µS
50µS
4
VCC
GND
5
BIT
TO
PROG
GND
5V
1651µS

3


2V
100µS
5µS
TR1
VCC
GND
2704µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	12.5	12.5	13.0	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	11.5	12.0	12.5	V	
	TPW	40	50	60	µs	
	TR1	5		20	µs	
	TR2	10		20	µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	0.4	0.5	0.6	V	701-1655/TP2
	High Load	17.5	18.5	19.5	V	701-1655/TP4
	Low Load	17.5	18.5	19.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.3	2.4	2.5	V	701-1655/TP2
	High Load	6.0	7.0	8.0	V	701-1655/TP4
	Low Load	6.0	7.0	8.0	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family 91.*
2. *Load RAM with hex 01 for Family 92.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		CJZ	11/82
		ECN #4831		JCH	5/83
		ECN #5023		CJZ	3/84

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 91, 92

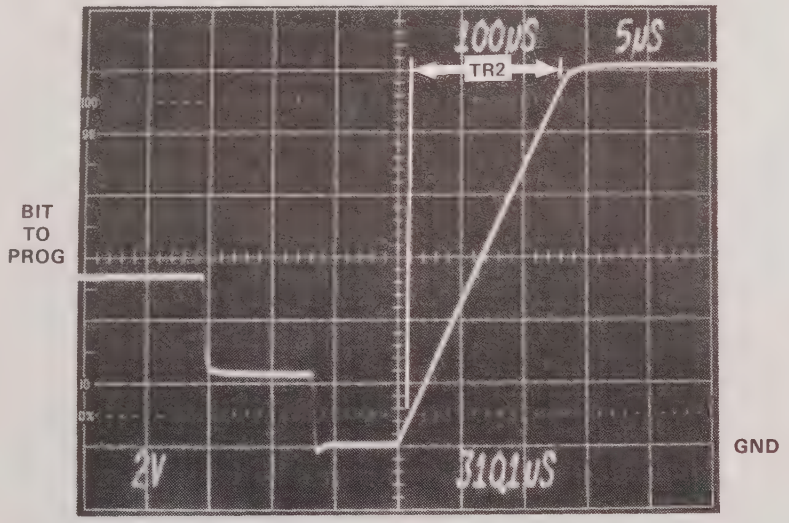
DRAWN BY:

CHECKED BY:

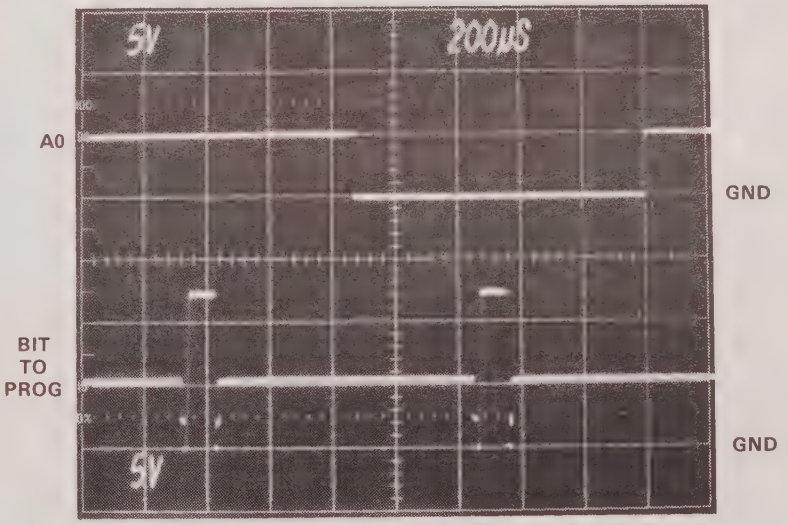
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1/2


100µS
5µS
TR2
BIT
TO
PROG
2V
GND

5


5V
200µS
A0
GND
BIT
TO
PROG
5V
GND

6

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.Z.	11/82
		ECN #4831		[illegible]	5/83

DATA I/O ISSAQUAH, WA

TITLE: TIMING DIAGRAM

FAMILY CODES 91, 92

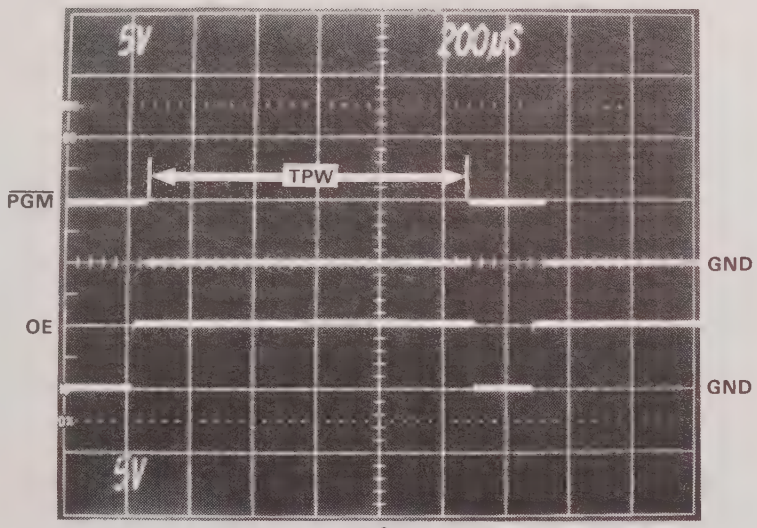
DRAWN BY: [illegible]

CHECKED BY:

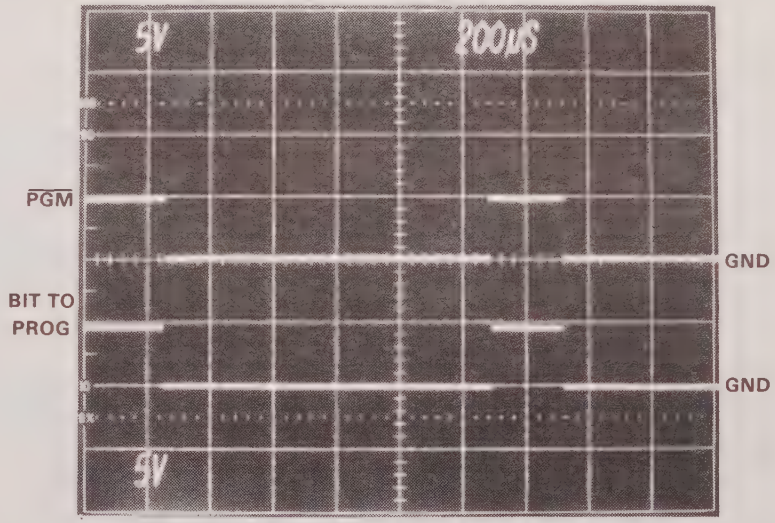
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

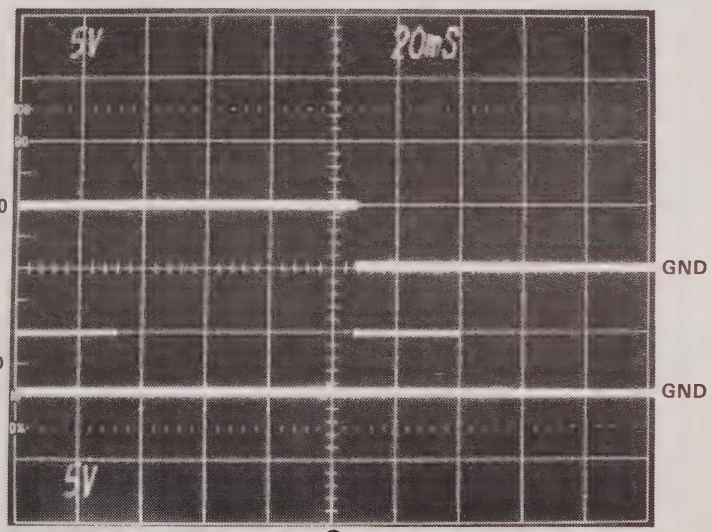
SHEET 2/2


5V
200µS
TPW
PGM
GND
OE
GND
5V

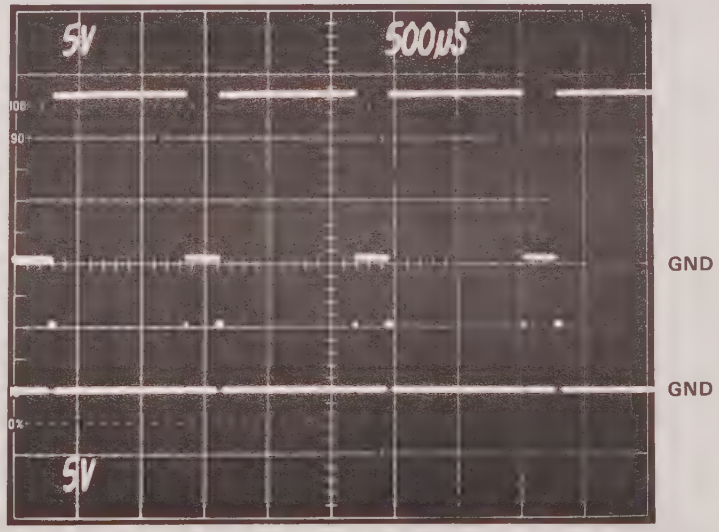
1


5V
200µS
PGM
GND
BIT TO
PROG
GND
5V

2


5V
20mS
A0
GND
BIT TO
PROG
GND
5V

3


5V
500µS
VPP
GND
PE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.00	6.25	V	Not shown
	VOP					NA
	VPP	12.2	12.5	12.8	V	Not shown
	VPPV					NA
	TPW	0.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		25		Pulses	
	Overprogram		1		Pulse	See note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

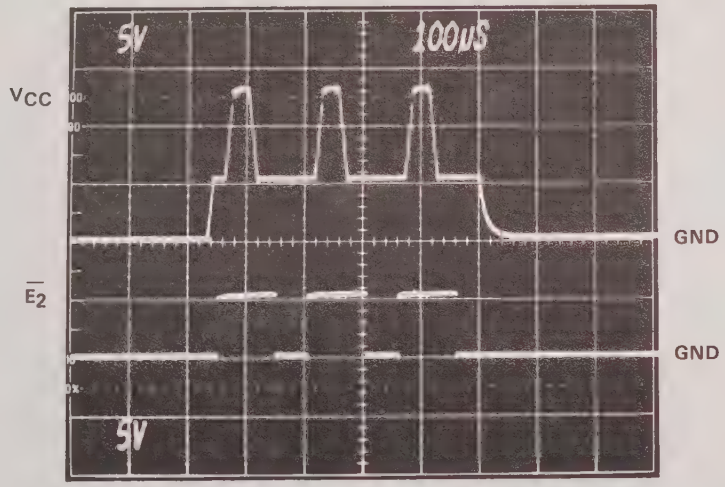
1. *Load RAM with hex FE for Family 93.*
2. *Load RAM with hex 01 for Family 94, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 3 ms times the number of programming pulses required to program the location.*
4. *Photo 4 is for Pinout 24.*

REVISIONS

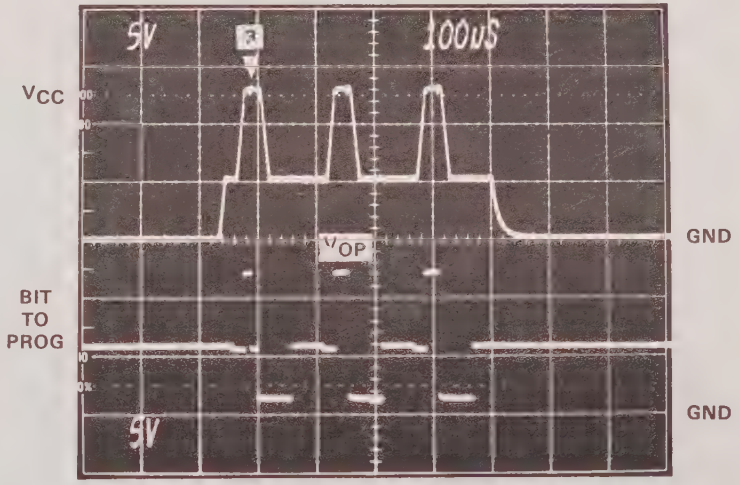
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		C73	3/84

DATA I/O

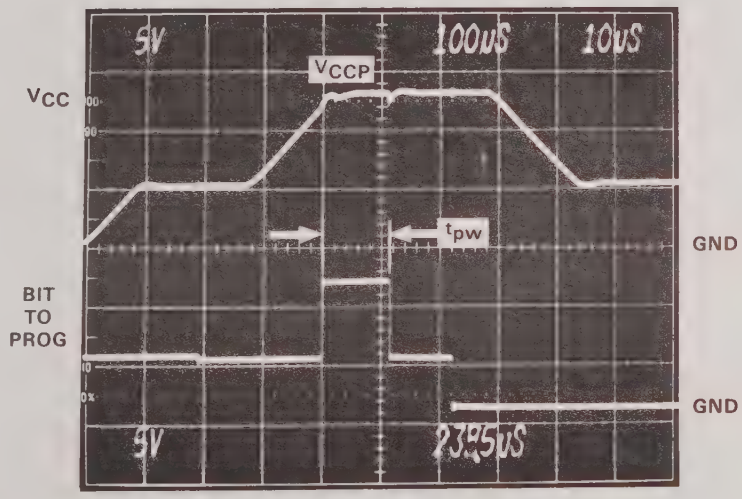
TITLE: TIMING DIAGRAM FAMILY CODES 93, 94		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 1


5V
100uS
VCC
GND
$\overline{E_2}$
GND
5V

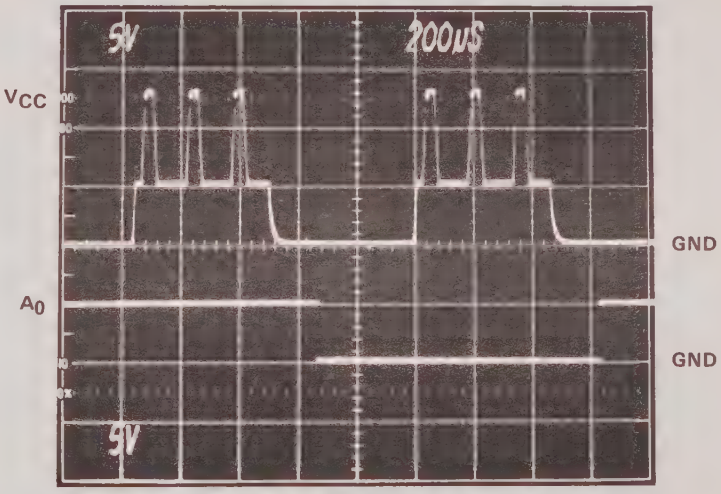
1


5V
100uS
VCC
GND
VOP
BIT
TO
PROG
GND
5V

2


5V
100uS
10uS
VCC
VCCP
GND
tpw
BIT
TO
PROG
GND
5V
23.5uS

3


5V
200uS
VCC
GND
A0
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	12.0	12.5	13.0	V	
	V_{OP}	11.5	12.0	12.5	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	10	11	12	μs	See note 5
	t_r					N.A.
	t_f					N.A.
	Reject		3		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	0.7	0.8	0.9	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	16.9	17.4	17.9	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	18.5	19.0	19.5	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family A1.*
2. *Load RAM with hex 01 for Family A2.*
3. *Load V_{CC} with 100Ω, 2W resistor.*
4. *Load "Bit to Program" with 3.3KΩ, ¼W resistor.*
5. *First pulse TPW equals 11 µs; pulses 2 and 3 are equal to 22 µs.*

REVISIONS

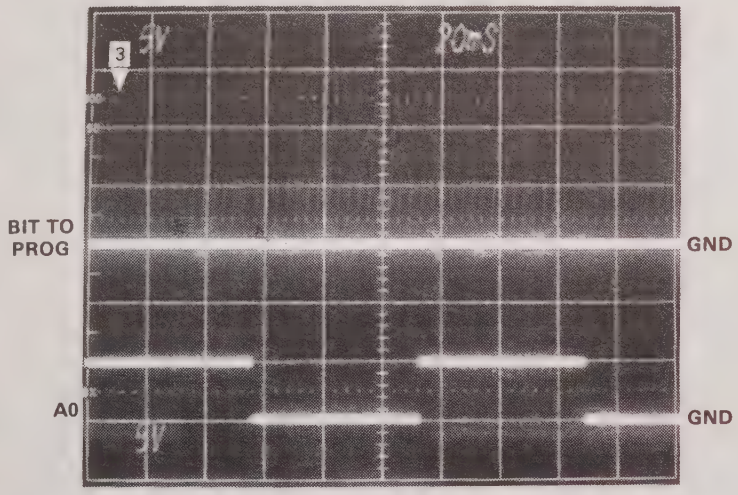
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

Sheet 1 of 1

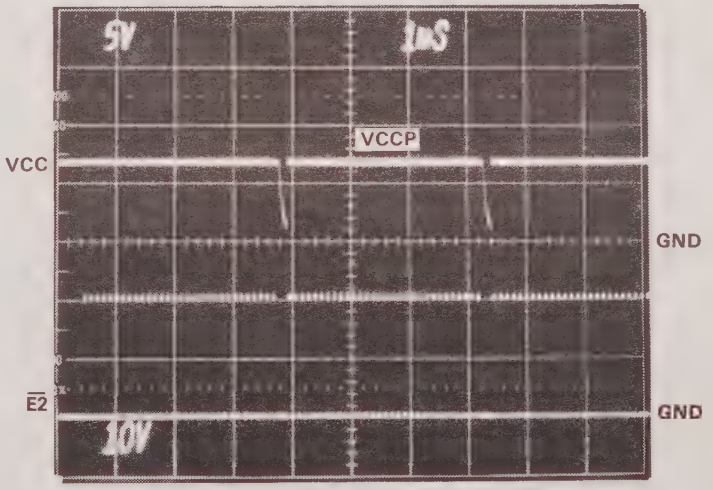
TIMING DIAGRAM

FAMILY CODES A1, A2

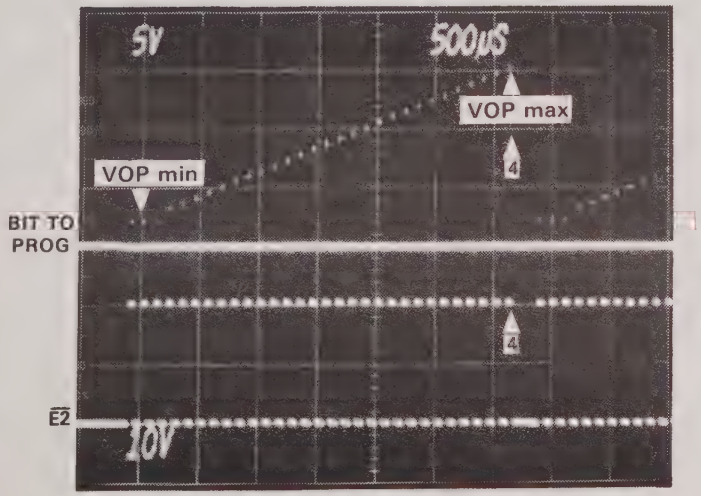
DATA I/O


5V
20mS
3
BIT TO PROG
GND
A0
GND
5V

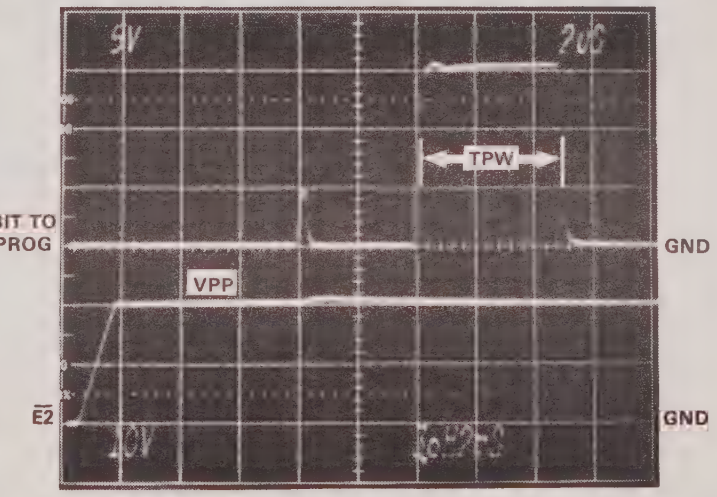
1


5V
1mS
VCCP
VCC
GND
E2
GND
10V

2


5V
500uS
VOP max
VOP min
4
BIT TO PROG
4
E2
10V

3


5V
2uS
TPW
BIT TO PROG
GND
VPP
E2
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	6.3	6.5	6.7	V	
	VPP	19.5	20.0	20.5	V	
	VOP max	15 5	16.0	16.5	V	See note 2
	VOP min	1 5	2.0	2.5	V	See note 2
	TPW	4.0	5.0	6.0	µs	
	Reject		16		Series	See note 3
	Overprogram		1		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	1 4	1.5	1.6	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	17.2	18.2	19.2	V	701-1655/TP3
2ND PASS VERIFY	VCC	5 4	5.5	5.6	V	
	VREF	1 4	1.5	1.6	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	17 2	18.2	19.2	V	701-1655/TP3

NOTES

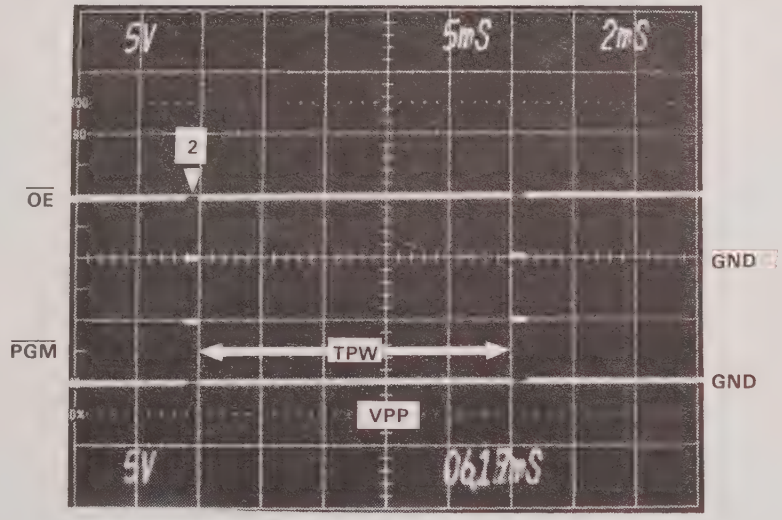
1. *Load RAM with hex FE for Family A3.*
2. *Load RAM with hex 01 for Family A4.*
3. *01 is loaded with a 100 Ω resistor. A series of program pulses is applied. The program pulses begin at VOP min and increase in magnitude to VOP max or until the bit programs.*
4. *Reject count is 16 program pulse series.*

REVISIONS

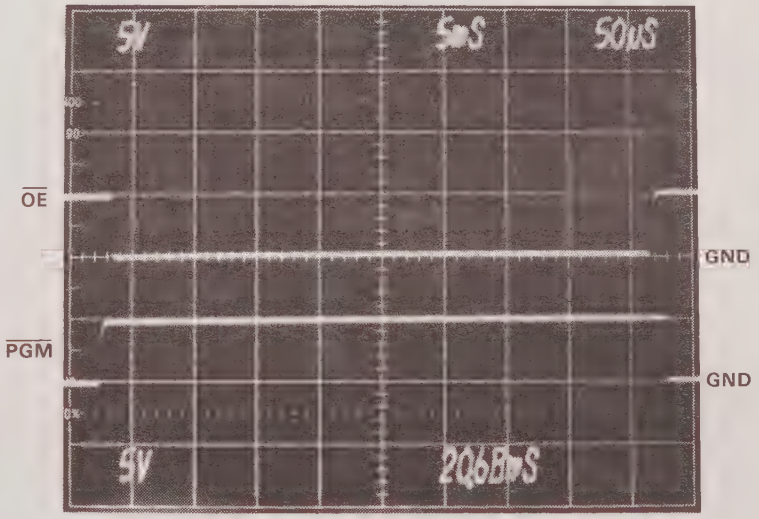
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release			
		ECN #4831		JCH	5 81
		ECN #5023		CTB	3/84

DATA I/O

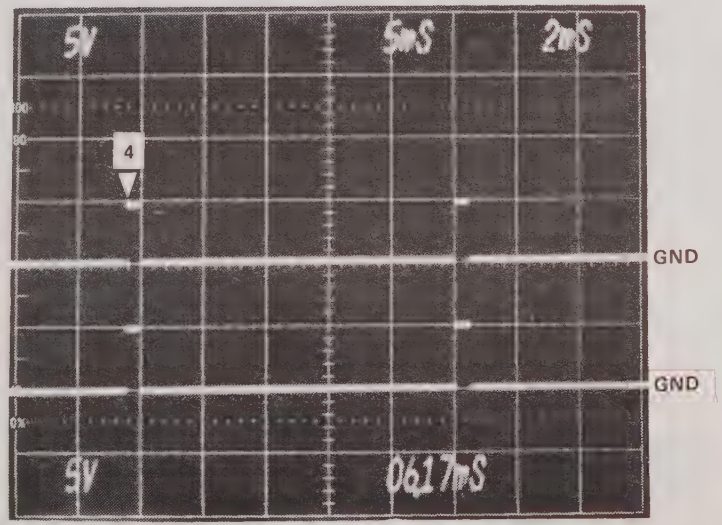
TITLE: TIMING DIAGRAM FAMILY CODES A3, A4		DRAWN BY:
		CHECKED BY: RH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 1


5V
5mS
2mS
2
OE
GND
PGM
TPW
GND
VPP
5V
0617mS

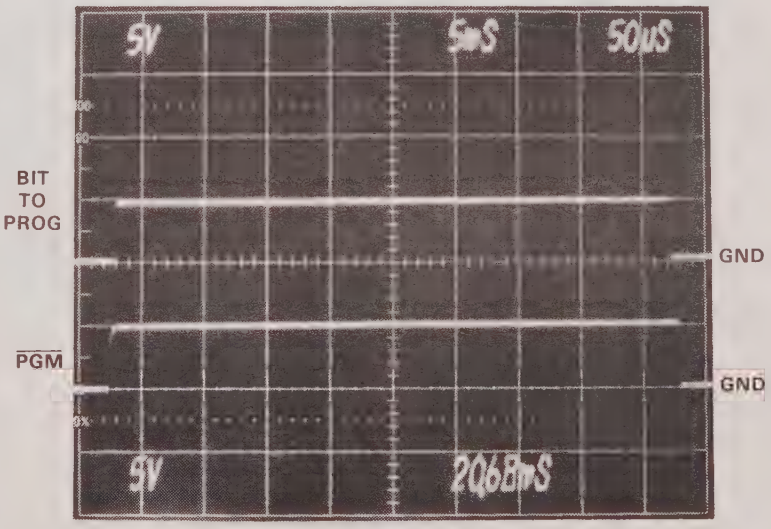
1


5V
5mS
50uS
OE
GND
PGM
GND
5V
206BmS

2


5V
5mS
2mS
4
BIT
TO
PROG
GND
PGM
GND
5V
0617mS

3


5V
5mS
50uS
BIT
TO
PROG
GND
PGM
GND
5V
206BmS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.5	5.0	5.5	V	
	VPP	0.0	0.0	0.8	V	
	VEE	12.0	14.5	21.0	V	
	TPW	5.0	10.0	15.0	ms	
	TR				NA	
	TF				NA	
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.5	4.6	4.7	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.5	5.5	6.5	V	701-1655/TP4
	Low Load	4.5	5.5	6.5	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.3	5.4	5.5	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.4	V	701-1655/TP4
	Low Load	6.8	7.8	8.8	V	701-1655/TP3

NOTES

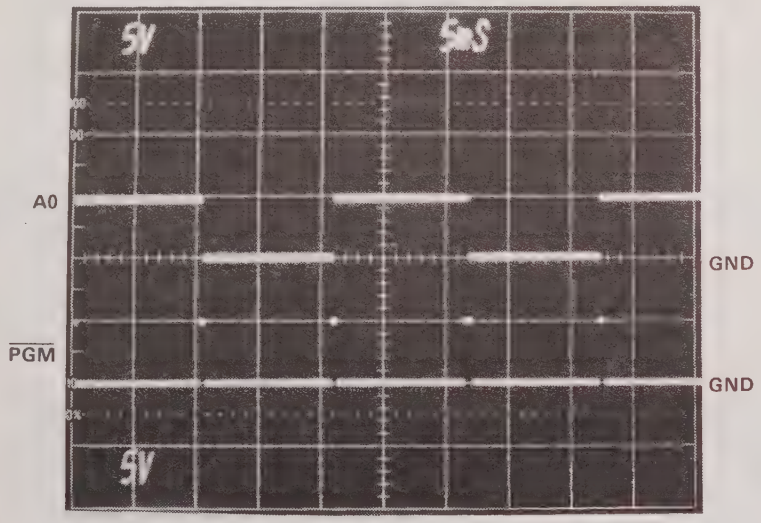
1. *Load RAM with hex FE for Family A5.*
2. *Load RAM with hex 01 for Family A6, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 6 and 7 are erase waveforms.*

REVISIONS

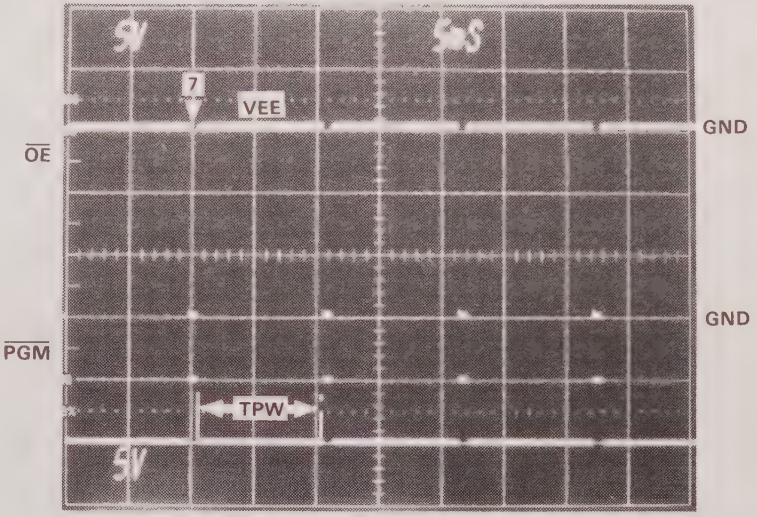
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.J.J.	11/82
		ECN #4831		JH	5/83
		ECN #5023		CJJ	3/84

DATA I/O ISSAQUAH, WA

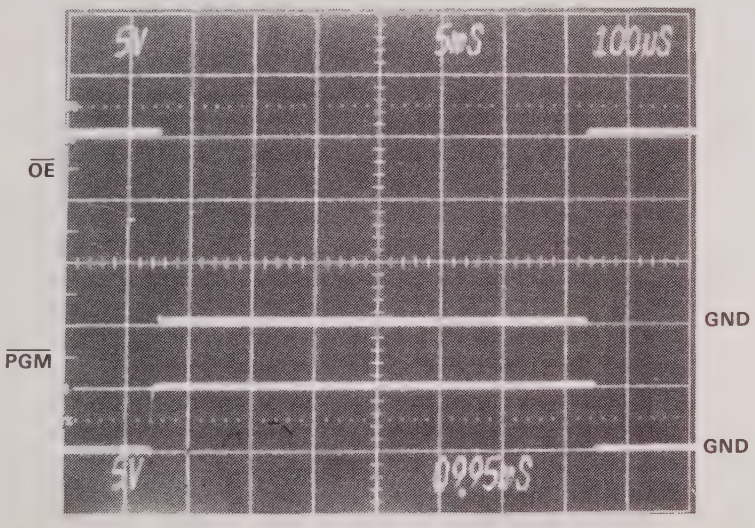
TITLE: TIMING DIAGRAM		DRAWN BY:
FAMILY CODES A5, A6		CHECKED BY: ZH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1/2


5V
5μS
A0
GND
PGM
GND
5V

5


5V
5μS
7
VEE
GND
OE
GND
PGM
TPW
5V

6

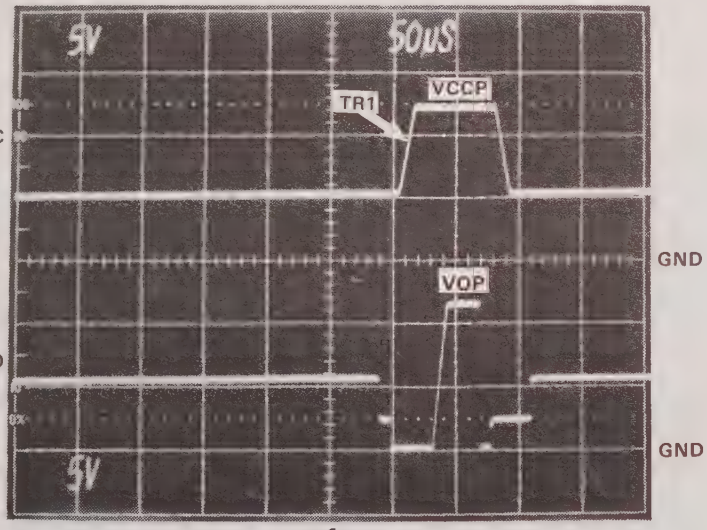

5V
5μS
100μS
OE
GND
PGM
GND
5V
0.95μS

7

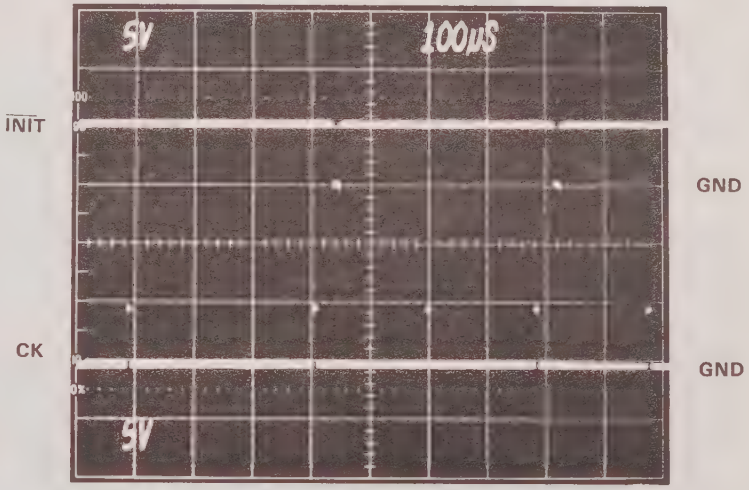
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		Release		C.T.J.	11/82
		ECN #4831		XX	5/83
		ECN #5023		CTJ	3/84

DATA I/O ISSAQUAH, WA

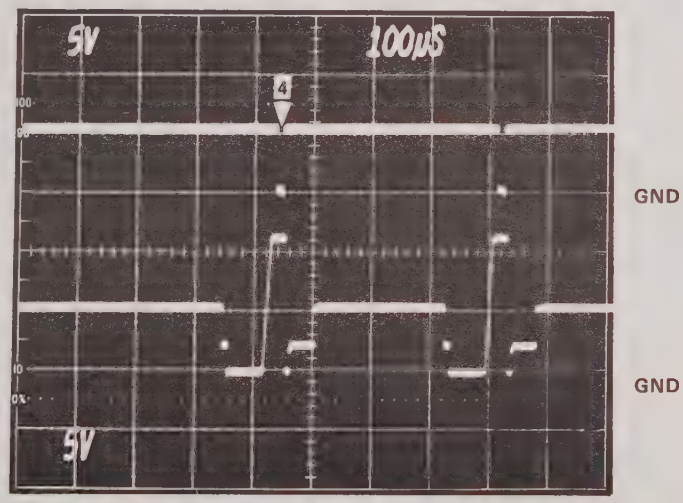
TITLE: TIMING DIAGRAM FAMILY CODES A5, A6		DRAWN BY: [illegible] CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2/2


5V
50µS
TR1
VCCP
VCC
GND
VOP
BIT TO PROG
GND
5V

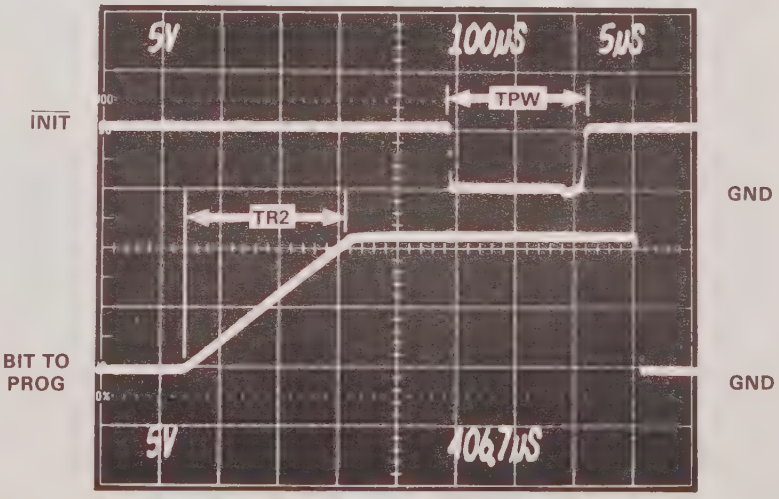
1


5V
100µS
INIT
GND
CK
GND
5V

2


5V
100µS
4
INIT
GND
BIT TO PROG
GND
5V

3


5V
100µS
5uS
TPW
INIT
GND
TR2
BIT TO PROG
GND
5V
106.7µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.6	11.8	12.0	V	
	VOP	10.5	11.0	11.5	V	
	VPP					NA
	VPPV					NA
	TPW	9.0	10.0	11.5	μs	
	TR1	1.0		20.0	μs	See note 3
	TR2	1.0		15.0	μs	
	TF					NA
	Reject		10		Pulses	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	3.4	3.5	3.6	V	701-1655/TP2
	High Load	8.3	9.3	10.3	V	701-1655/TP4
	Low Load	8.3	9.3	10.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family A9.*
2. *Load RAM with hex 01 for Family AA.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		YH	5/83
		ECN #5023		CTZ	3/84

DATA I/O

TITLE: TIMING DIAGRAM

FAMILY CODES A9, AA

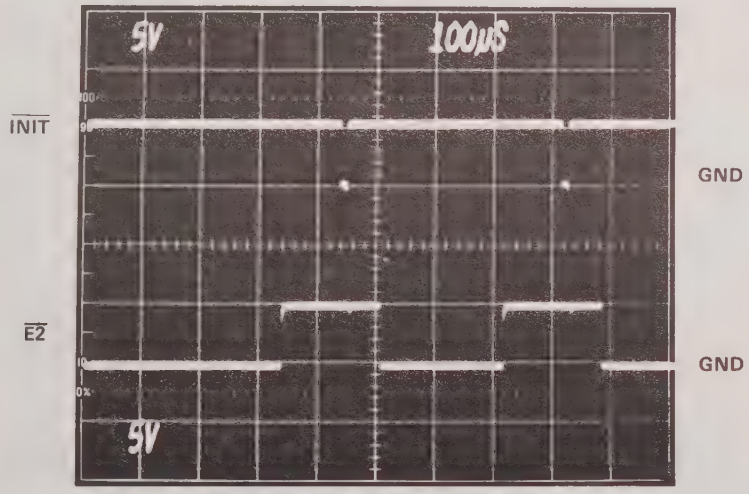
DRAWN BY:

CHECKED BY: YH

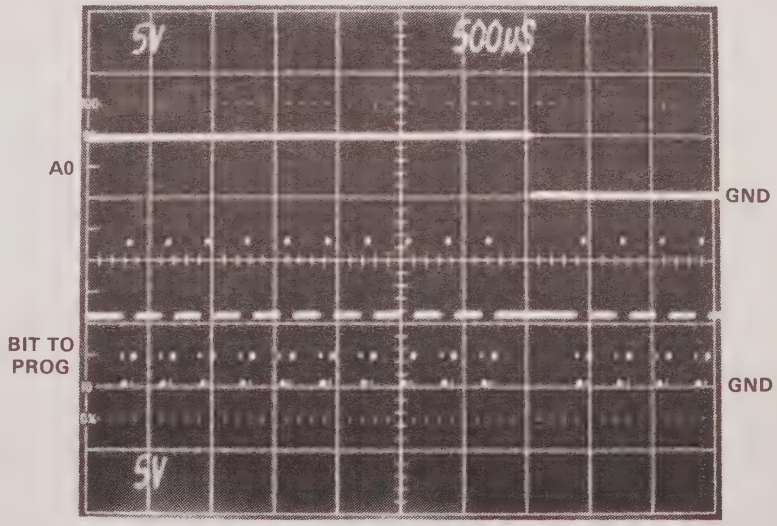
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

SCALE

SHEET 1 of 2



5



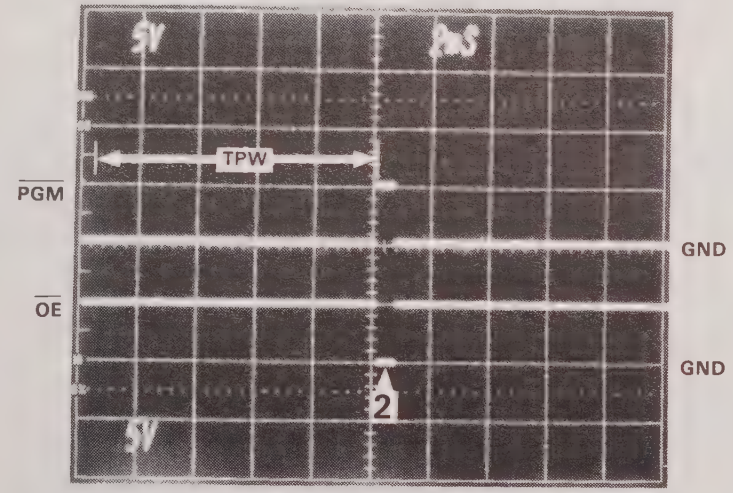
6

REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		CH	5/83
		ECN #5023		CZB	3/84

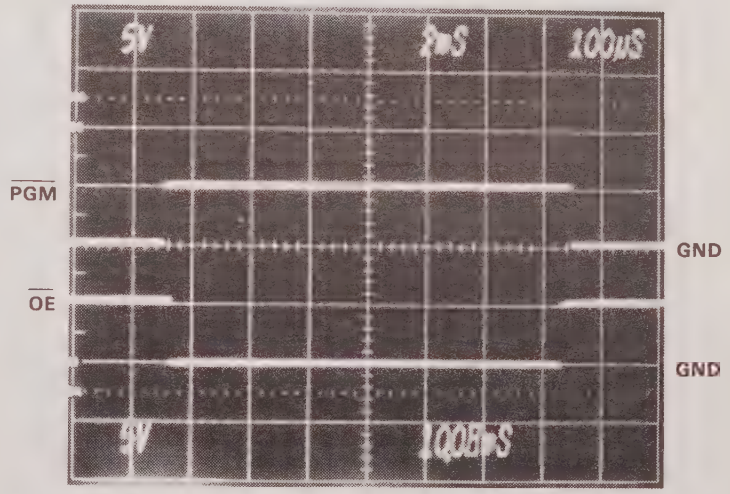
DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES A9, AA		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2

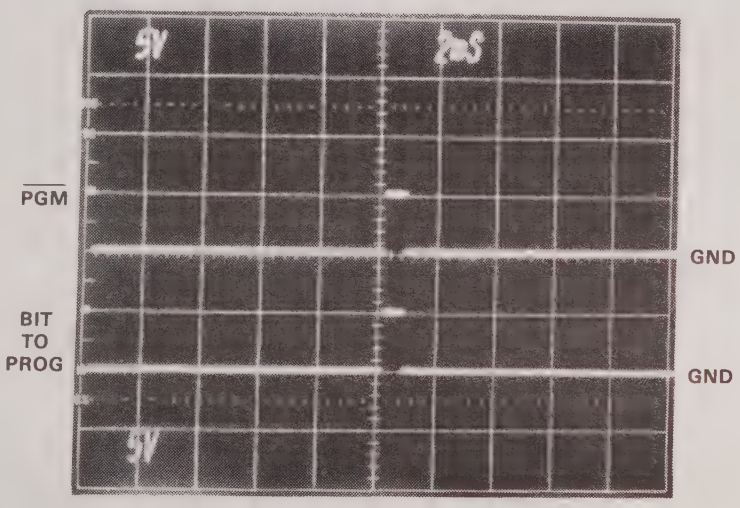
B-185
10-950-0059


5V
2mS
TPW
PGM
GND
OE
GND
2
5V

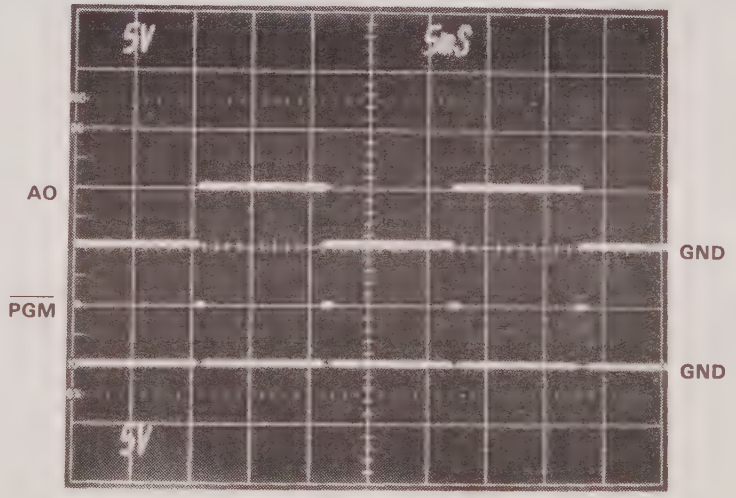
1


5V
2mS
100µS
PGM
GND
OE
GND
5V
100µS

2


5V
2mS
PGM
GND
BIT
TO
PROG
GND
5V

3


5V
5mS
AO
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	5.0	5.5	6.0	V	701-1655/TP4
	LOW LOAD	5.0	5.5	6.0	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	7.3	7.8	8.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family AB.*
2. *Photos 5 to 8 are chip erase waveforms.*

REVISIONS

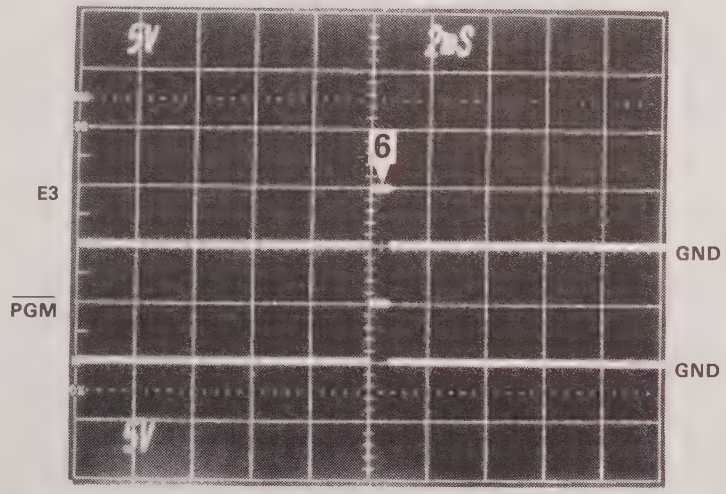
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/87

Sheet 1 of 2

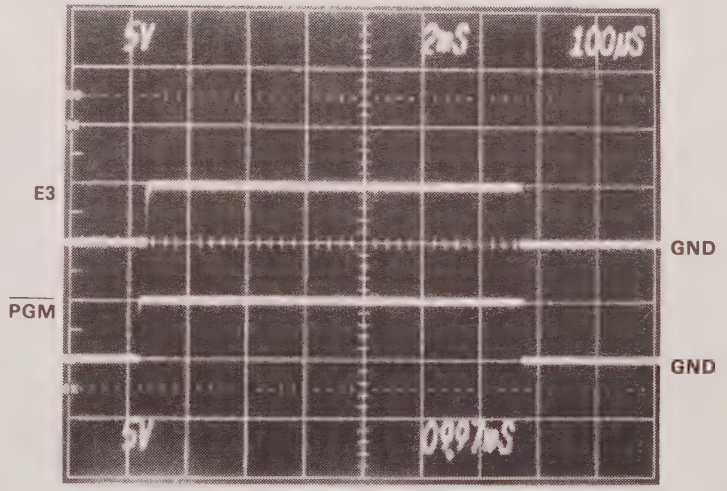
TIMING DIAGRAM

FAMILY CODES AB, AC

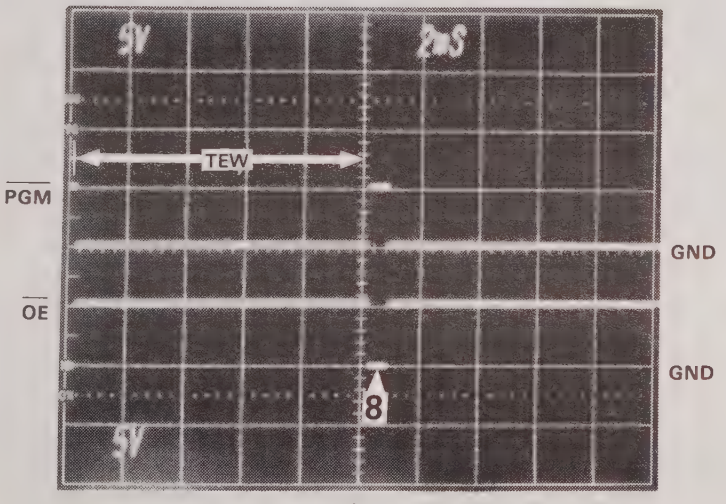
DATA I/O


5V
2mS
6
E3
GND
PGM
GND
5V

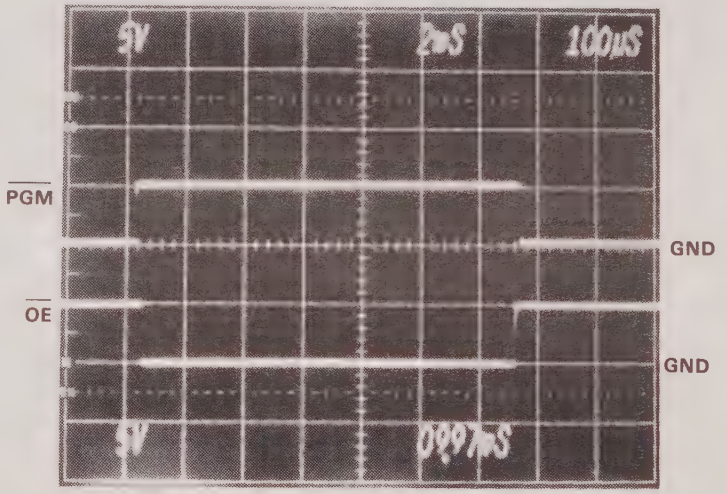
5


5V
2mS
100µS
E3
GND
PGM
GND
5V

6


5V
2mS
TEW
PGM
GND
OE
GND
8
5V

7


5V
2mS
100µS
PGM
GND
OE
GND
5V

8

B-189
10-950-0059

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	C73	3/84

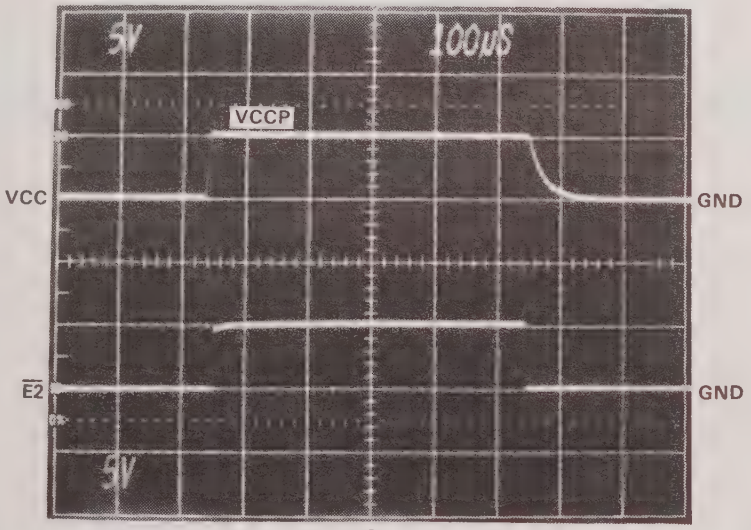
Sheet 2 of 2

TIMING DIAGRAM

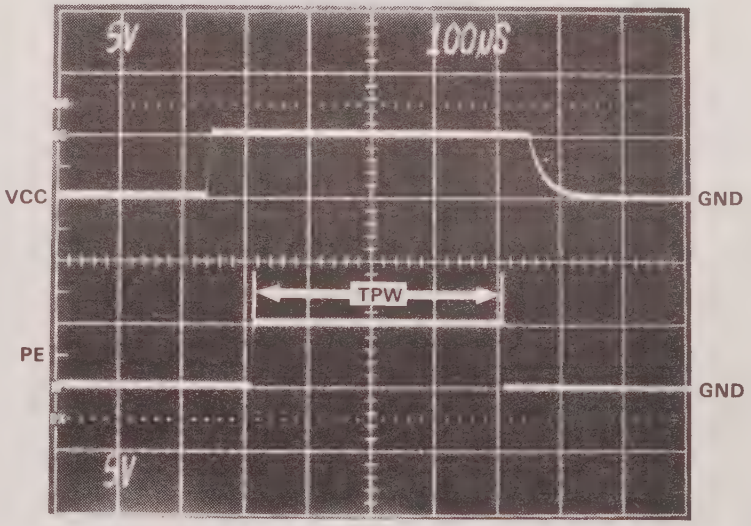
FAMILY CODES AB, AC

DATA I/O

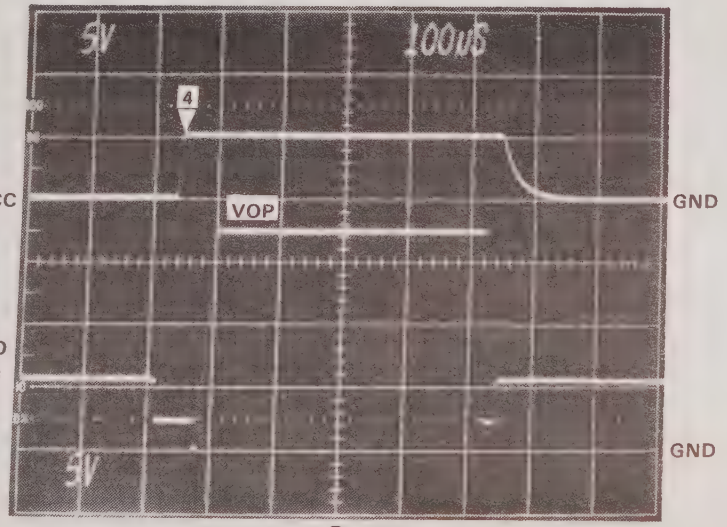
0526/1282


5V
100uS
VCCP
VCC
GND
E2
GND
5V

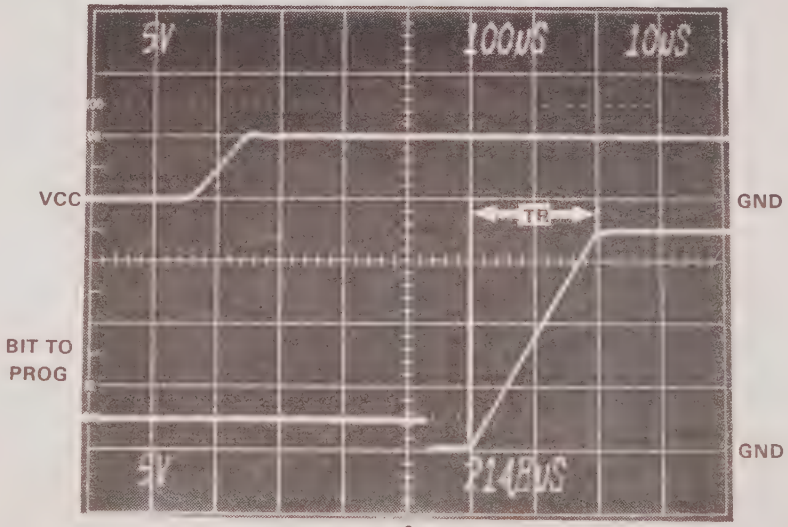
1


5V
100uS
VCC
GND
TPW
PE
GND
5V

2


5V
100uS
4
VCC
VOP
GND
BIT TO
PROG
GND
5V

3


5V
100uS
10uS
VCC
GND
TR
BIT TO
PROG
GND
5V
P14.8uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	
	VOP	16.0	17.0	18.0	V	
	VPP					NA
	VPPV					NA
	TPW	300	400	500	µs	
	TR	10		50	µs	
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.4	4.5	4.6	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	1.4	1.5	1.6	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.6	5.1	5.6	V	701-1655/TP3

NOTES

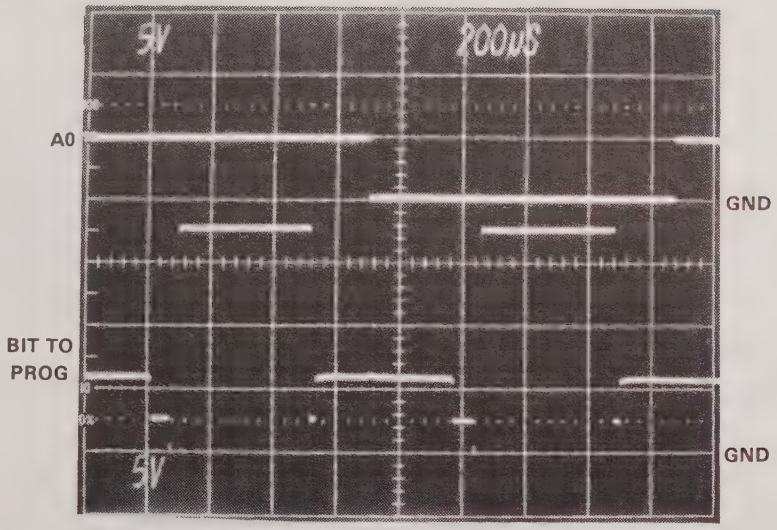
1. *Load RAM with hex FE for Family AD.*
2. *Load RAM with hex 01 for Family AE.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

REVISIONS

ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		C78	3/84

DATA I/O

TITLE: TIMING DIAGRAM FAMILY CODES AD, AE	DRAWN BY:	
	CHECKED BY: XH	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 2

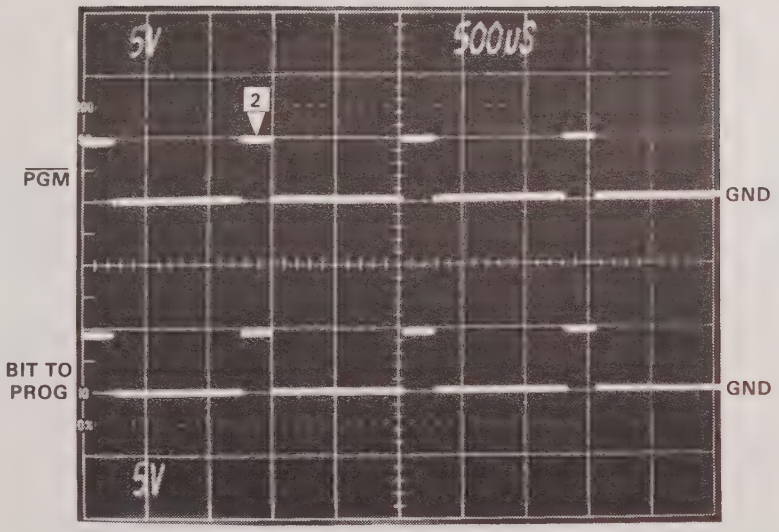


5

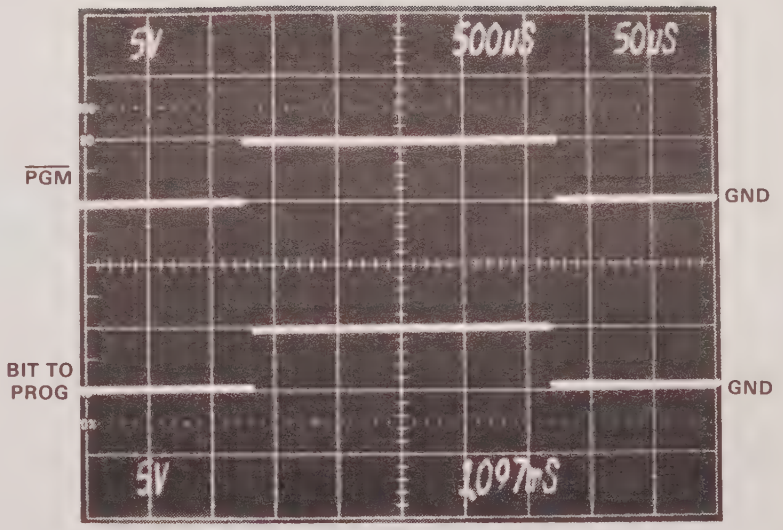
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		CTJ	3/84

DATA I/O

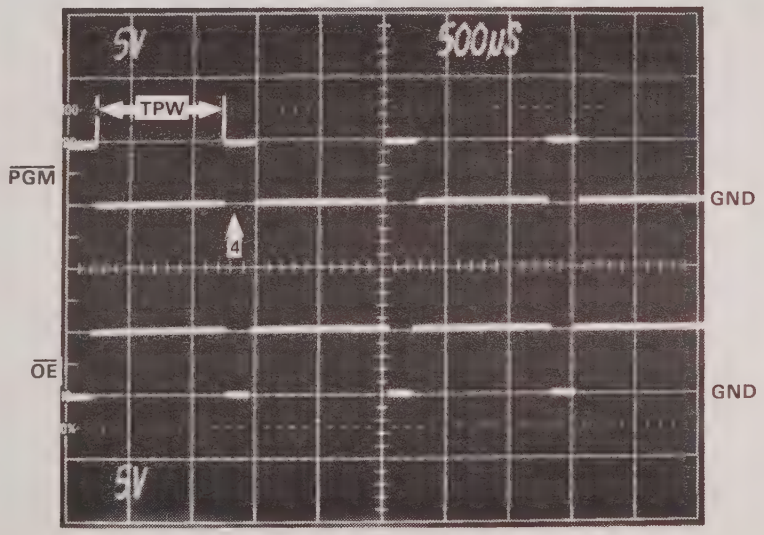
TITLE: TIMING DIAGRAM FAMILY CODES AD, AE		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


5V
500uS
2
PGM
GND
BIT TO PROG
GND
5V

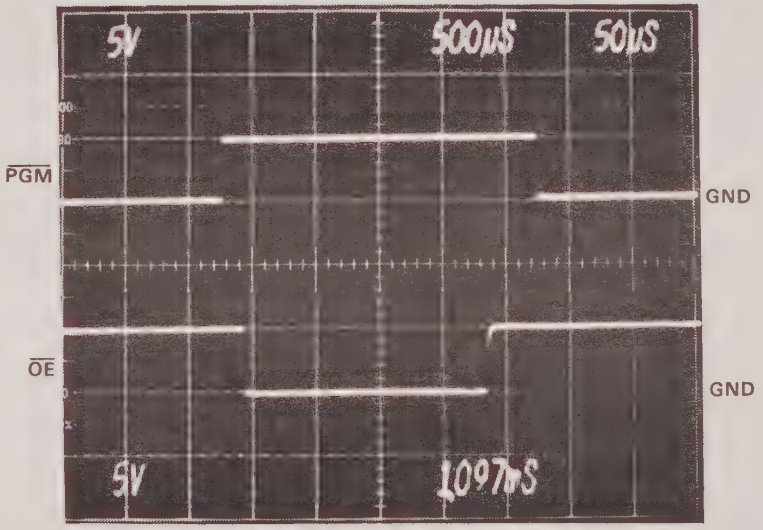
1


5V
500uS
50uS
PGM
GND
BIT TO PROG
GND
5V
1.097mS

2


5V
500uS
TPW
PGM
GND
4
OE
GND
5V

3


5V
500uS
50uS
PGM
GND
OE
GND
5V
1.097mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	21.0	21.5	22.0	V	Not shown
	V_{PPV}					N.A.
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSE	
	Overprogram		1		PULSE	See note 3
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family AF.*
2. *Load RAM with hex 01 for Family BO and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 2 ms long; see photos 6 and 7.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTB	3/84

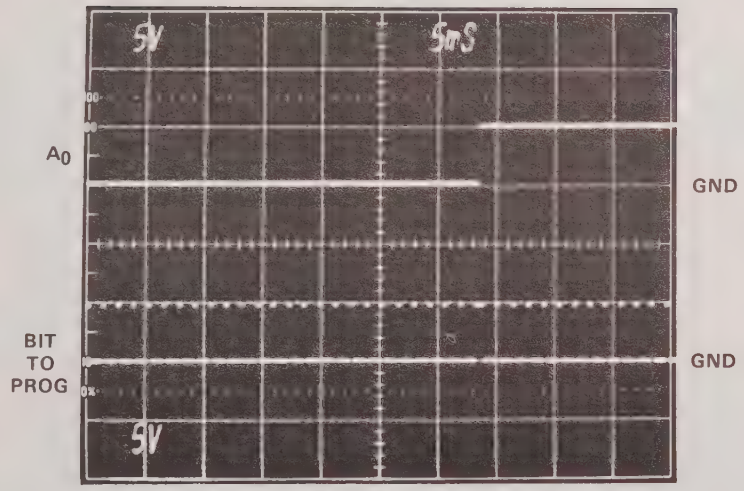
Sheet 1 of 2

TIMING DIAGRAM

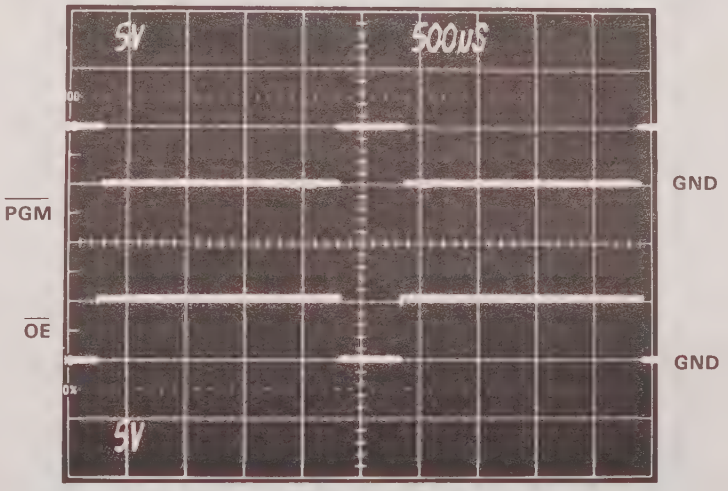
FAMILY CODES AF, BO

DATA I/O

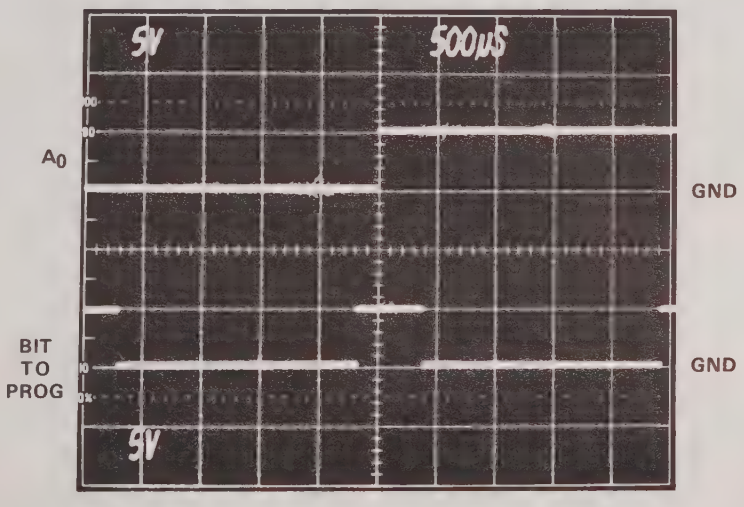
0526/1282


5V
5mS
A0
GND
BIT
TO
PROG
GND
5V

5


5V
500uS
GND
PGM
OE
GND
5V

6


5V
500uS
A0
GND
BIT
TO
PROG
GND
5V

7

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10-950-0059

REVISIONS

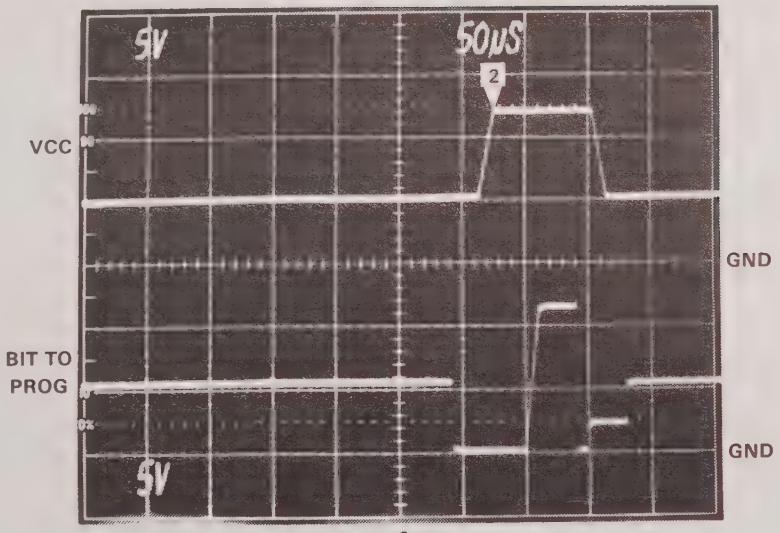
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

Sheet 2 of 2

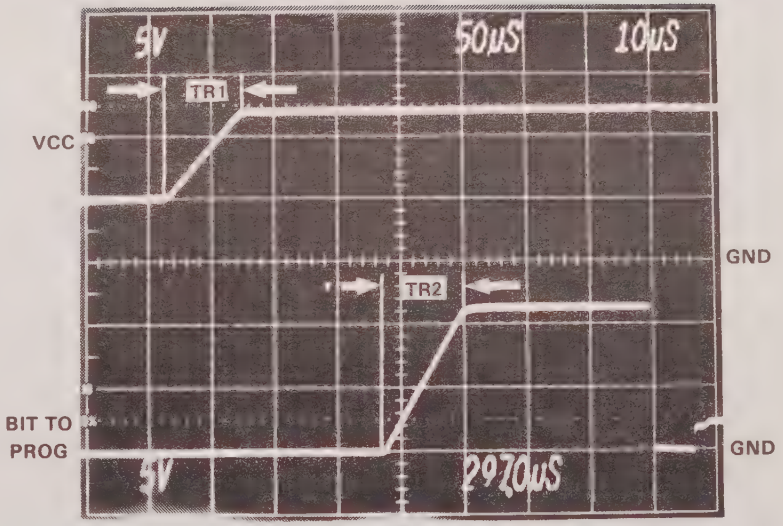
TIMING DIAGRAM

FAMILY CODES AF, BO

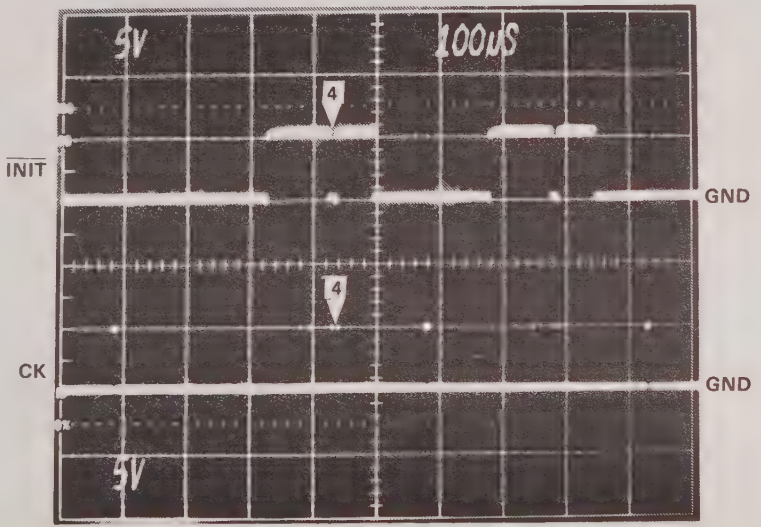
DATA I/O


5V
50µS
2
VCC
GND
BIT TO
PROG
GND
5V

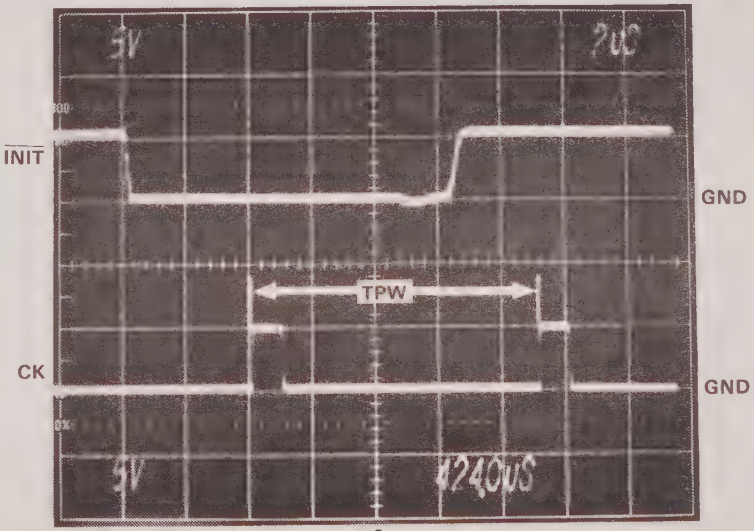
1


5V
50µS
10µS
TR1
VCC
GND
TR2
BIT TO
PROG
GND
5V
2970µS

2


5V
100µS
4
INIT
GND
4
CK
GND
5V

3


5V
7µS
INIT
GND
TPW
CK
GND
5V
4240µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.6	11.8	12.0	V	
	VOP	10.5	11.0	11.5	V	
	VPP					NA
	VPPV					NA
	TPW	9.0	10.0	11.5	µs	
	TR1	1.0		20.0	µs	See note 3
	TR2	1.0		15.0	µs	
	TF					NA
	Reject		10		Pulses	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1655/TP2
	High Load	7.0	8.0	9.0	V	701-1655/TP4
	Low Load	7.0	8.0	9.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	3.4	3.5	3.6	V	701-1655/TP2
	High Load	8.3	9.3	10.3	V	701-1655/TP4
	Low Load	8.3	9.3	10.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family B1.*
2. *Load RAM with hex 01 for Family B2.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

REVISIONS

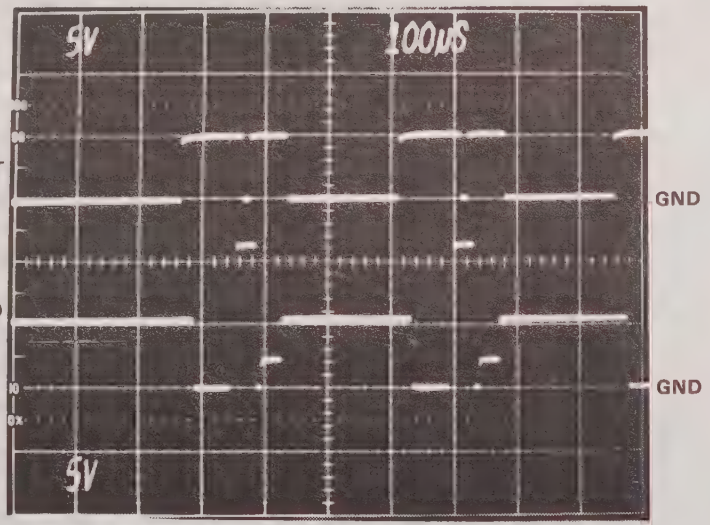
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/8/3
		ECN #5023		CTJ	3/24

DATA I/O

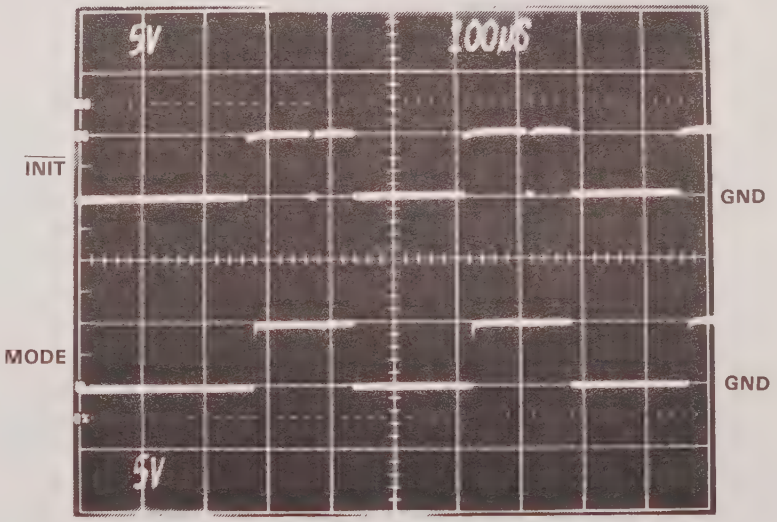
TITLE	DRAWN BY:
TIMING DIAGRAM FAMILY CODES B1, B2	CHECKED BY: XH

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	33-950-0059

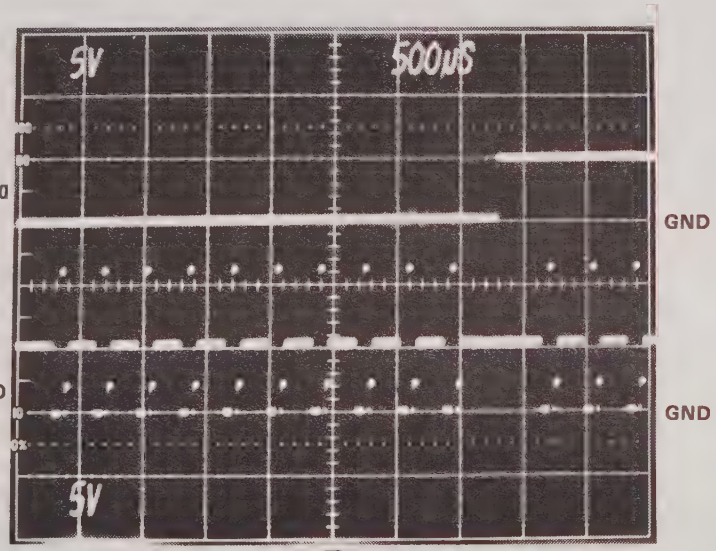
SCALE | SHEET 1 of 2


5V
100uS
INIT
GND
BIT TO
PROG
GND
5V

5


5V
100uS
INIT
GND
MODE
GND
5V

6


5V
500uS
A0
GND
BIT S TO
PROG
GND
5V

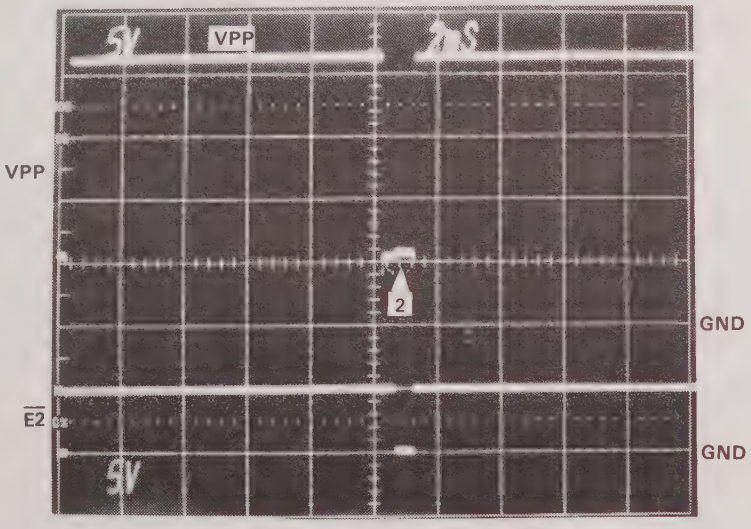
7

B-201
10-950-0059

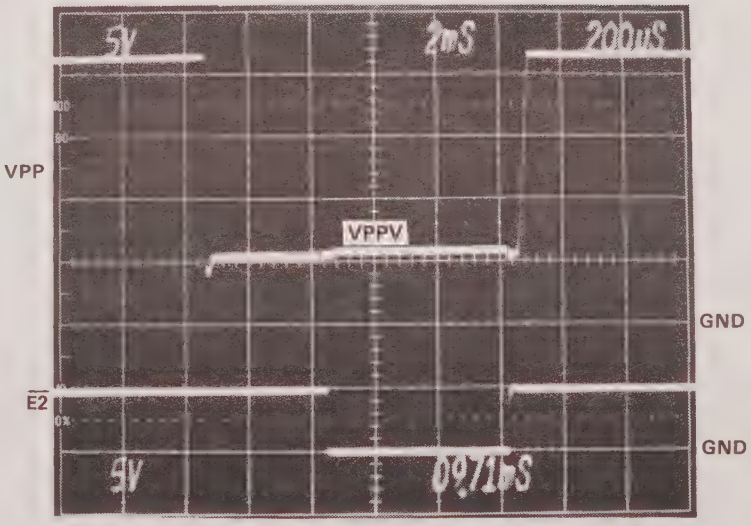
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		CTZ	3/84

DATA I/O

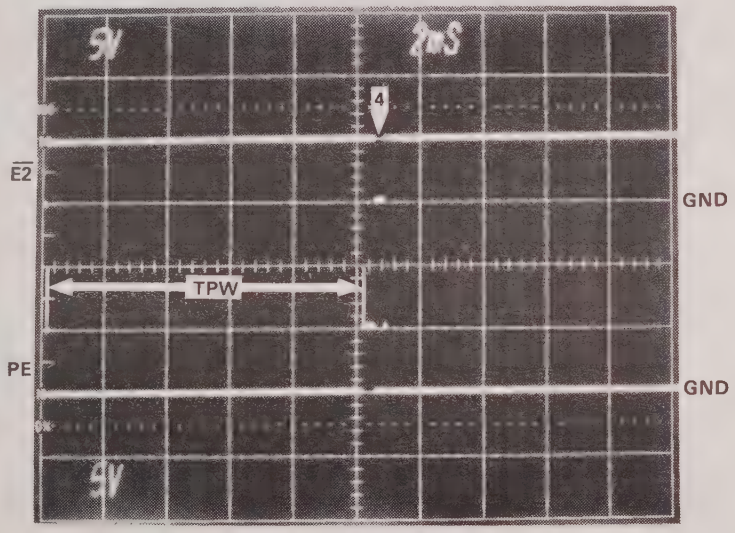
TITLE: TIMING DIAGRAM FAMILY CODES B1, B2		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 2


5V
VPP
2mS
VPP
2
GND
E2
GND
5V

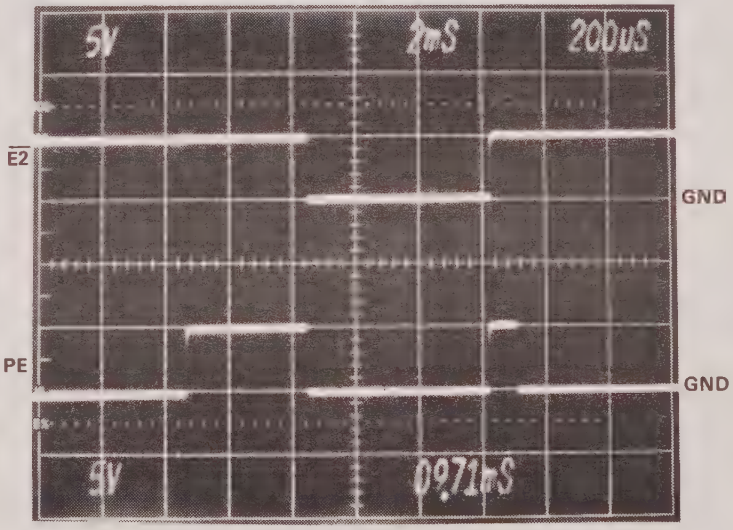
1


5V
2mS
200uS
VPP
VPPV
GND
E2
GND
5V
0971uS

2


5V
2mS
4
E2
GND
TPW
PE
GND
5V

3


5V
2mS
200uS
E2
GND
PE
GND
5V
0971mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	VEE	9.0	12.0	15.0	V	
	TPW	9.0		15.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

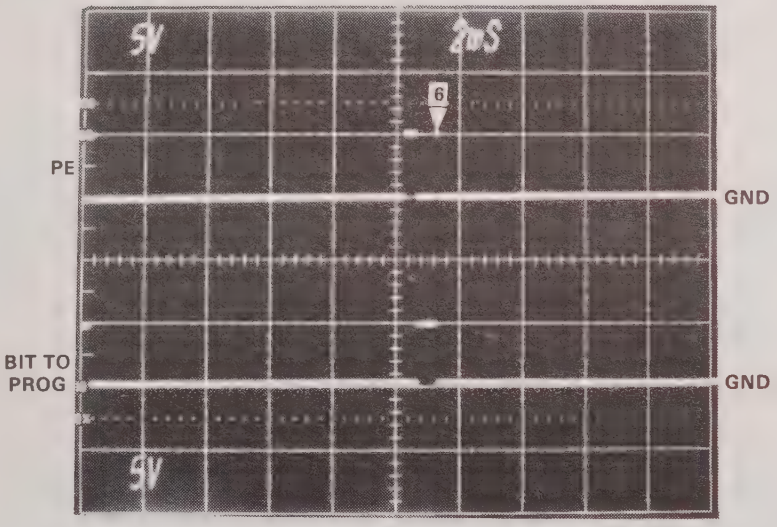
1. *Load RAM with hex FE for Family B3.*
2. *Load RAM with hex 01 for Family B4 and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Chip erase waveforms are photos 8 and 9.*
4. *Byte erase waveforms are photos 10 and 11.*

REVISIONS

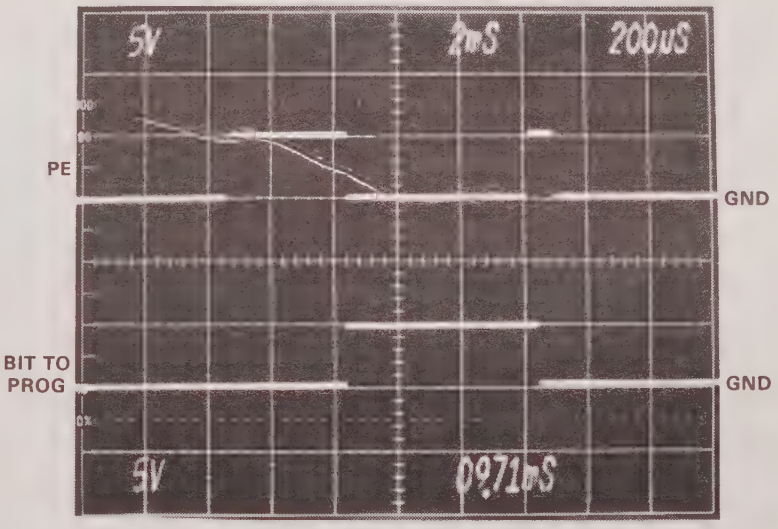
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		JCA	5/83
		ECN #5023		CTJ	3/84

DATA I/O

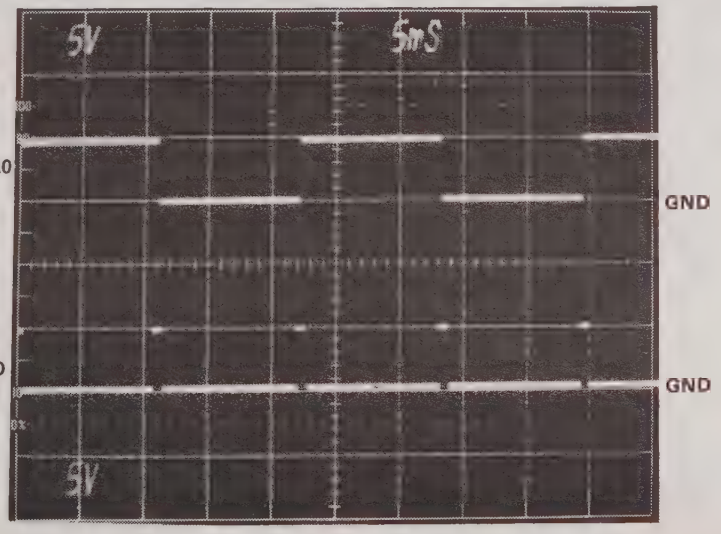
TITLE: TIMING DIAGRAM FAMILY CODES B3, B4		DRAWN BY:
		CHECKED BY: KH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 3


5V
2mS
6
PE
GND
BIT TO PROG
GND
5V

5


5V
2mS
200uS
PE
GND
BIT TO PROG
GND
5V
0971mS

6

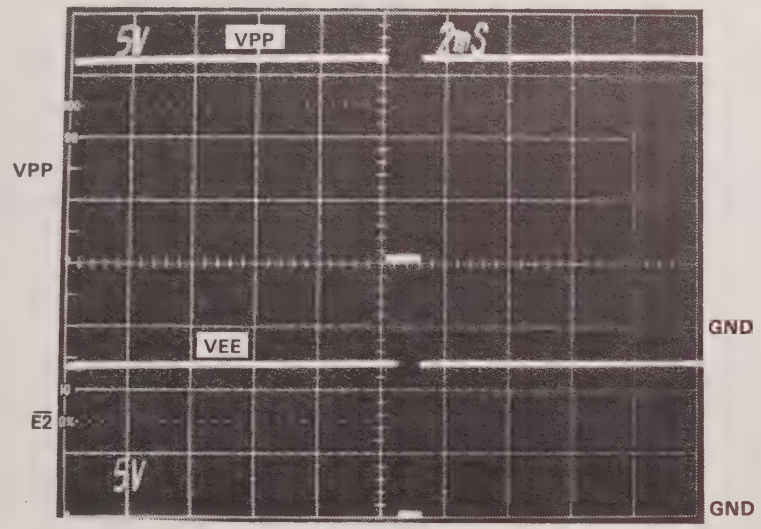

5V
5mS
A0
GND
BIT TO PROG
GND
5V

7

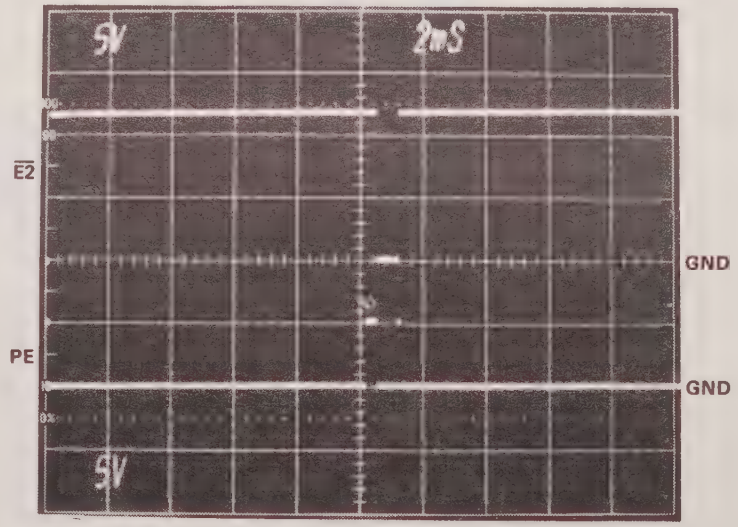
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831			
		ECN #5023	D	CTZ	3/84

DATA I/O

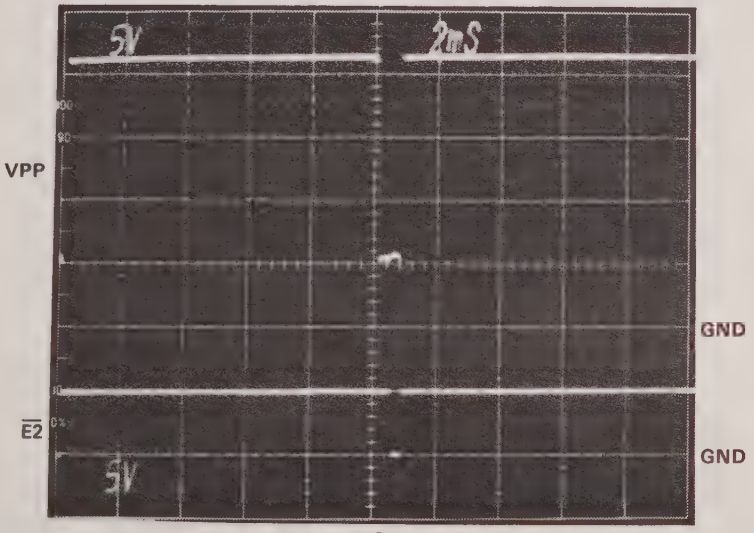
TITLE: TIMING DIAGRAM FAMILY CODES B3, B4	DRAWN BY:	CHECKED BY:
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 2 of 3


5V
VPP
2mS
VPP
VEE
GND
E2
5V
GND

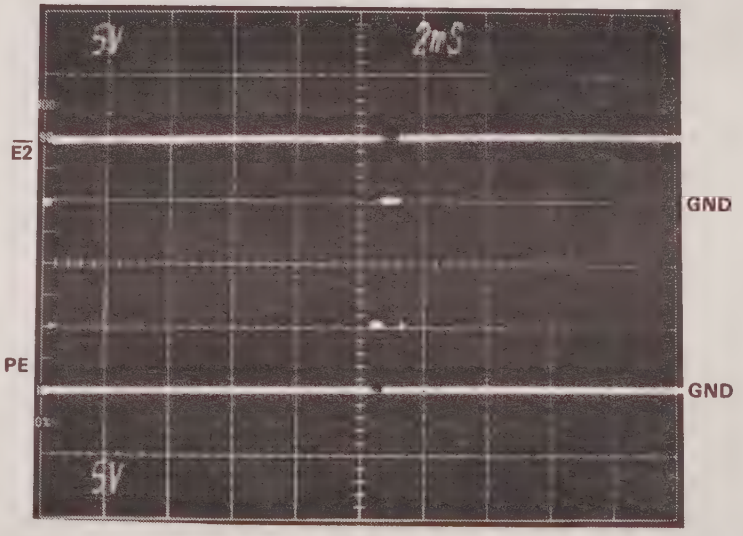
8


5V
2mS
E2
GND
PE
GND
5V

9


5V
2mS
VPP
GND
E2
GND
5V

10

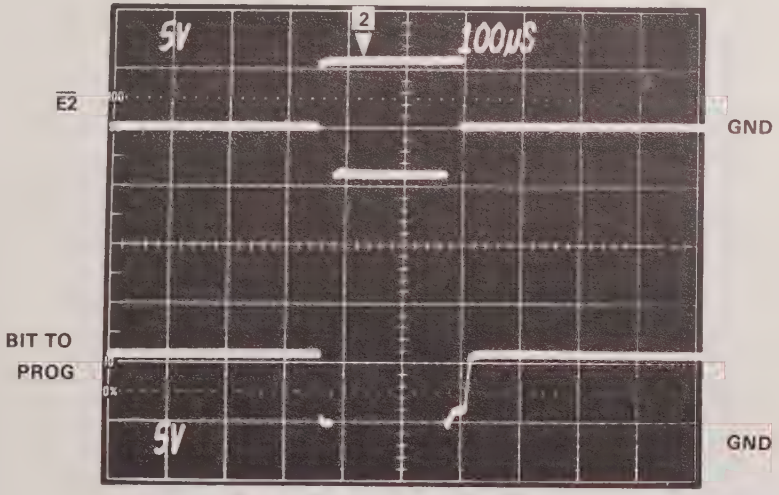

5V
2mS
E2
GND
PE
GND
5V

11

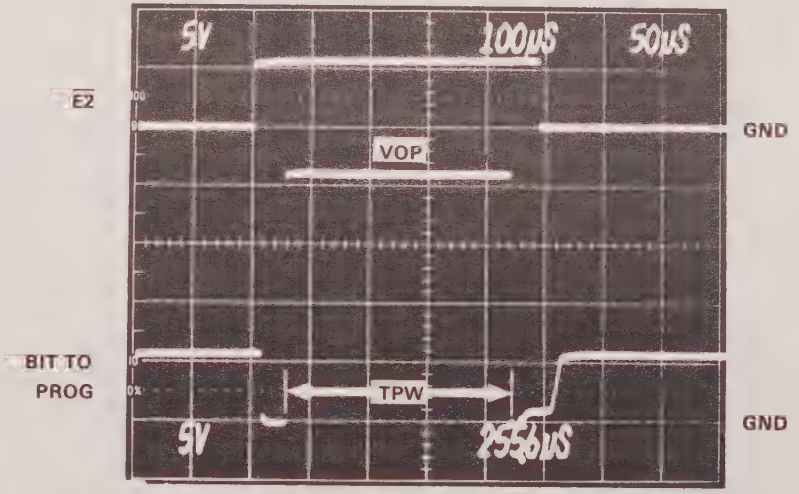
REVISIONS					
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		XH	5/83
		ECN #5023		CTZ	3/84

DATA I/O

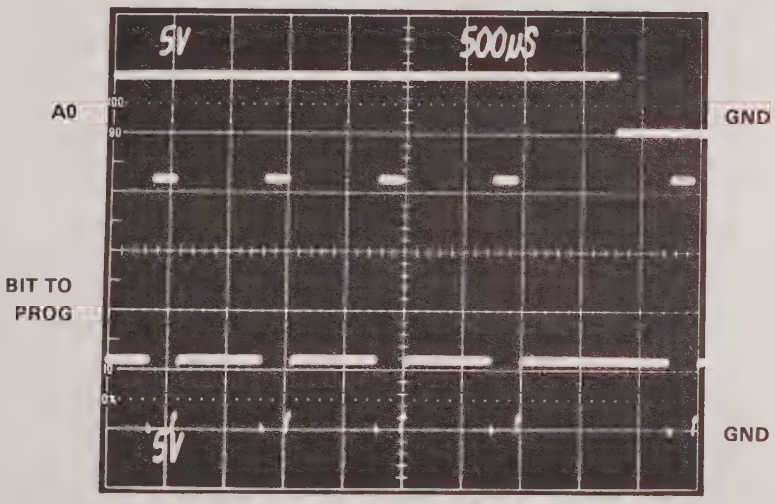
TITLE: TIMING DIAGRAM FAMILY CODES B3, B4		DRAWN BY:
		CHECKED BY: XH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 3 of 3


5V
2
100µS
E2
GND
BIT TO
PROG
5V
GND

1


5V
100µS
50µS
E2
GND
VOP
BIT TO
PROG
TPW
5V
GND

2


5V
500µS
A0
GND
BIT TO
PROG
5V
GND

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.00	5.25	V	Not shown
	VOP	20.0	20.5	21.0	V	
	VPP					NA
	VPPV					NA
	TPW	180	190	200	µs	At 10V Level
	TR					NA
	TF					NA
	Reject		4		Pulses	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.3	4.4	4.5	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	24.3	25.3	26.3	V	701-1655/TP4
	Low Load	24.3	25.3	26.3	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.4	5.5	5.6	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	6.3	6.8	7.3	V	701-1655/TP4
	Low Load	6.3	6.8	7.3	V	701-1655/TP3

NOTES

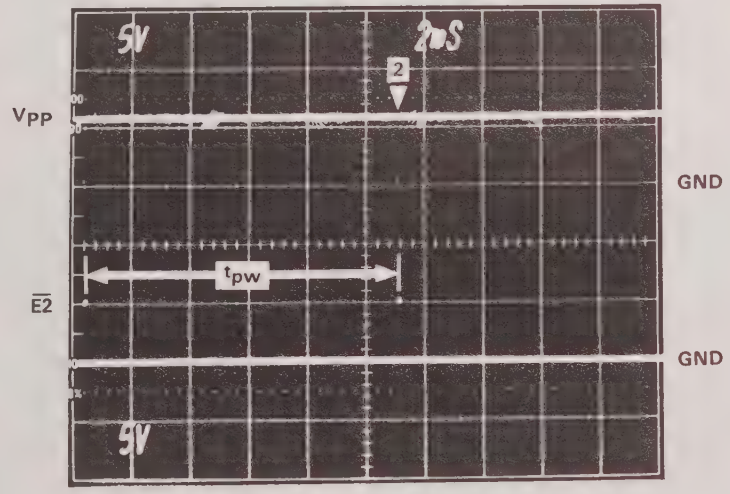
1. *Load RAM with hex FE for Family B5.*
2. *Load RAM with hex 01 for Family B6.*

REVISIONS

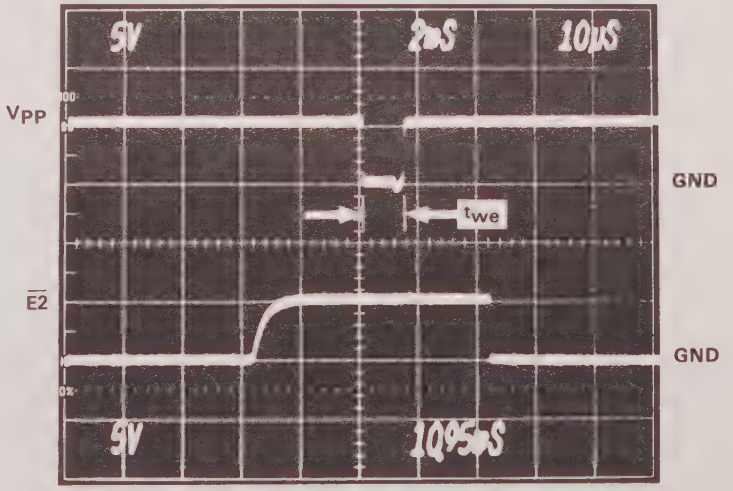
ZONE	LTR	DESCRIPTION	CM.	PE.	DATE
		ECN #4831		KH	9/84
		ECN #5023		C73	3/87

DATA I/O

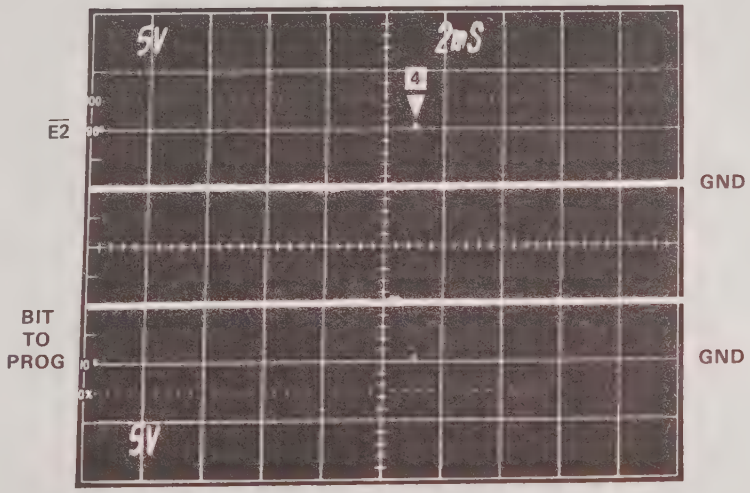
TITLE: TIMING DIAGRAM FAMILY CODES B5, B6		DRAWN BY:
		CHECKED BY: KH
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 33-950-0059
SCALE		SHEET 1 of 1


5V
2mS
2
VPP
GND
tpw
E2
GND
5V

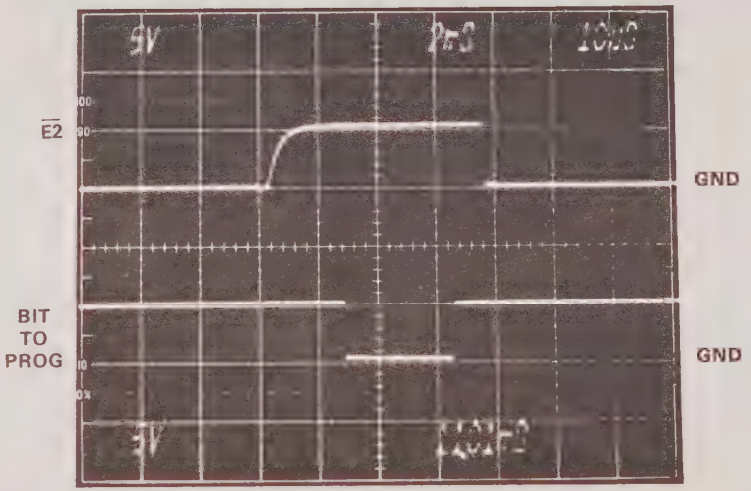
1


5V
2mS
10μS
VPP
GND
twe
E2
GND
5V

2


5V
2mS
4
E2
GND
BIT
TO
PROG
GND
5V

3


5V
E2
GND
BIT
TO
PROG
GND

4

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EP}	20.5	21.0	21.5	V	
	V_{EE}	11.5	12.0	12.5	V	
	t_{we}	150			ns	
	t_{pw}	9	10		ms	
	t_r					N.A.
	t_{ew}	9.0	10	15	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.3	0.4	0.5	V	701-1655/TP2
	HIGH LOAD	4.7	5.2	5.7	V	701-1655/TP4
	LOW LOAD	4.7	5.2	5.7	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	6.5	7.0	7.5	V	701-1655/TP3

1. *Load RAM with hex FE for Family B7.*
2. *Load RAM with hex 01 for Family B8.*
3. *Photo 6 shows erase pulse.*

REVISIONS

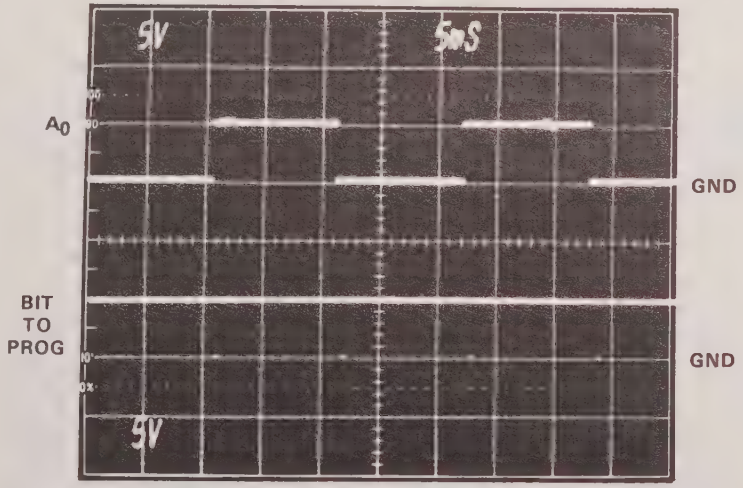
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

Sheet 1 of 2

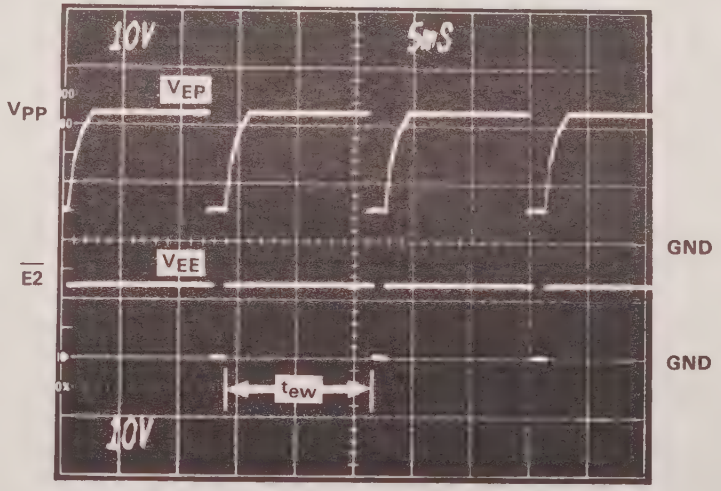
TIMING DIAGRAM

FAMILY CODES B7, B8

DATA I/O


5V
5mS
A0
GND
BIT
TO
PROG
GND
5V

5


10V
5mS
VPP
VEP
GND
E2
VEE
GND
tew
10V

6

B-213
10-950-0059

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

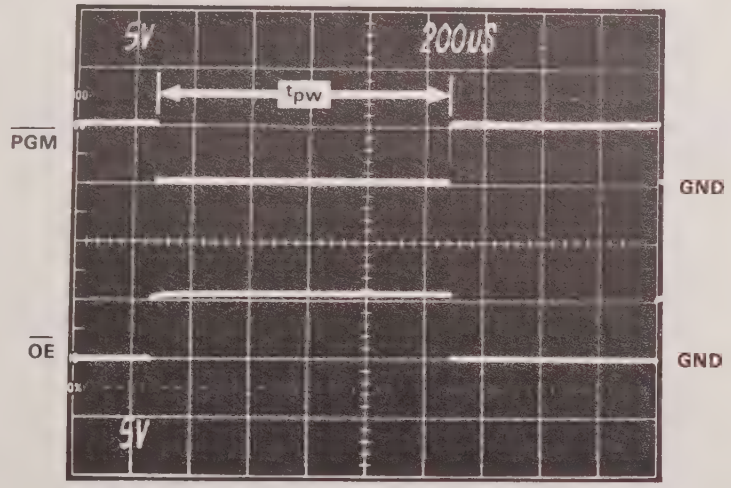
Sheet 2 of 2

TIMING DIAGRAM

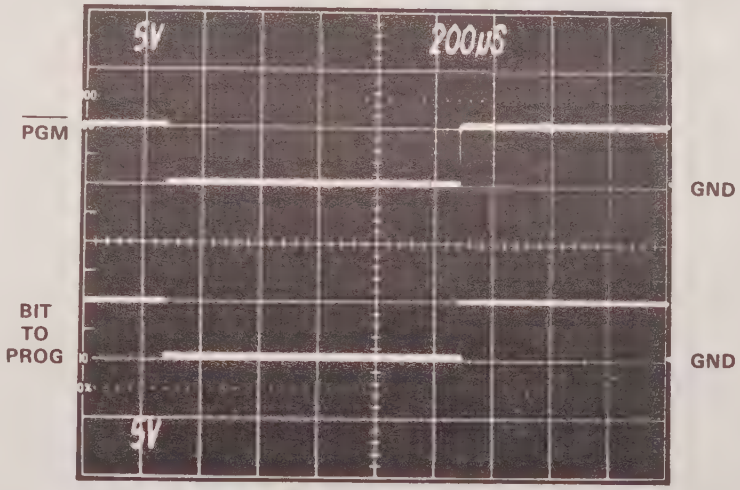
FAMILY CODES B7, B8

DATA I/O

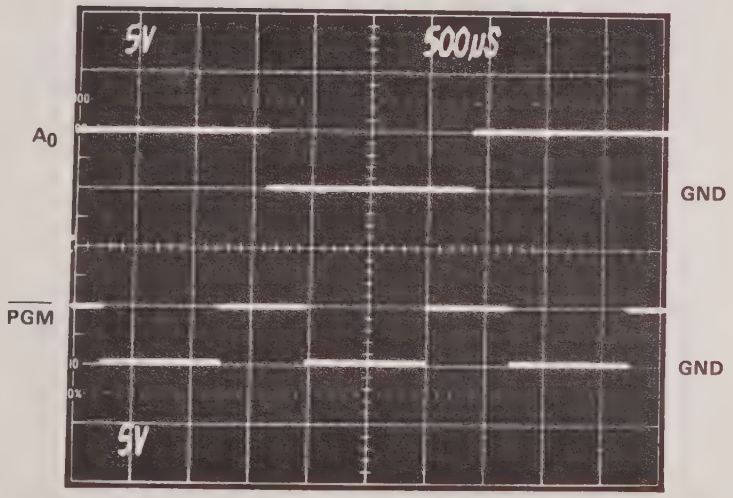
0526/1282


5V
200μS
t_{pw}
PGM
GND
OE
GND
5V

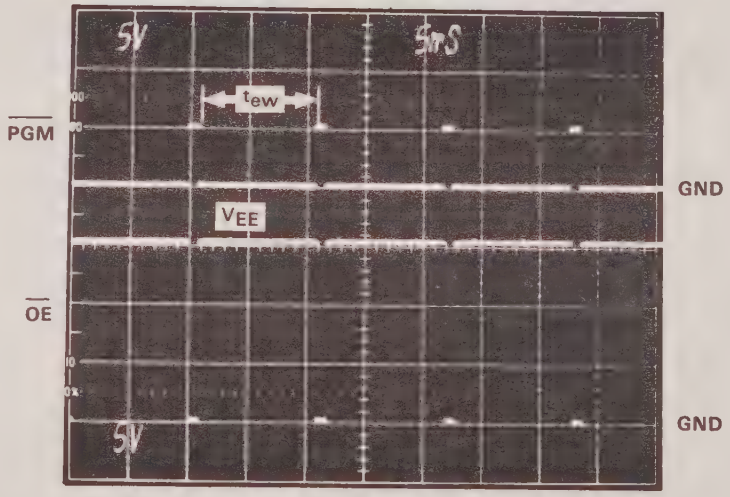
1


5V
200μS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
500μS
A_0
GND
PGM
GND
5V

3


5V
5mS
t_{ew}
PGM
GND
V_{EE}
OE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	14.0	14.5	15.0	V	
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	5.0	5.5	6.0	V	701-1655/TP4
	LOW LOAD	5.0	5.5	6.0	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	7.3	7.8	8.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family B9.*
2. *Photo 4 is chip erase.*

REVISIONS

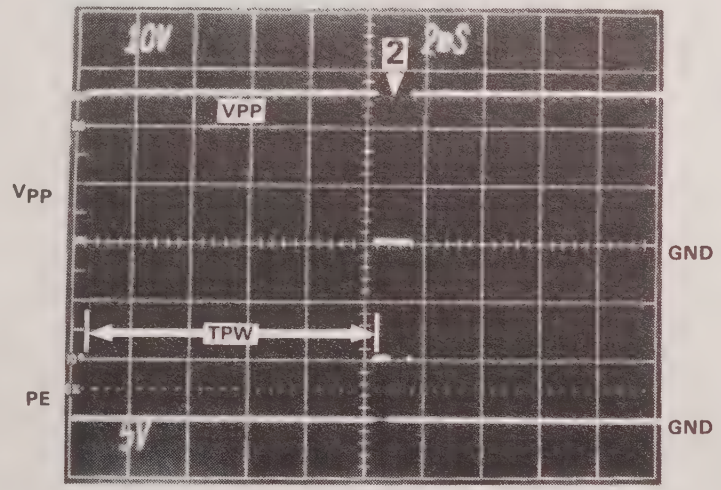
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTS	3/84

Sheet 1 of 1

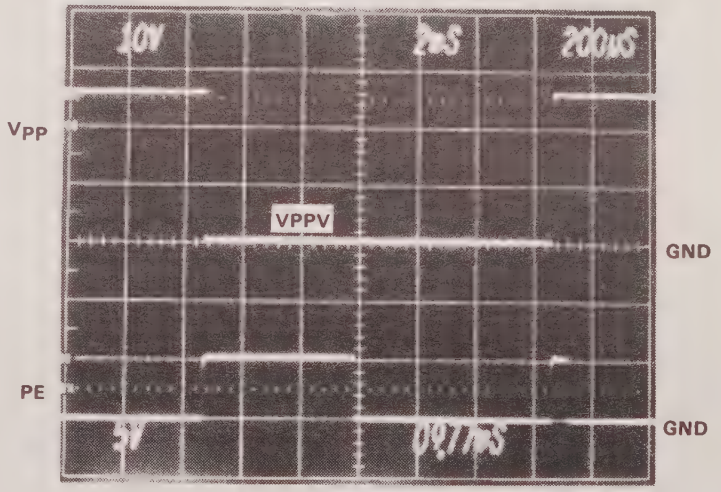
TIMING DIAGRAM

FAMILY CODES B9, BA

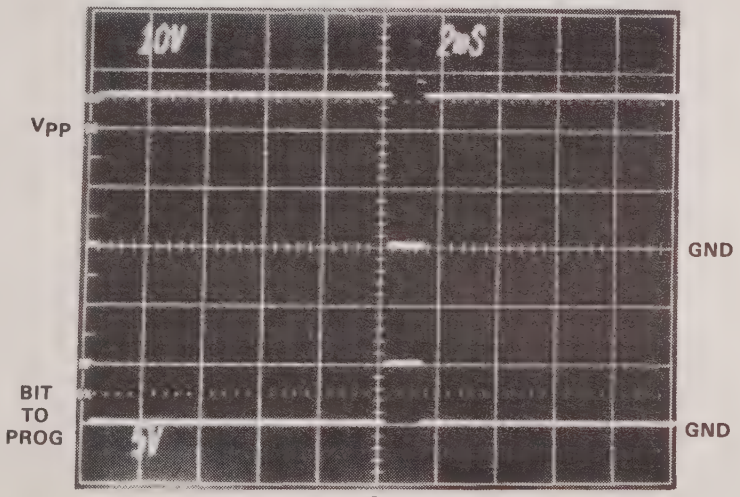
DATA I/O


10V
2mS
2
VPP
VPP
GND
TPW
PE
GND
5V

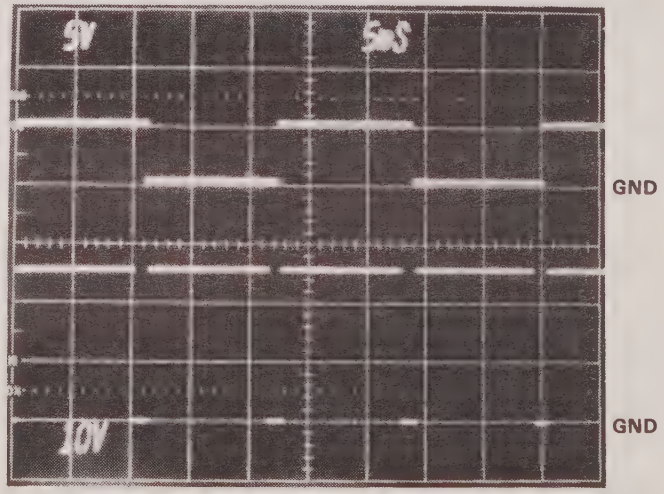
1


10V
2mS
200uS
VPP
VPPV
GND
PE
GND
5V

2


10V
2mS
VPP
GND
BIT
TO
PROG
5V
GND

3


9V
5mS
AO
GND
VPP
10V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	24.5	25.0	25.5	V	
	V_{PPV}	0.0	0.0	0.5	V	
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family BD.*
2. *Photo 5 is for Pinout 23.*
3. *Photo 6 is for Pinouts 25 and 30.*

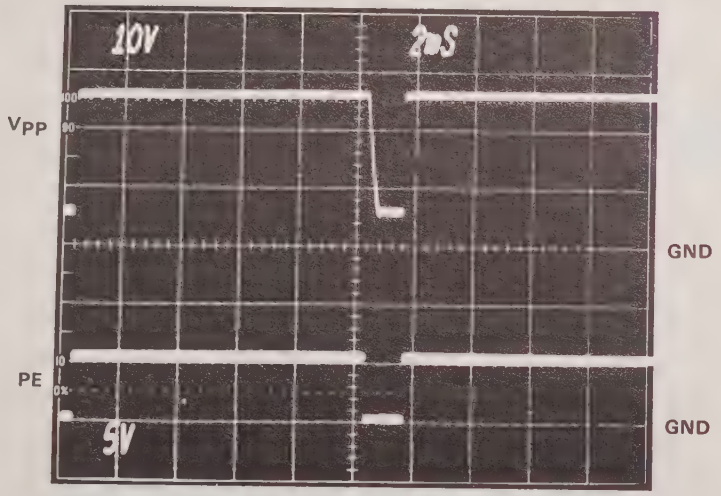
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	C73	3/84

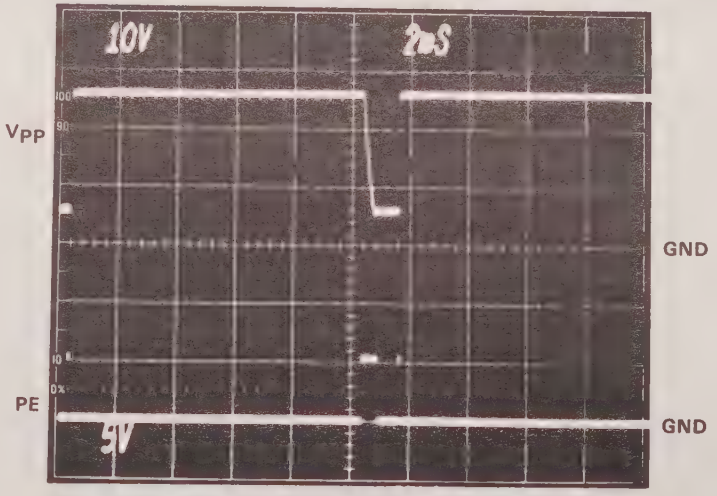
TIMING DIAGRAM

FAMILY CODES BD, BE

DATA I/O



5



6

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTZ	3/84

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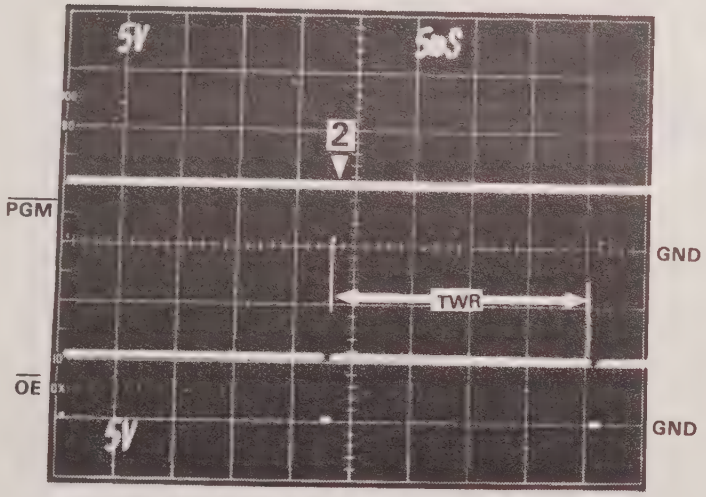
TIMING DIAGRAM

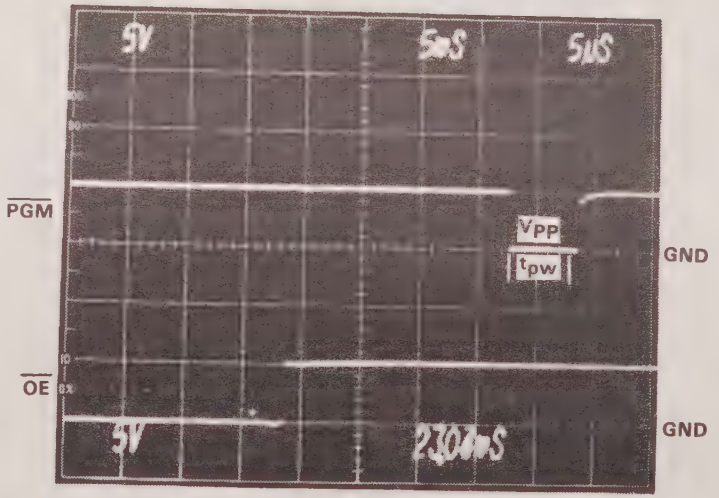
FAMILY CODES BD, BE

DATA I/O

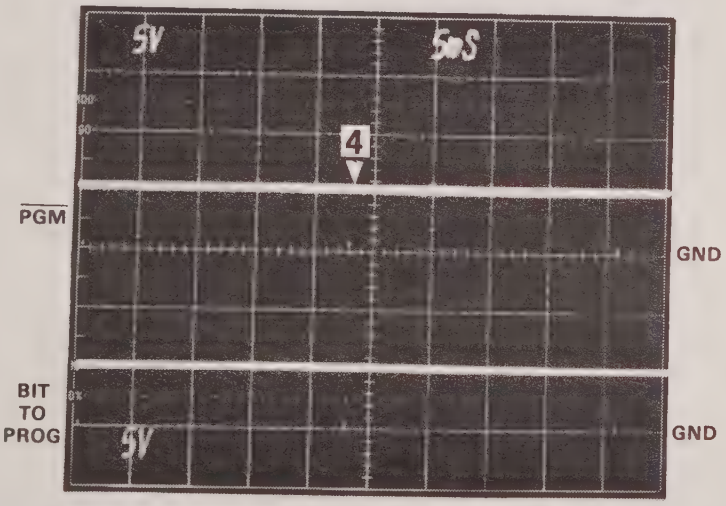
0526/1282


5V
5mS
2
PGM
GND
TWR
OE
GND
5V

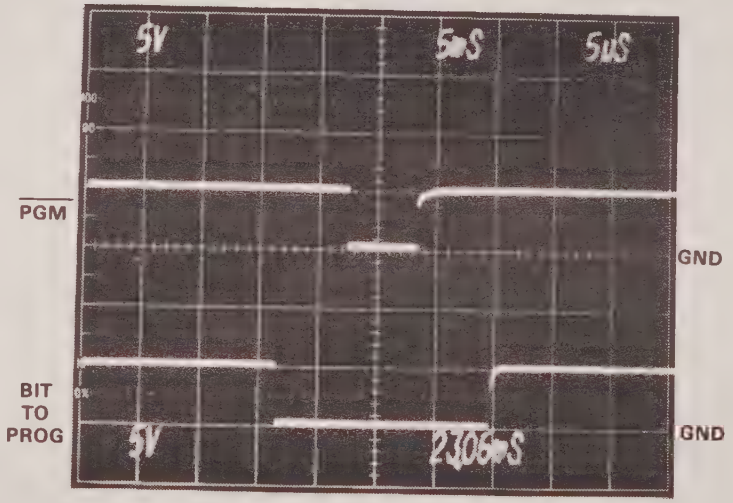
1


5V
5mS
5uS
PGM
VPP
tpw
GND
OE
GND
5V
2304mS

2


5V
5mS
4
PGM
GND
BIT
TO
PROG
GND
5V

3


5V
5mS
5uS
PGM
GND
BIT
TO
PROG
GND
5V
2306mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	0.0	0.0	0.8	V	
	V_{PPV}					N.A.
	t_{pw}	100			ns	
	t_r					N.A.
	t_{wr}	20			ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family BF.*
2. *Load pin 1 with a 330 Ω, ½-watt resistor to observe TWR in photo 1.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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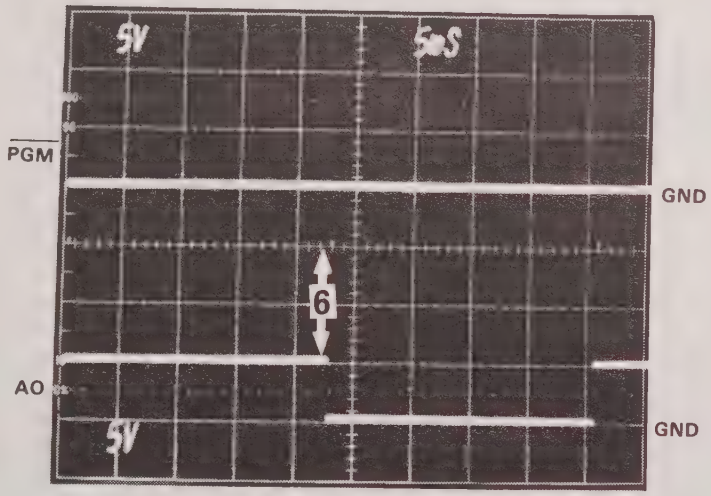
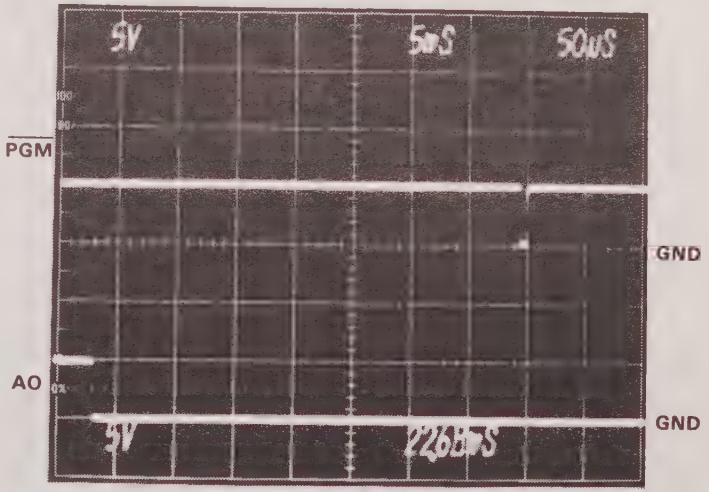
TIMING DIAGRAM

FAMILY CODES BF, CO

DATA I/O



5



6

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

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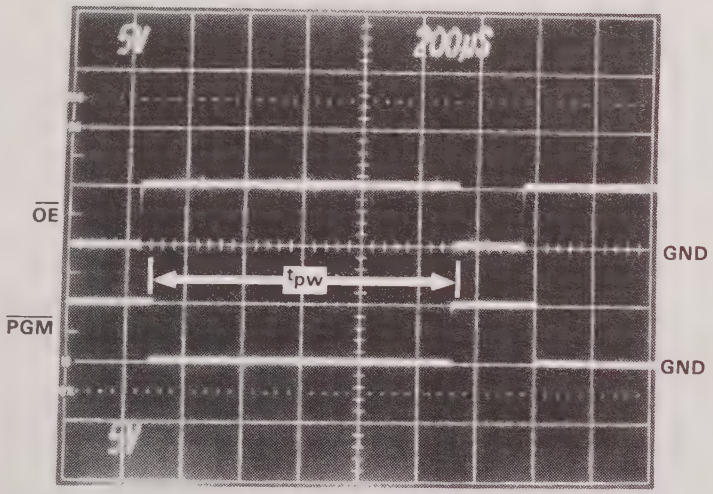
TIMING DIAGRAM

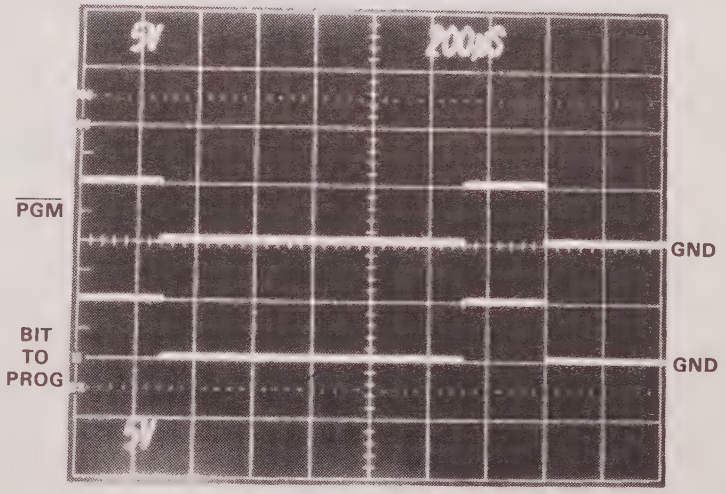
FAMILY CODES BF, CO

DATA I/O

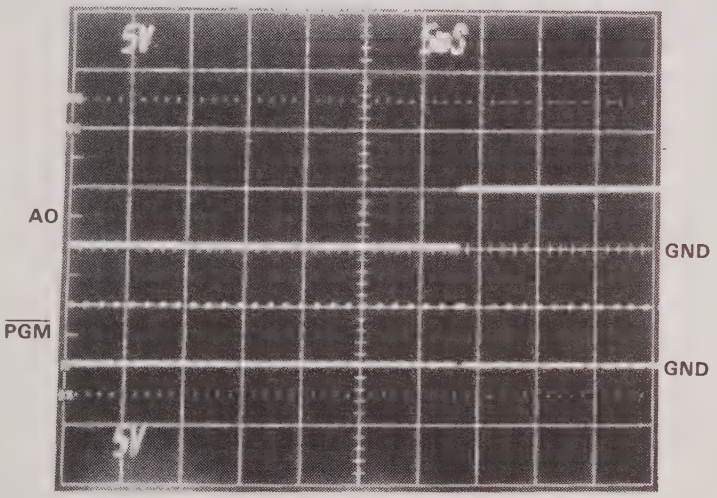
0526/1282


5V
200μS
OE
GND
t_{pw}
PGM
GND
5V

1


5V
200μS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
5mS
AO
GND
PGM
GND
5V

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	12.5	13.0	13.5	V	Not shown
	V_{PPV}					N.A.
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSE	
	Overprogram		1		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. Load RAM with hex FE for Family C1.

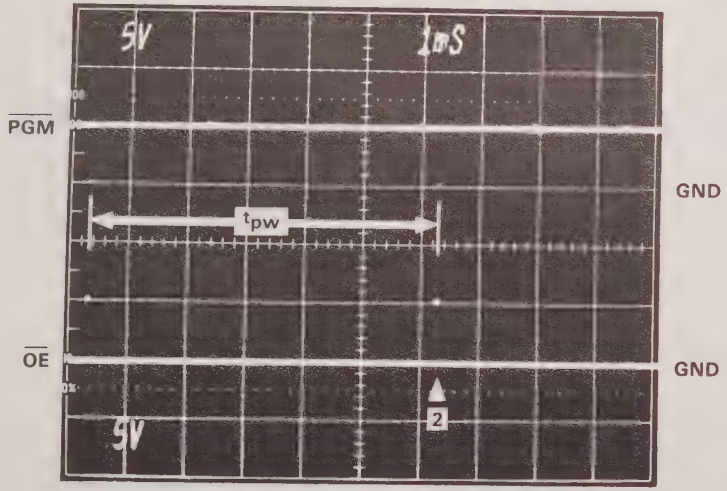
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

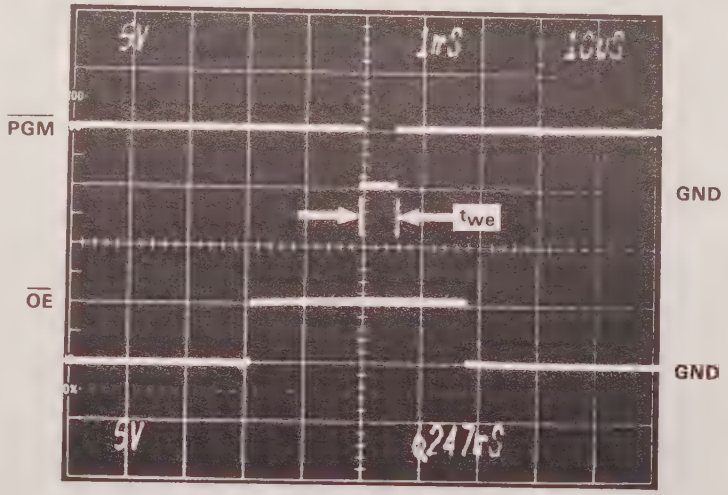
TIMING DIAGRAM

FAMILY CODES C1, C2

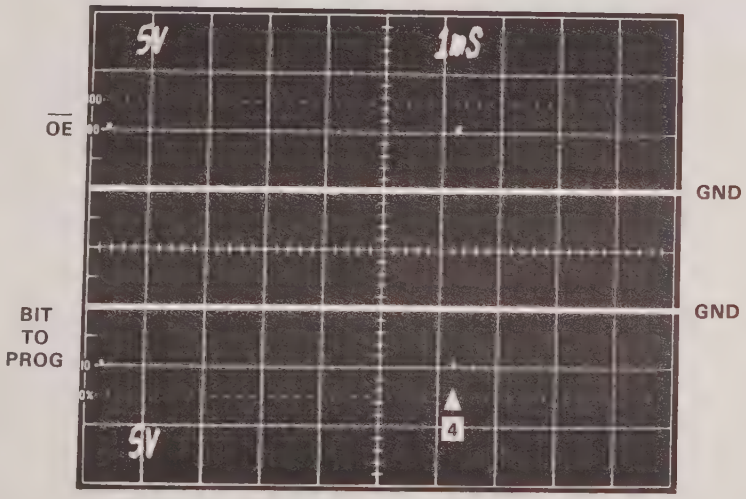
DATA I/O


5V
1mS
PGM
GND
tpw
OE
GND
5V
2

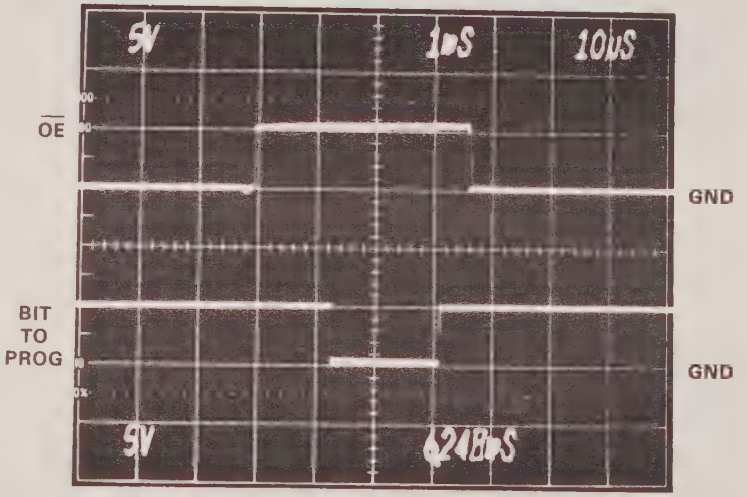
1


5V
1mS
10uS
PGM
GND
twe
OE
GND
5V
4247FS

2


5V
1mS
OE
GND
BIT
TO
PROG
GND
5V
4

3


5V
1mS
10uS
OE
GND
BIT
TO
PROG
GND
5V
421B5

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	14.5	15.0	15.5	V	
	t_{we}	150			ns	
	t_{pw}	0.1	5.0		ms	
	t_r					N.A.
	t_{ew}	150			ns	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.3	0.4	0.5	V	701-1655/TP2
	HIGH LOAD	4.7	5.2	5.7	V	701-1655/TP4
	LOW LOAD	4.7	5.2	5.7	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	6.5	7.0	7.5	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family C3.*
2. *Load RAM with hex 01 for Family C4.*
3. *Photos 6 and 7 show erase pulse.*

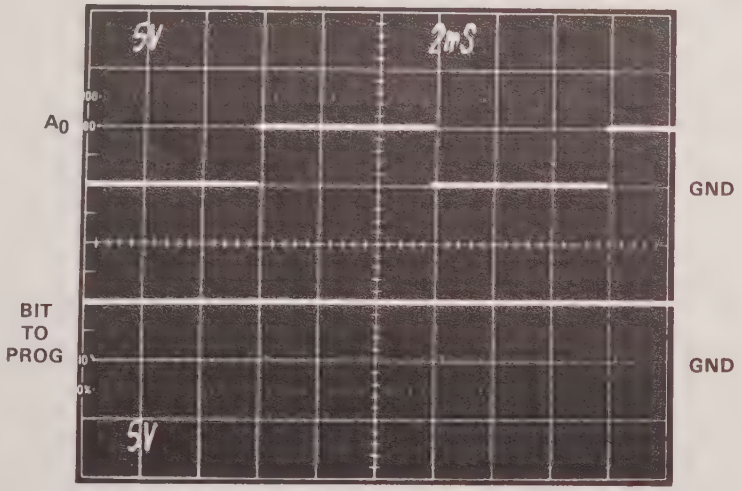
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	C78	3/84

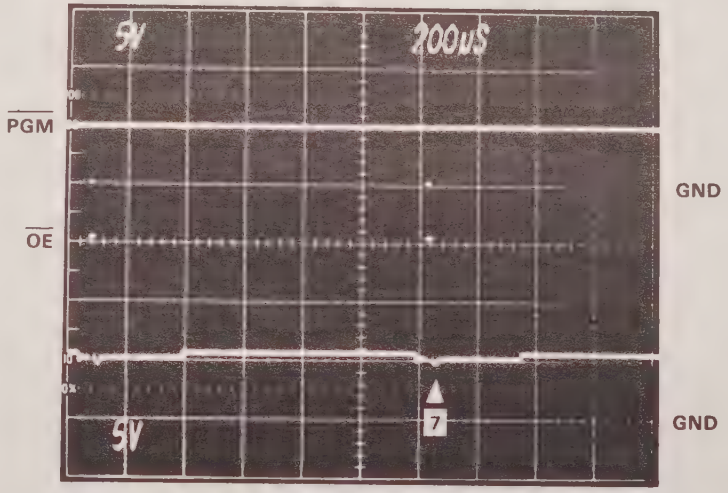
TIMING DIAGRAM

FAMILY CODES C3, C4

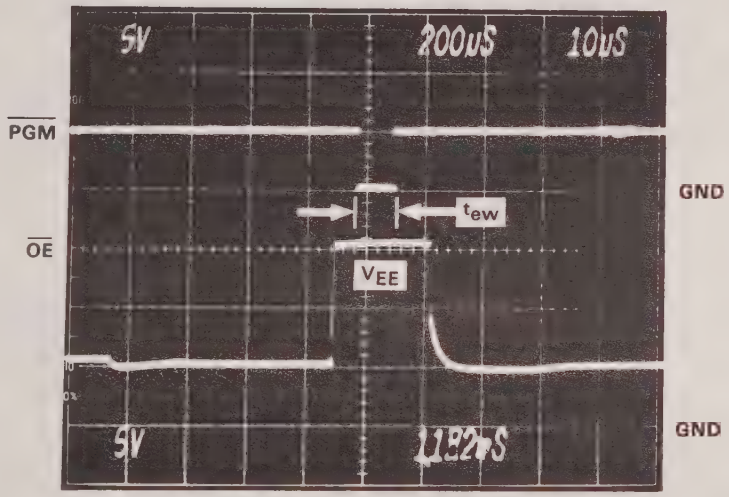
DATA I/O


5V
2mS
A0
GND
BIT
TO
PROG
GND
5V

5


5V
200uS
PGM
GND
OE
7
GND
5V

6


5V
200uS
10uS
PGM
GND
tew
OE
VEE
GND
5V

7

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTS	3/84

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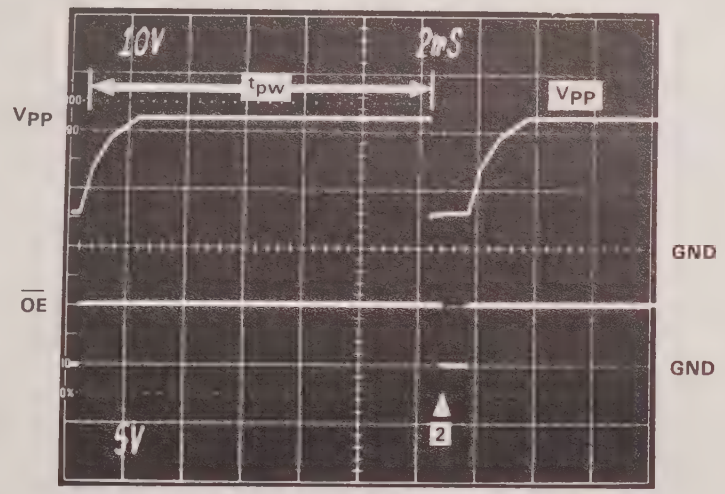
TIMING DIAGRAM

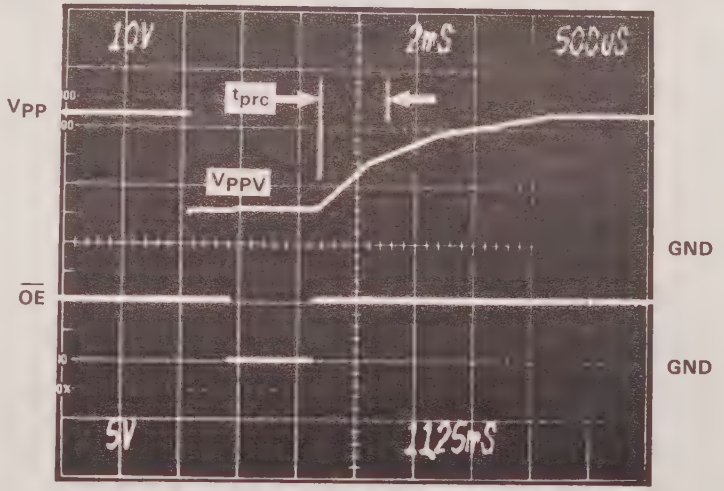
FAMILY CODES C3, C4

DATA I/O

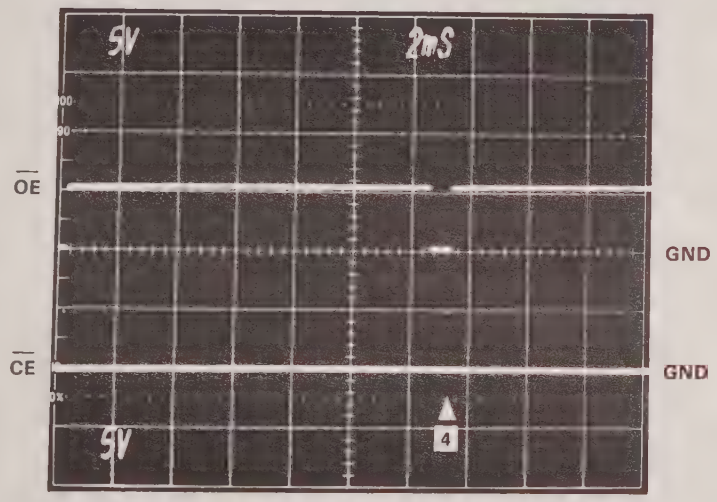
0526/1282


10V
2mS
t_{pw}
V_{PP}
V_{PP}
GND
$\overline{OE}$
GND
5V
2

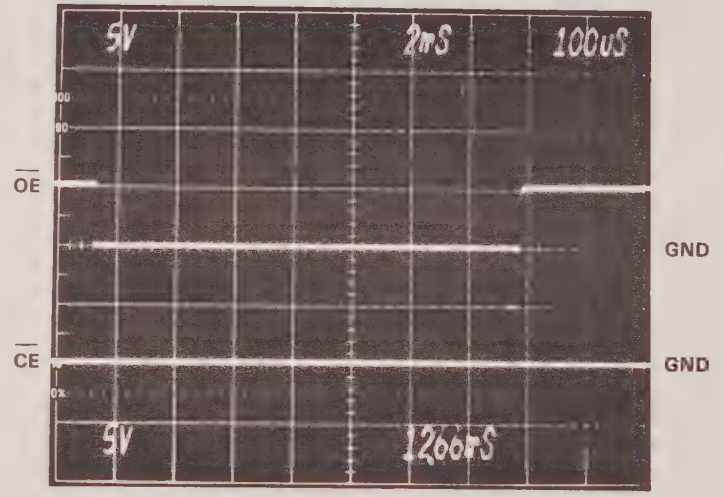
1


10V
2mS
500uS
V_{PP}
t_{prc}
V_{PPV}
GND
$\overline{OE}$
GND
5V
1.125mS

2


5V
2mS
$\overline{OE}$
GND
$\overline{CE}$
GND
5V
4

3


5V
2mS
100uS
$\overline{OE}$
GND
$\overline{CE}$
GND
5V
1266nS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	20.0	21.0	22.0	V	
	V_{PPV}	4.0	5.0	6.0	V	
	t_{prc}	450	600	750	μs	See note 3
	t_{pw}	9.0		15.0	ms	
	t_r					N.A.
	t_f			100	μs	
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family C7.*
2. *Load RAM with hex 01 for Family C8.*
3. *TPRC is measured from 6V to 15.5V.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	C7Z	3/84

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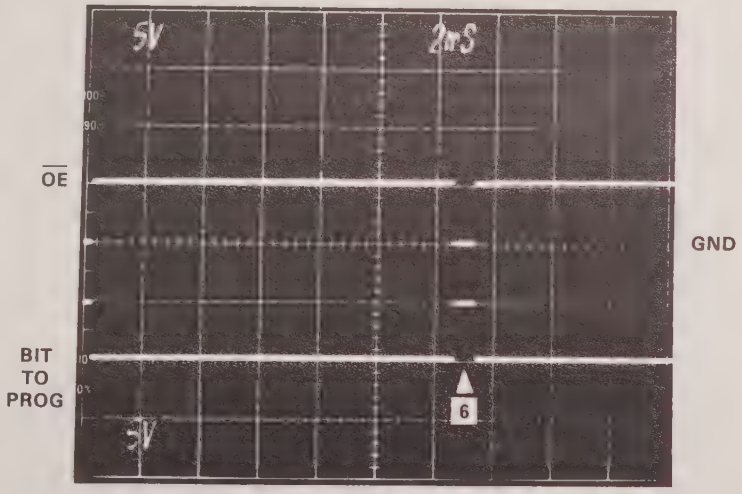
TIMING DIAGRAM

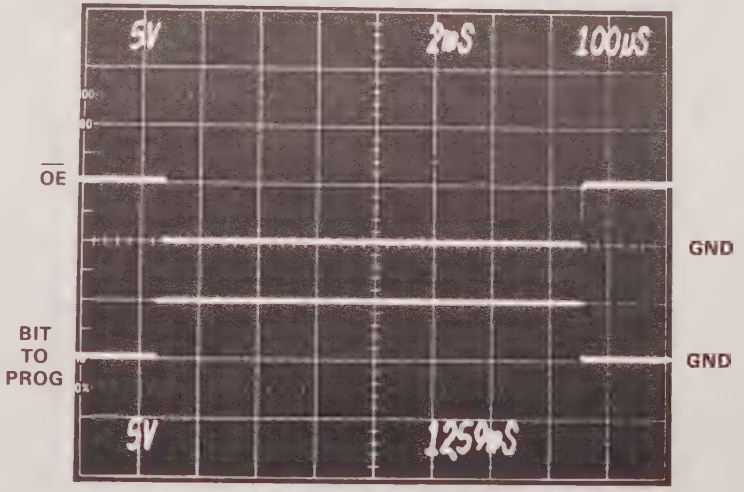
FAMILY CODES C7, C8

DATA I/O

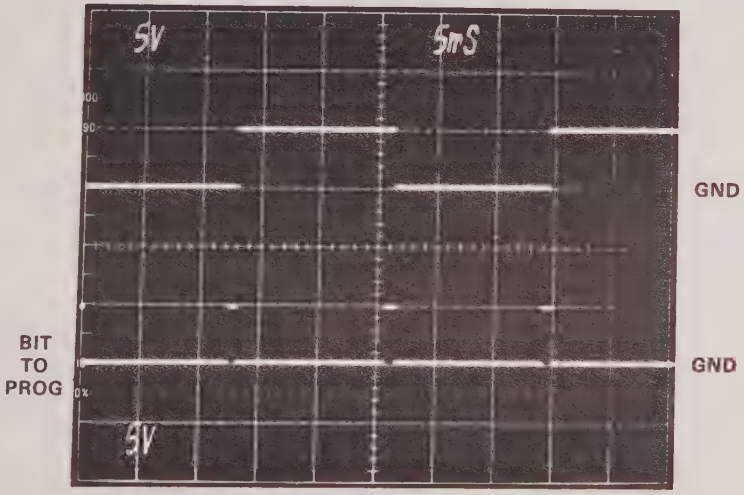
0526/1282


5V
2mS
OE
GND
BIT
TO
PROG
6
5V

5


5V
2mS
100uS
OE
GND
BIT
TO
PROG
GND
5V
1250uS

6


5V
5mS
GND
BIT
TO
PROG
GND
5V

7

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REVISIONS

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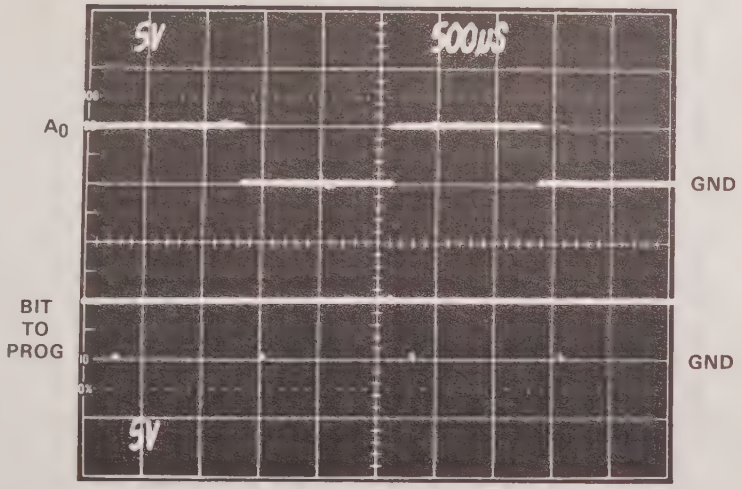
TIMING DIAGRAM

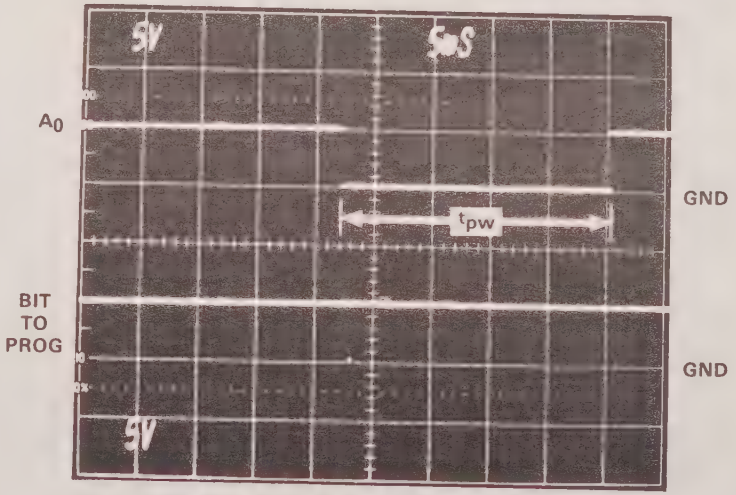
FAMILY CODES C7, C8

DATA I/O

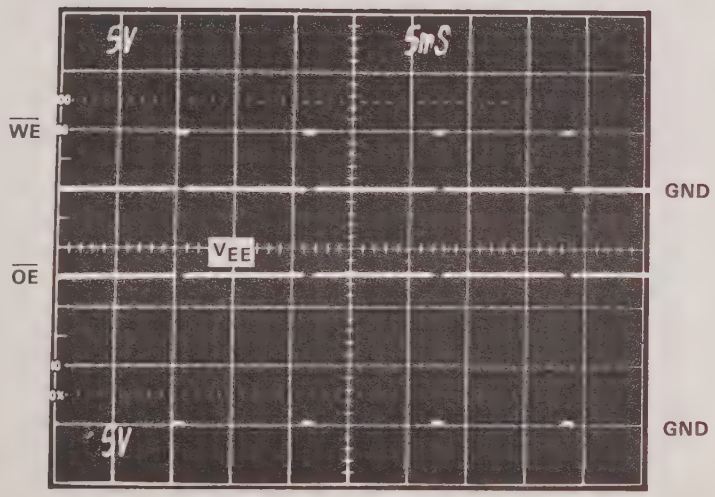
0526/1282


5V
500μS
A0
GND
BIT
TO
PROG
GND
5V

5


5V
5mS
A0
GND
tpw
BIT
TO
PROG
GND
5V

6


5V
5mS
WE
GND
VEE
OE
GND
5V

7

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REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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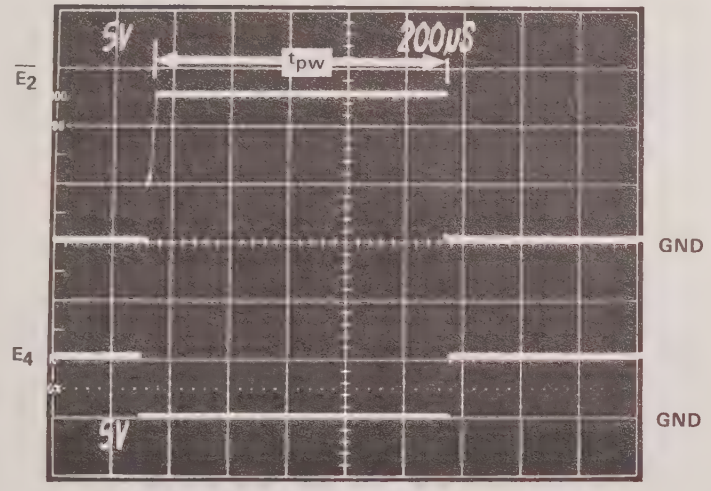
TIMING DIAGRAM

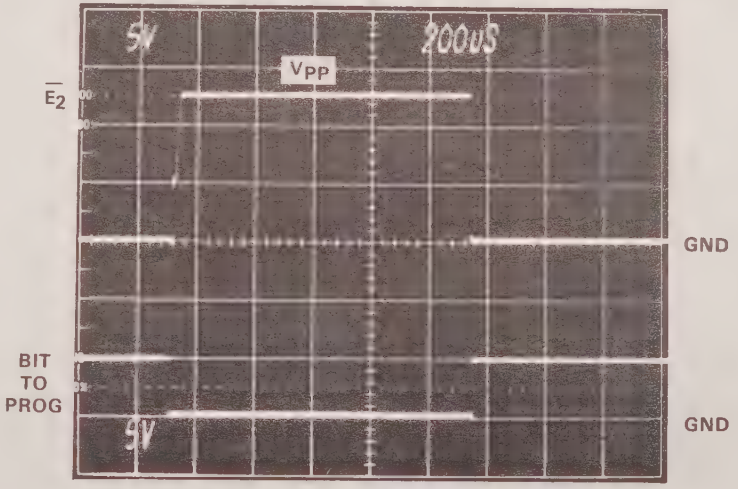
FAMILY CODES C9, CA

DATA I/O

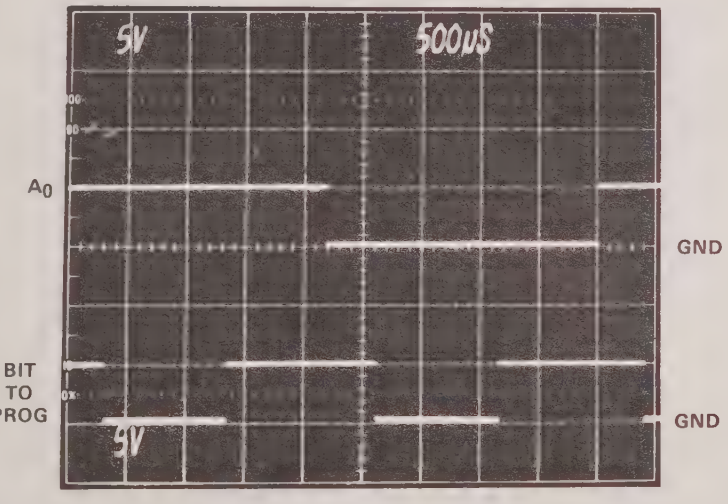
0526/1282


5V
200µS
t_{pw}
$\overline{E_2}$
GND
E_4
GND
5V

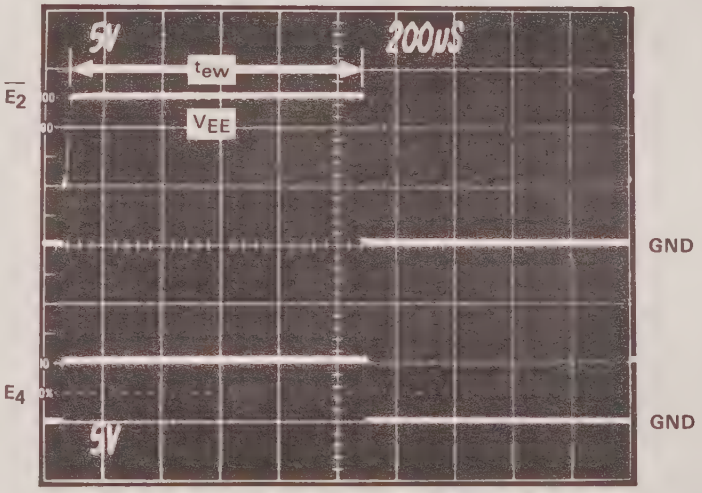
1


5V
200µS
V_{PP}
$\overline{E_2}$
GND
BIT TO PROG
GND
5V

2


5V
500µS
A_0
GND
BIT TO PROG
GND
5V

3


5V
200µS
t_{ew}
$\overline{E_2}$
V_{EE}
GND
E_4
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	11.5	12.0	12.5	V	
	V_{PPV}					N.A.
	V_{EE}	11.5	12.0	12.5	V	
	t_{pw}	1.0			ms	
	t_r					N.A.
	t_{ew}	1.0			ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	0.7	0.8	0.9	V	701-1655/TP2
	HIGH LOAD	5.1	5.6	6.1	V	701-1655/TP4
	LOW LOAD	5.1	5.6	6.1	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	1.9	2.0	2.1	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	6.1	6.6	7.1	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family CD.*
2. *Load RAM with hex 01 for Family CE.*
3. *Photo 4 shows erase pulse.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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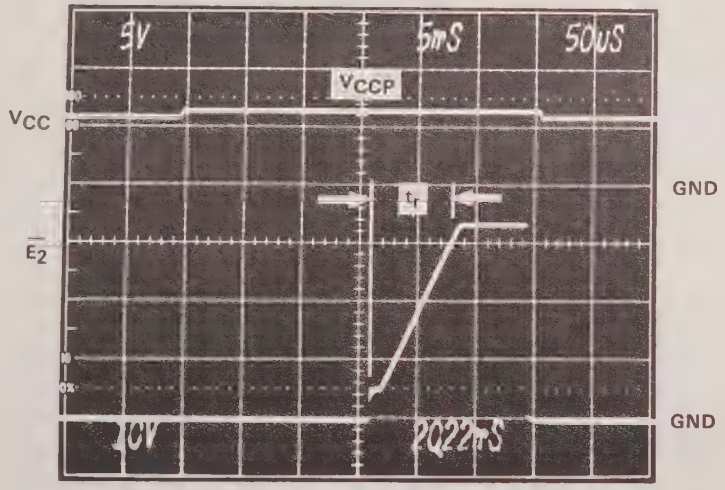
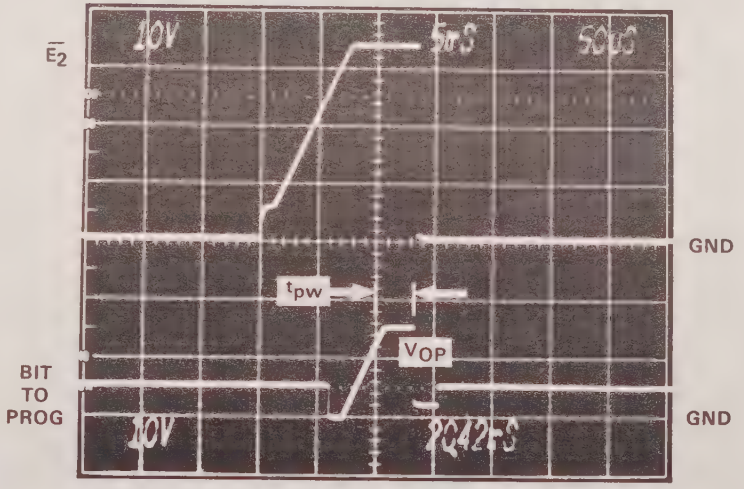
TIMING DIAGRAM

FAMILY CODES CD, CE

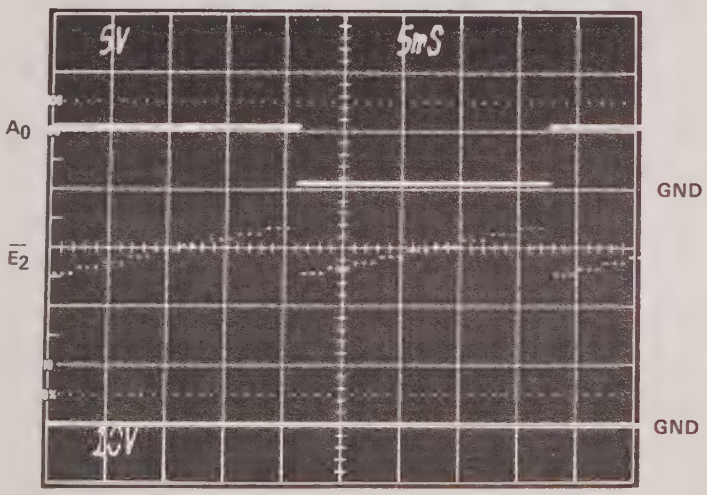
DATA I/O


9V
5mS
50uS
VCCP
VCC
GND
tr
E2
GND
1CV
2Q22mS

1


E2
10V
5mS
50uS
GND
tpw
VOP
BIT
TO
PROG
GND
10V
2Q42FS

2


9V
5mS
A0
GND
E2
GND
1CV

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.25	5.5	5.75	V	
	V_{OP}	14.5	15.0	15.5	V	
	V_{PPS}	24.0	25.0	26.0	V	See note 3
	V_{PPF}	32 0	33.0	34.0	V	See note 3
	t_{pw}	10		40	μs	
	t_r	53	66	88	μs	See note 4
	t_f					N.A.
	Reject		27		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1655/TP2
	HIGH LOAD	18.4	18.9	19.4	V	701-1655/TP4
	LOW LOAD	18.4	18.9	19.4	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	2.9	3.0	3.1	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	5.1	5.6	6.1	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family D1.*
2. *Load RAM with hex 01 for Family D2.*
3. *Vpp starts at 25V and increments to 33V in 1-volt steps with 3 pulses per step.*
4. *TR is measured 10% to 90% of greatest amplitude $\overline{E_2}$ pulse.*

REVISIONS

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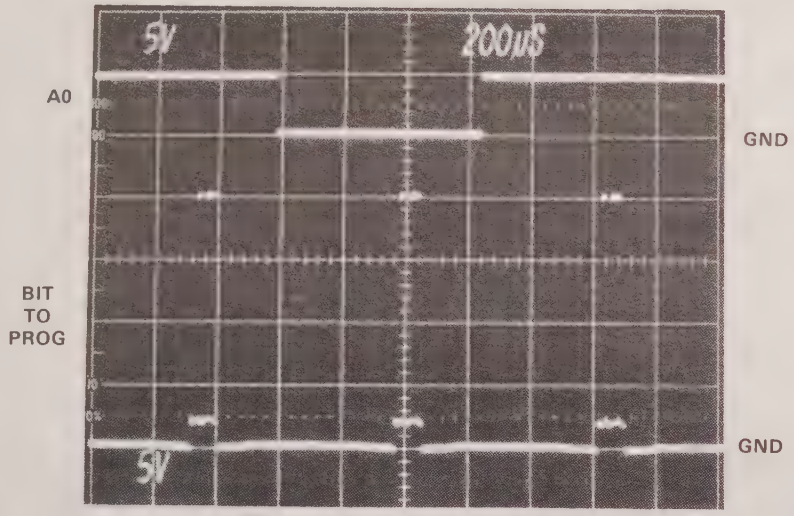
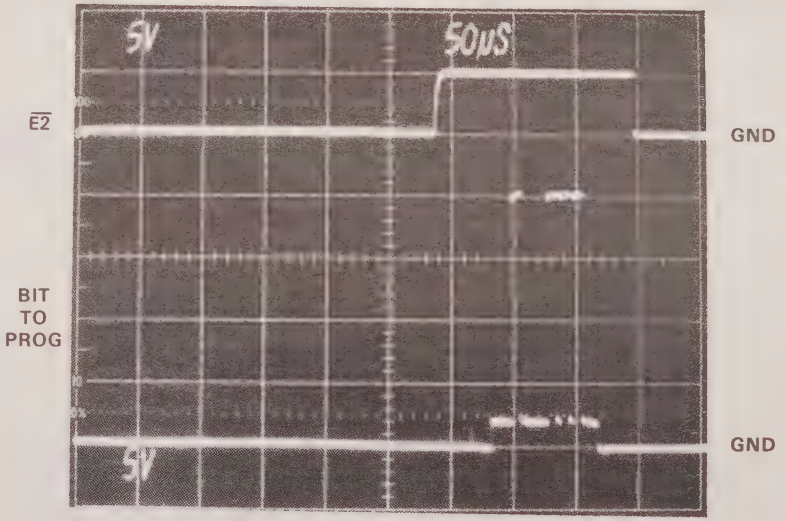
TIMING DIAGRAM

FAMILY CODES D1, D2

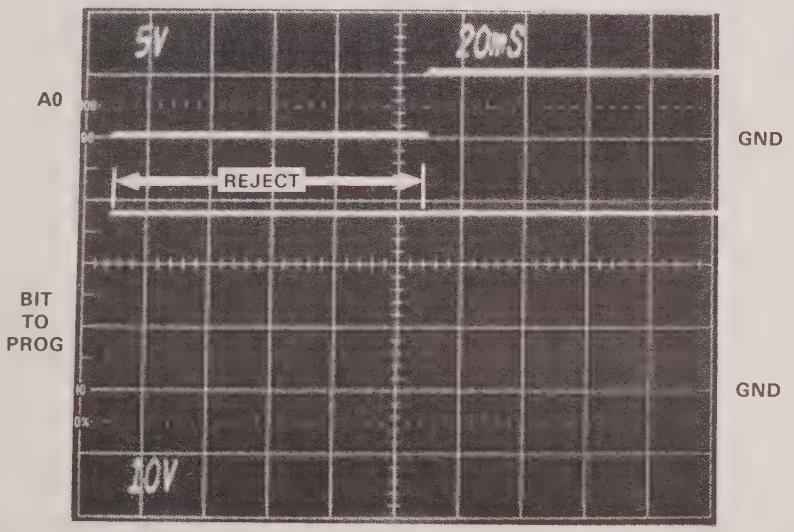
DATA I/O


5V
200μS
A0
GND
BIT
TO
PROG
GND
5V

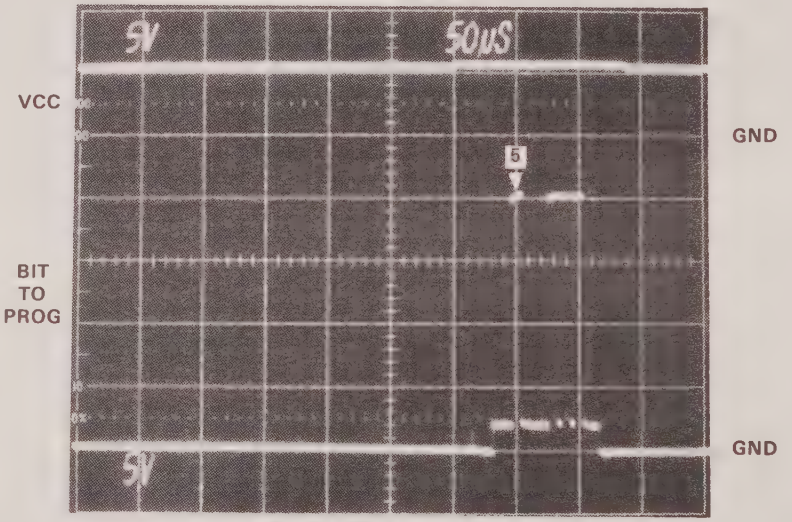
1


5V
50μS
$\overline{E2}$
GND
BIT
TO
PROG
GND
5V

2


5V
20mS
A0
GND
REJECT
BIT
TO
PROG
GND
10V

3


5V
50μS
VCC
GND
5
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.00	5.20	5.40	V	
	VPP					NA
	VOP	27.5	28.0	28.5	V	
	TPW	7.0	7.5	8.0	μs	See Note 2
	T_R	0.21		0.30	μs	
	T_F	0.21		0.30	μs	
	Overprogram		4		Pulses	
	Reject		10,000		Pulses	See Note 3
	Duty Cycle	70	75	80	%	
1ST PASS VERIFY	VCC	4.0	4.1	4.2	V	
	VREF	0.7	0.8	0.9	V	701-1655/TP2
	High Load	25.0	26.0	27.0	V	701-1655/TP4
	Low Load	25.0	26.0	27.0	V	701-1655/TP3
2ND PASS VERIFY	VCC	6.4	6.5	6.6	V	
	VREF	6.9	7.0	7.1	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	8.6	9.6	10.6	V	701-1655/TP3

NOTES

1A. Load RAM with hex FE for Family D3.
1B. Load RAM with hex 01 for Family D4.
2. Measurement taken at 10V point of 01 with a 100 Ω load.
3. 10,000 pulses equals 100 ms as shown in photo 3.
4. Do not use a wirewound load resistor.

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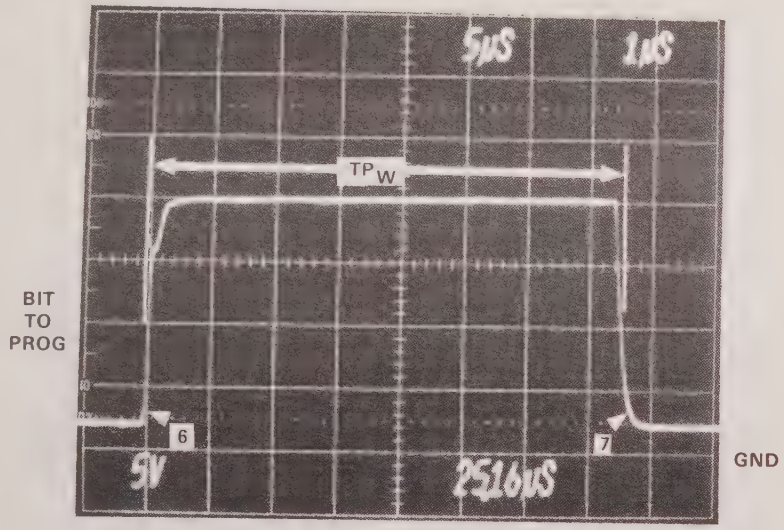
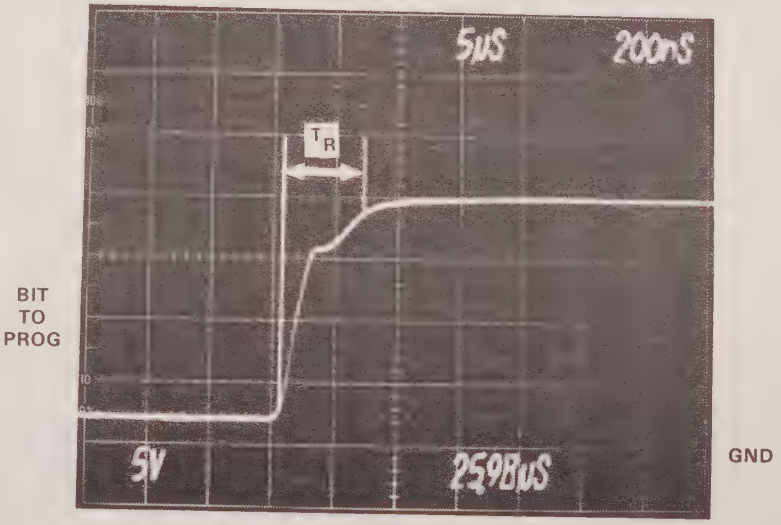
TIMING DIAGRAM

FAMILY CODES D3, D4

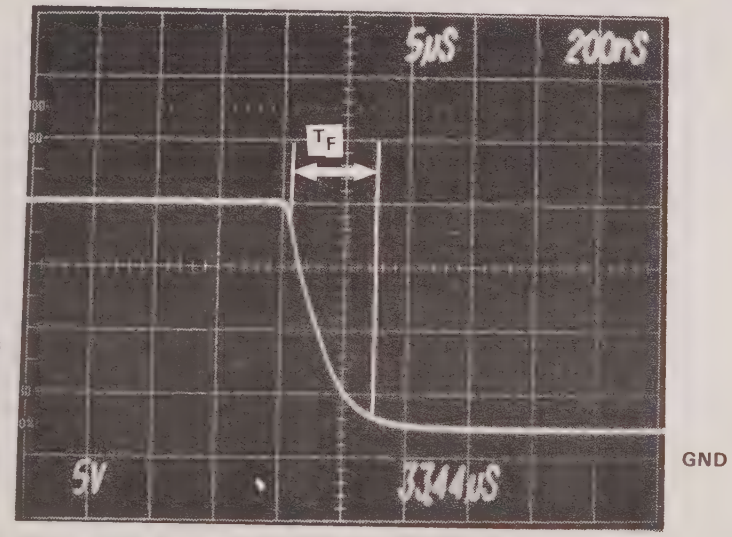
DATA I/O


5uS
1uS
TPW
BIT
TO
PROG
6
7
5V
2516uS
GND

5


5uS
200nS
TR
BIT
TO
PROG
5V
2598uS
GND

6


5uS
200nS
TF
BIT
TO
PROG
5V
3144uS
GND

7

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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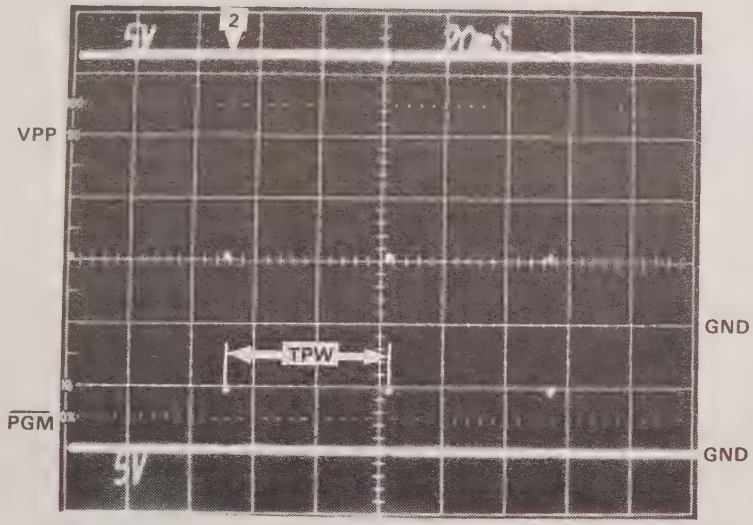
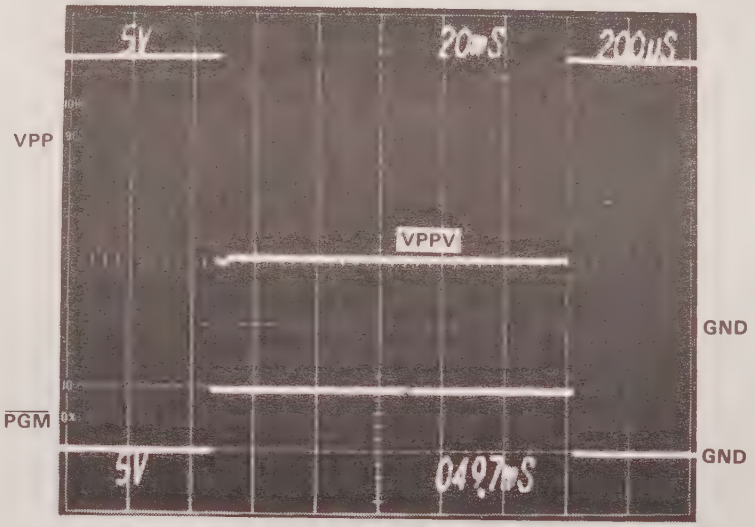
TIMING DIAGRAM

FAMILY CODES D3, D4

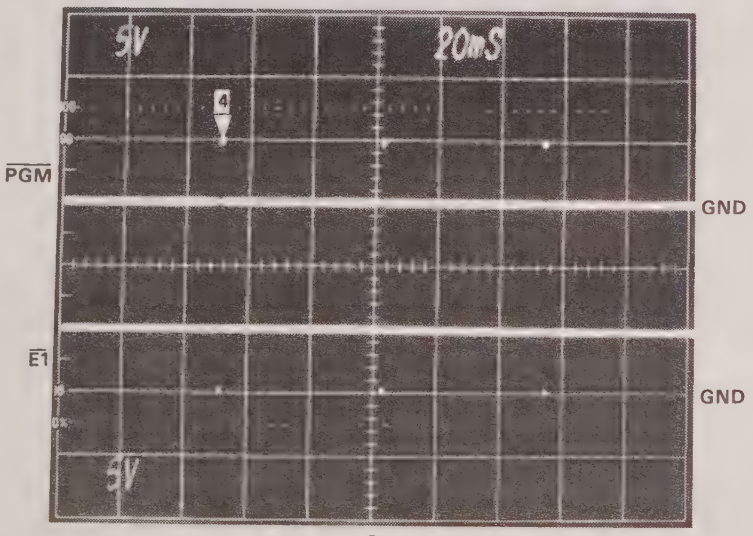
DATA I/O


5V
2
20mS
VPP
TPW
GND
PGM
GND
5V

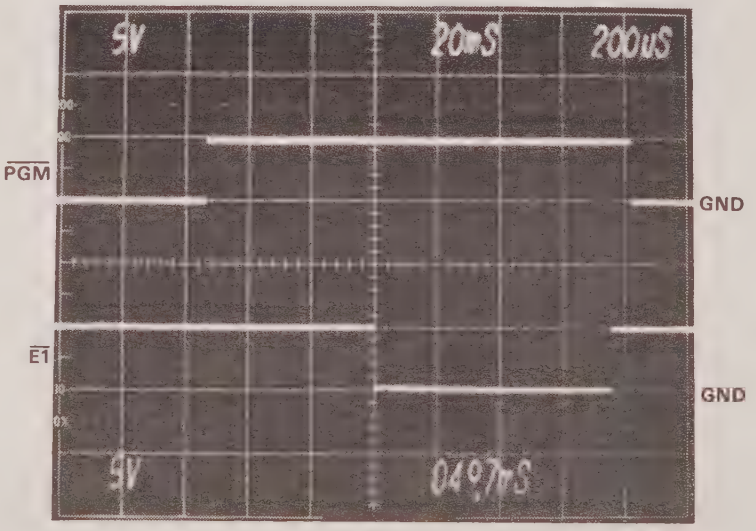
1


5V
20mS
200uS
VPP
VPPV
GND
PGM
GND
5V
049.7mS

2


5V
20mS
4
PGM
GND
E1
GND
5V

3


5V
20mS
200uS
PGM
GND
E1
GND
5V
049.7mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1655/TP2
	High Load	4.8	5.3	5.8	V	701-1655/TP4
	Low Load	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1655/TP2
	High Load	0.0	0.0	0.5	V	701-1655/TP4
	Low Load	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family D5.*
2. *Load RAM with hex 01 for Family D6 and bit-to-prog waveform becomes bit-no-prog waveform.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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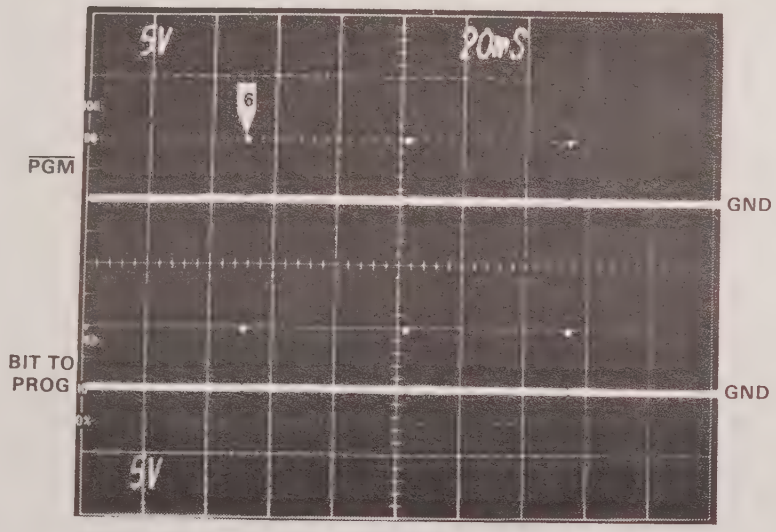
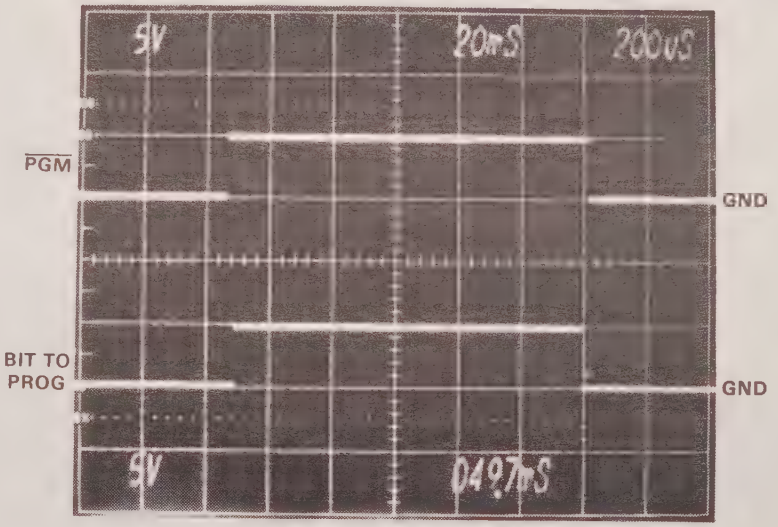
TIMING DIAGRAM

FAMILY CODES D5, D6

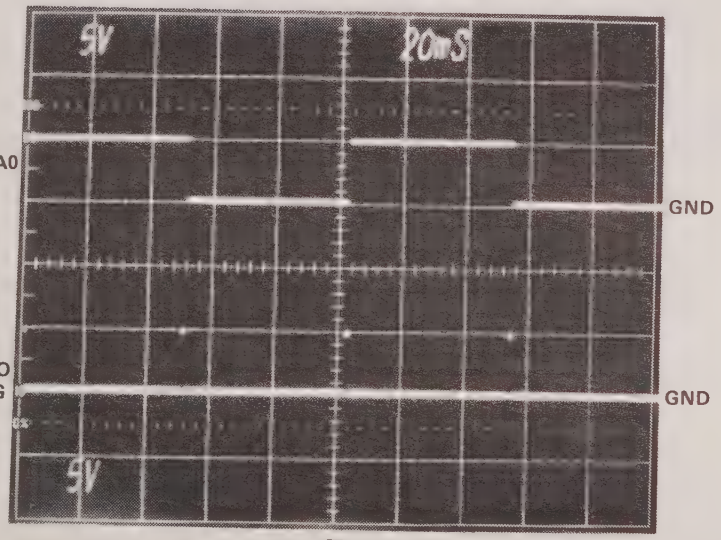
DATA I/O


5V
20mS
6
PGM
GND
BIT TO
PROG
GND
5V

5


5V
20mS
200uS
PGM
GND
BIT TO
PROG
GND
5V
049?mS

6


5V
20mS
A0
GND
BIT TO
PROG
GND
5V

7

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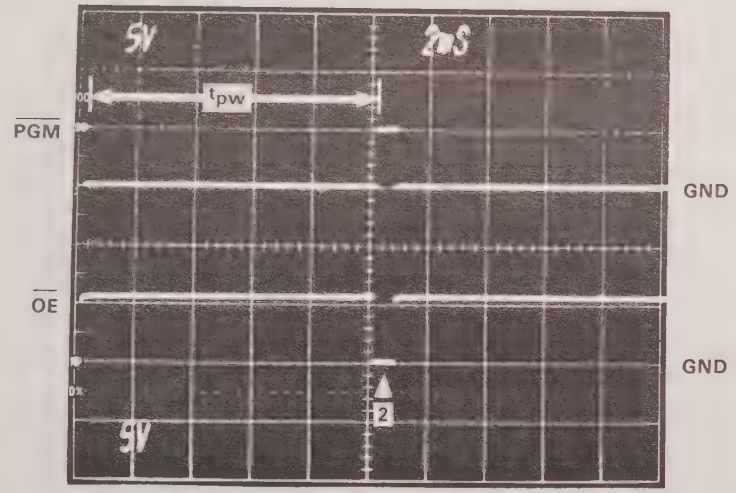
TIMING DIAGRAM

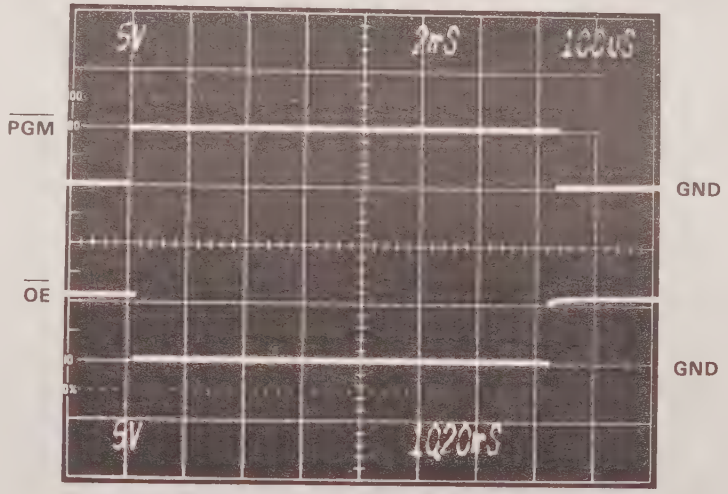
FAMILY CODES D5, D6

DATA I/O

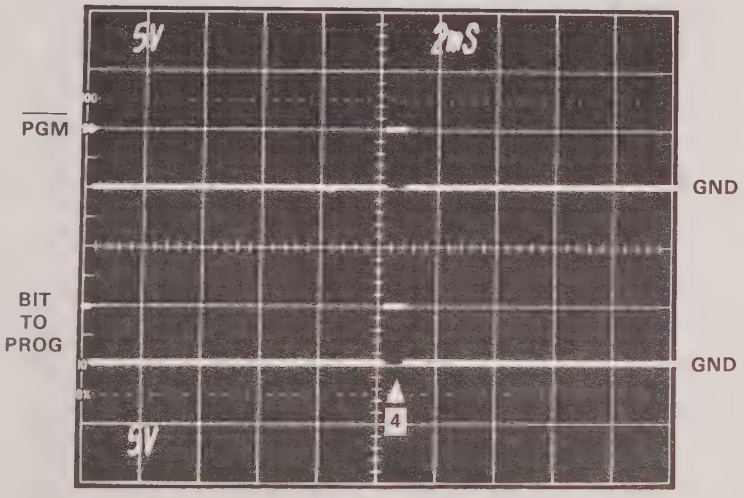
0526/1282


5V
2mS
t_{pw}
PGM
GND
OE
GND
5V
2

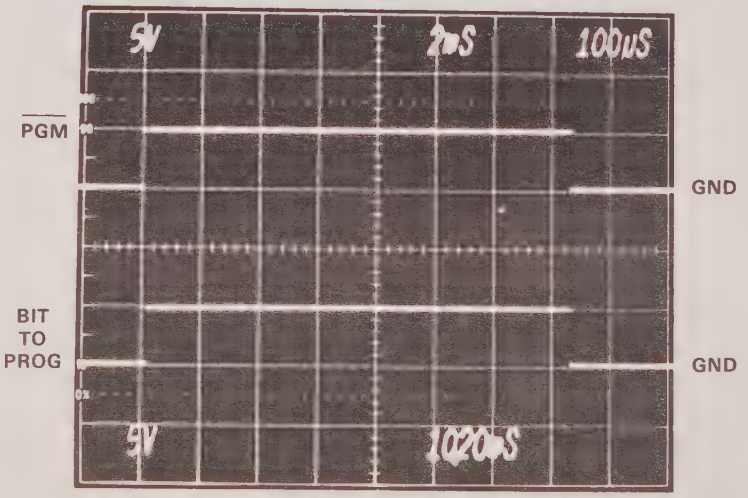
1


5V
2mS
100uS
PGM
GND
OE
GND
5V
1020mS

2


5V
2mS
PGM
GND
BIT
TO
PROG
GND
5V
4

3


5V
2mS
100uS
PGM
GND
BIT
TO
PROG
GND
5V
1020mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_{ew}	95	100	105	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	5.0	5.5	6.0	V	701-1655/TP4
	LOW LOAD	5.0	5.5	6.0	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	7.3	7.8	8.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family D7.*
2. *Load RAM with hex 01 for Family D8.*
3. *Photo 6 shows chip erase.*

REVISIONS

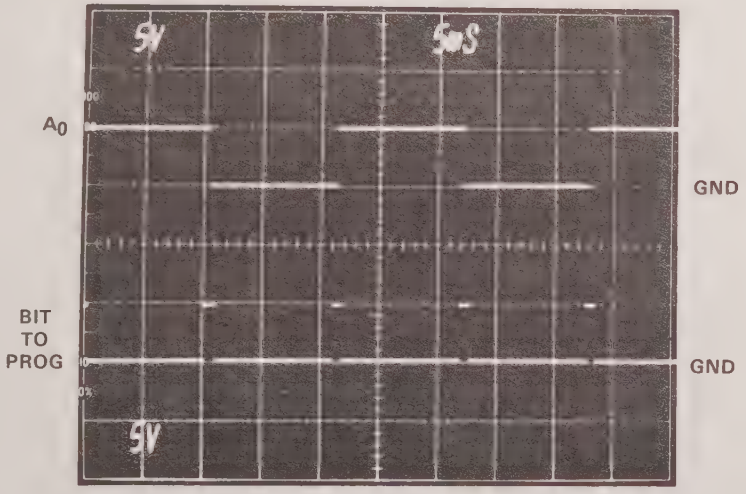
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	5/84

Sheet 1 of 2

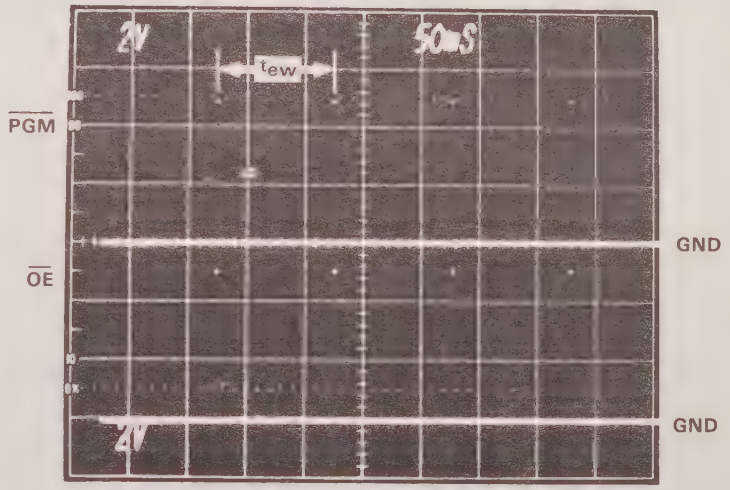
TIMING DIAGRAM

FAMILY CODES D7, D8

DATA I/O



5



6

B-253
10-950-0059

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

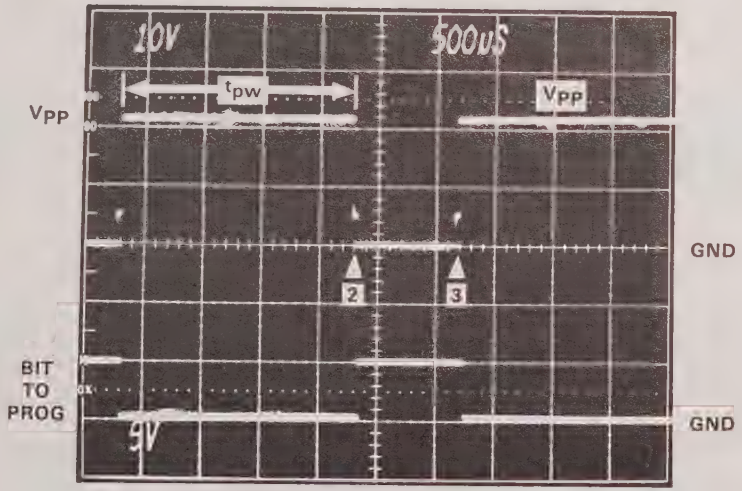
Sheet 2 of 2

TIMING DIAGRAM

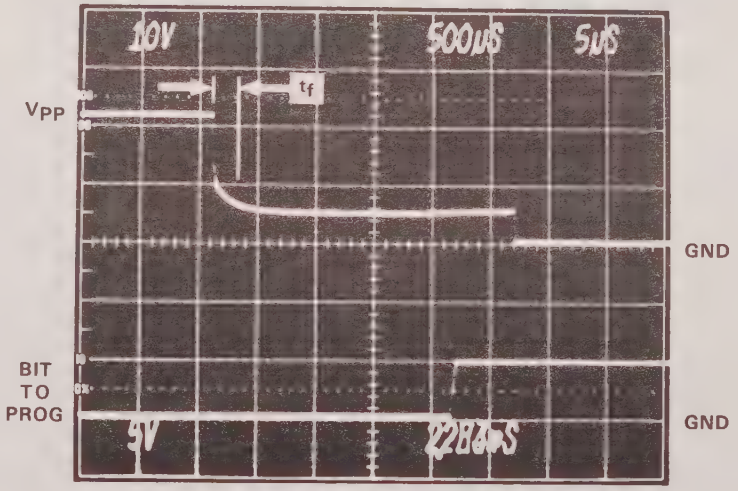
FAMILY CODES D7, D8

DATA I/O

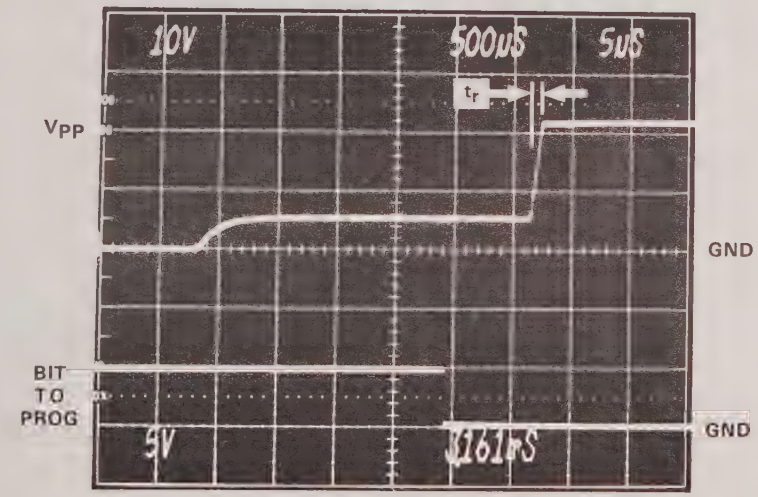
0526/1282


10V
500uS
t_{pw}
V_{PP}
V_{PP}
GND
2
3
BIT
TO
PROG
5V
GND

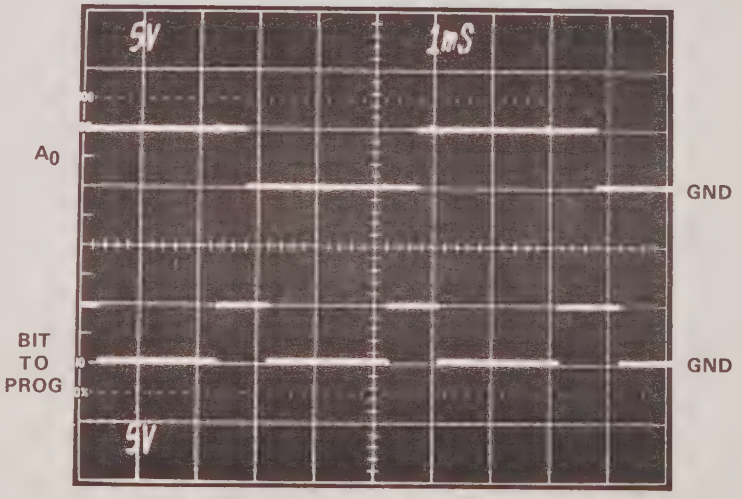
1


10V
500uS
5uS
t_f
V_{PP}
GND
BIT
TO
PROG
5V
GND

2


10V
500uS
5uS
t_r
V_{PP}
GND
BIT
TO
PROG
5V
GND

3


5V
1mS
A_0
GND
BIT
TO
PROG
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	20.5	21.0	21.5	V	
	V_{PPV}					N.A.
	t_{pw}	1.9	2.0	2.1	ms	
	t_r	0.5		2.0	μs	
	t_f	0.5		5.0	μs	
	Reject		20		PASSES	
	Overprogram		5		PASSES	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.4	0.5	0.6	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	6.5	7.0	7.5	V	701-1655/TP3

NOTES

1. Load RAM with hex FE for Family D9
2. Load RAM with hex 01 for Family DA.

REVISIONS

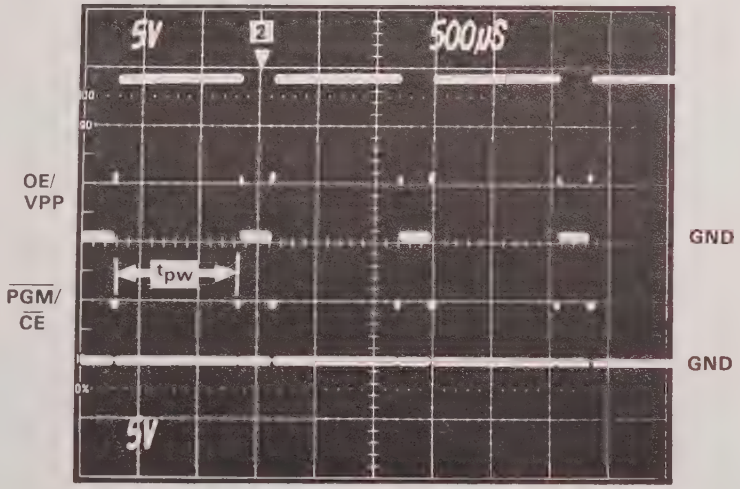
LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

Sheet 1 of 1

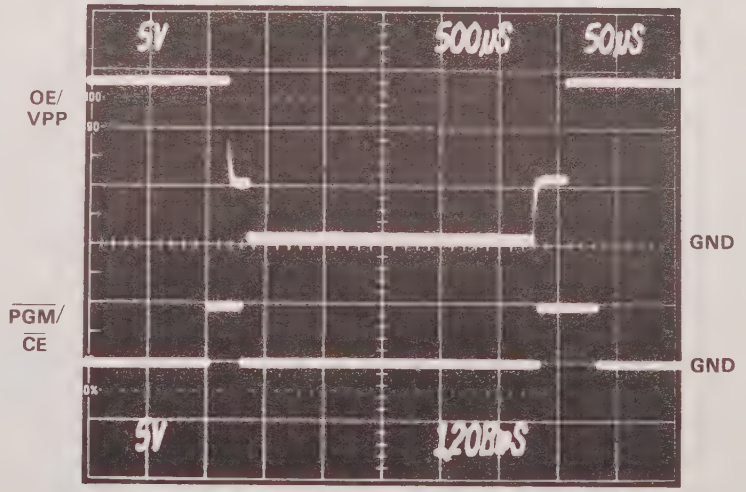
TIMING DIAGRAM

FAMILY CODES D9, DA

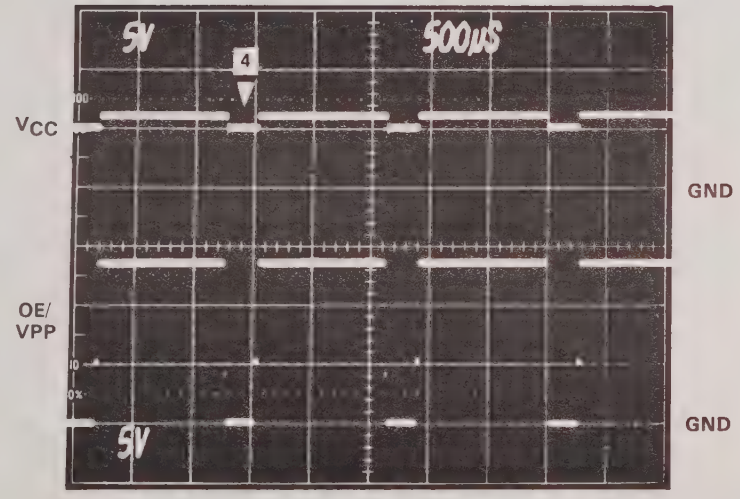
DATA I/O


5V
2
500µS
OE/
VPP
GND
tpw
PGM/
CE
GND
5V

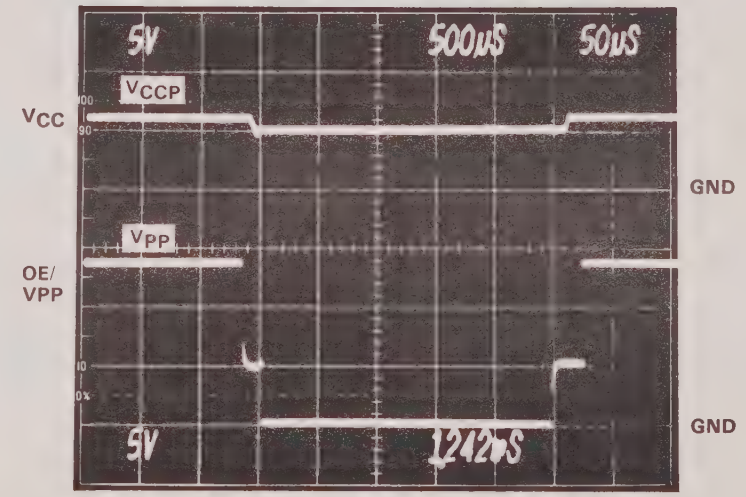
1


5V
500µS
50µS
OE/
VPP
GND
PGM/
CE
GND
5V
1208µS

2


5V
4
500µS
VCC
GND
OE/
VPP
GND
5V

3


5V
500µS
50µS
VCCP
VCC
GND
VPP
OE/
VPP
GND
5V
1242µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	12.5	13.0	13.5	V	
	V_{PPV}					N.A.
	t_{pw}		1		ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSES	
	Overprogram		1		PULSES	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1655/TP2
	HIGH LOAD	4.8	5.3	5.8	V	701-1655/TP4
	LOW LOAD	4.8	5.3	5.8	V	701-1655/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1655/TP2
	HIGH LOAD	0.0	0.0	0.5	V	701-1655/TP4
	LOW LOAD	4.3	4.8	5.3	V	701-1655/TP3

NOTES

1. *Load RAM with hex FE for Family DD.*
2. *Load RAM with hex 01 for Family DE.*

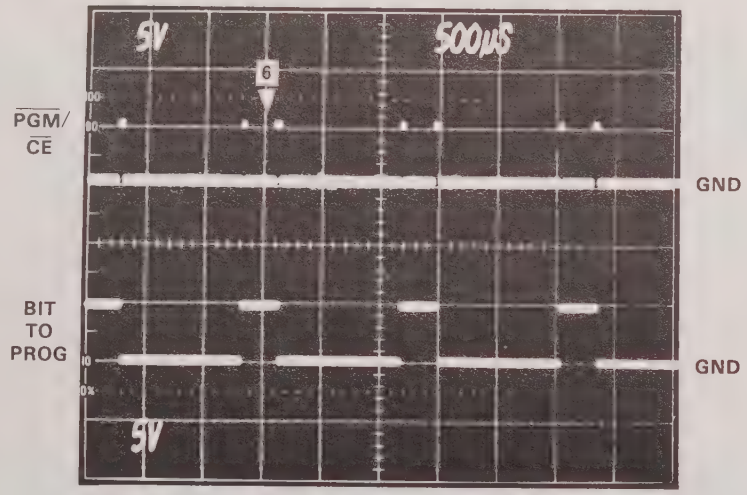
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

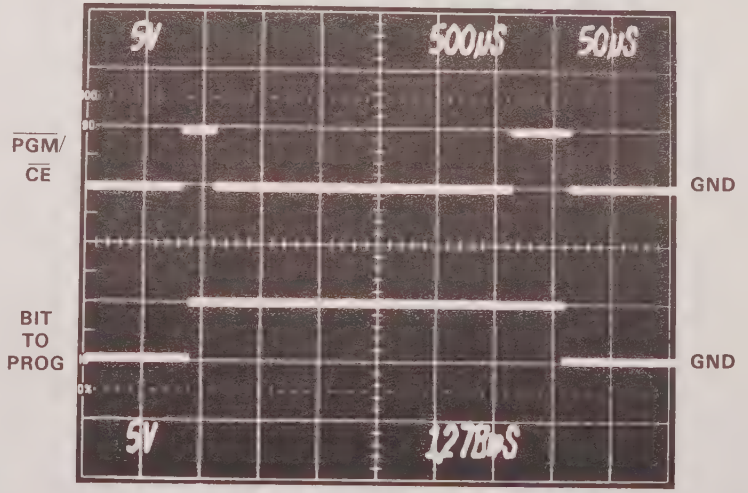
TIMING DIAGRAM

FAMILY CODES DD, DE

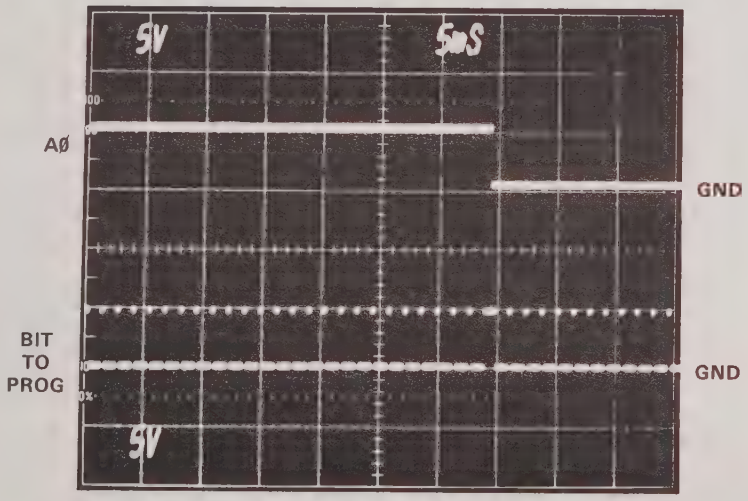
DATA I/O


5V
500µS
6
PGM/
CE
GND
BIT
TO
PROG
GND
5V

5


5V
500µS
50µS
PGM/
CE
GND
BIT
TO
PROG
GND
5V
127mS

6


5V
5mS
AØ
GND
BIT
TO
PROG
GND
5V

7

B-259
10-950-0059

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5023	CTJ	3/84

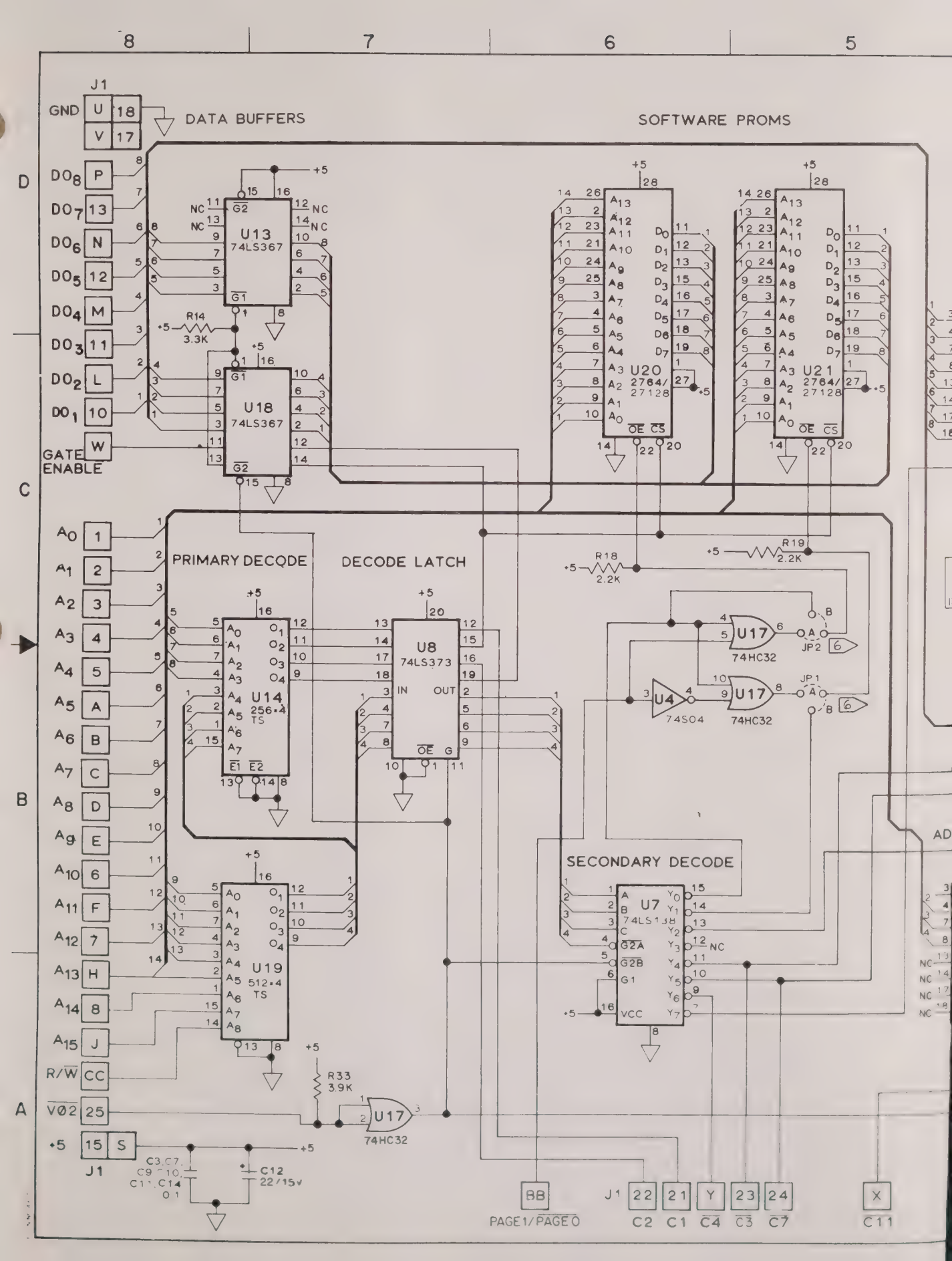
TIMING DIAGRAM

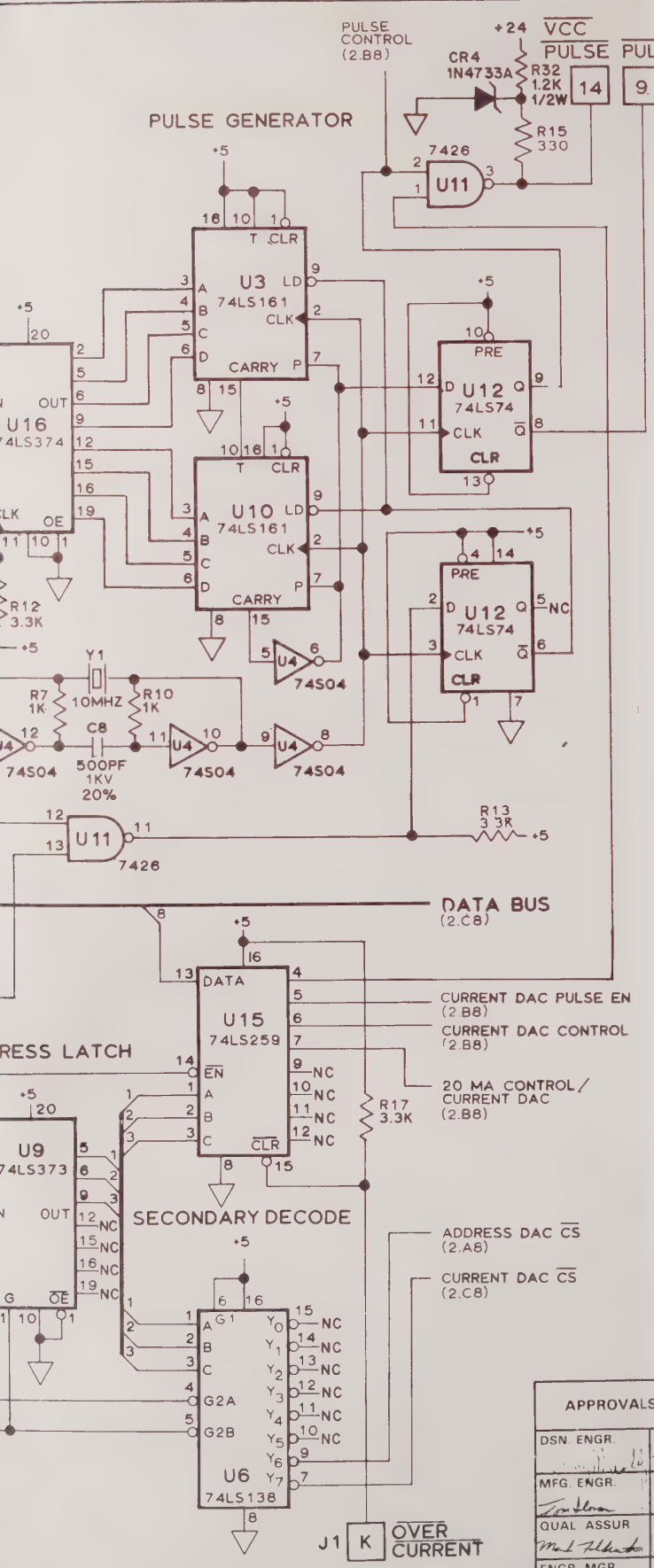
FAMILY CODES DD, DE

DATA I/O

APPENDIX C
SCHEMATICS

30-702-1650	Rev E	Memory Card
30-701-1655	Rev B	Address Card
30-702-1659	Rev D	Socket Card
30-702-1661	Rev A	Motherboard
30-701-1690	Rev A	Waveform Generator


8
7
6
5
D
C
B
A
J1
GND
U
18
V
17
DATA BUFFERS
SOFTWARE PROMS
DO8 P
DO7 13
DO6 N
DO5 12
DO4 M
DO3 11
DO2 L
DO1 10
GATE ENABLE W
U13
74LS367
U18
74LS367
R14
3.3K
+5
U20
2764/
27128
U21
2764/
27128
A0 1
A1 2
A2 3
A3 4
A4 5
A5 A
A6 B
A7 C
A8 D
A9 E
A10 6
A11 F
A12 7
A13 H
A14 8
A15 J
R/W CC
VØ2 25
+5 15 S
J1
PRIMARY DECODE
DECODE LATCH
U14
256•4
TS
U8
74LS373
U19
512•4
TS
R18
2.2K
R19
2.2K
U17
74HC32
U4
74S04
JP1
JP2
SECONDARY DECODE
U7
74LS138
R33
3.9K
C3,C7,
C9,C10,
C11,C14
01
C12
22/15v
BB
PAGE1/PAGE0
J1 22 21 Y 23 24
C2 C1 C4 C3 C7
X
C11



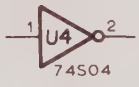
REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	MP/AK			1/22
B	ECN 4760	CL		C78	2/83
C	ECN 4768	CL		C78	2/83
D	ECN 4827	CL		C78	5/83
E	ECN 4889	BV		C78	4/84

NOTES: UNLESS OTHERWISE SPECIFIED.

1. RESISTORS ARE 1/4W AND IN OHMS, 5%
2. CAPACITORS ARE 50V AND IN MICROFARADS 10%.
3. LAST REFERENCE DESIGNATORS USED:
   R33, C14, CR4, VR3, U23, Q3, Y1, JP2
   REFERENCE DESIGNATORS NOT USED:
   U1, R22, R23
4. CONNECTIONS NOT SHOWN:

I.C. NO.	+5	GND
U4	14	7
U11	14	7
U17	14	7

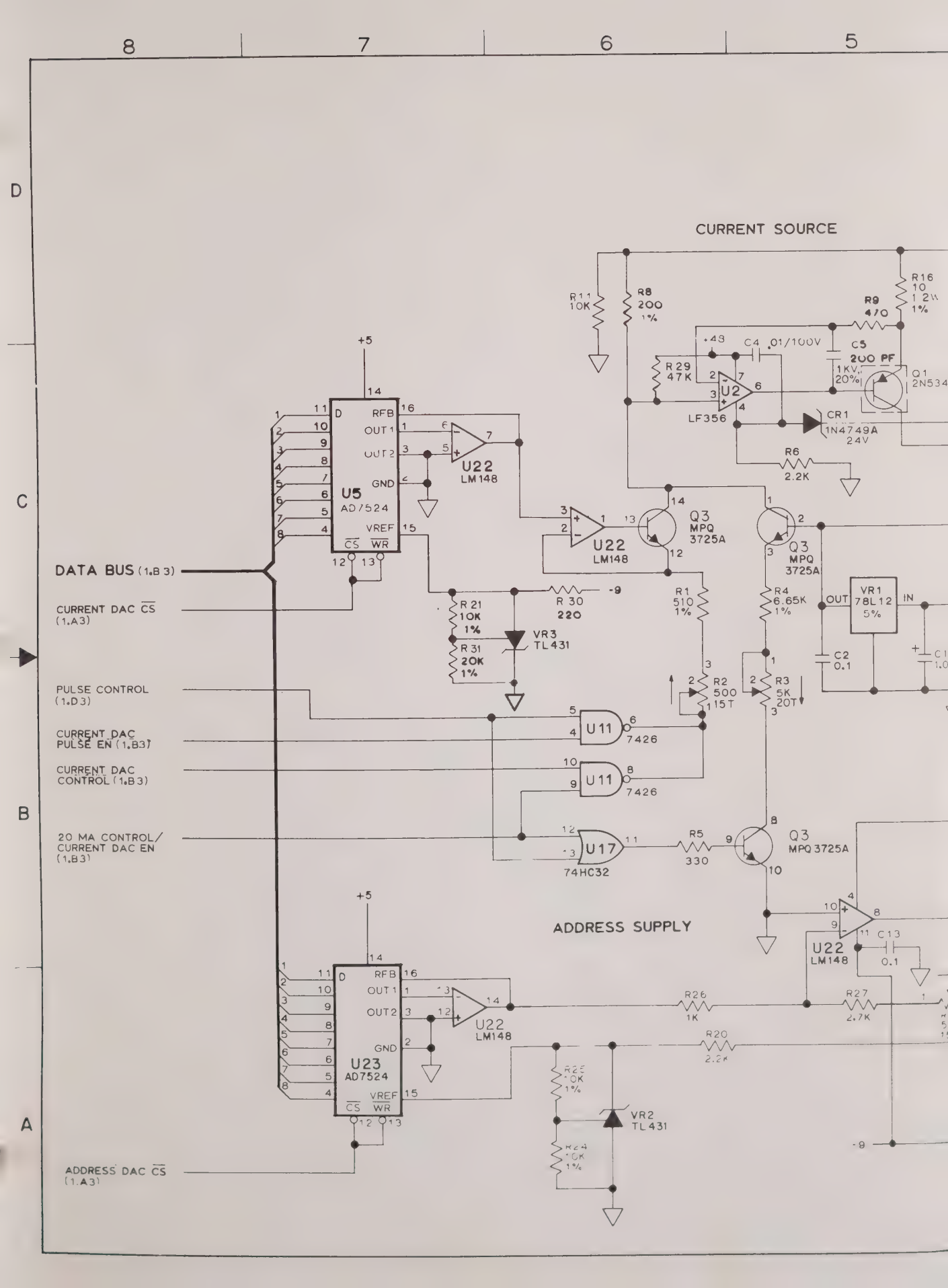
5. UNUSED GATES:



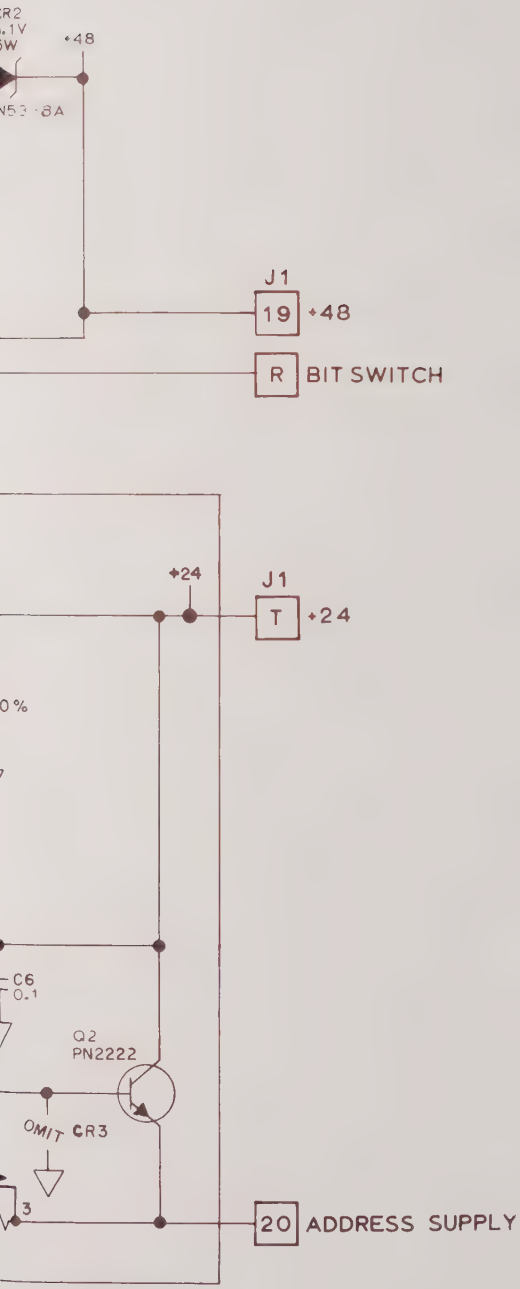
6 -002 INSTALL JP1 AND JP2 IN POSITION B,
-003 INSTALL JP1 AND JP2 IN POSITION A.

702-1650-002 SHOWN
702-1650-003 AS NOTED

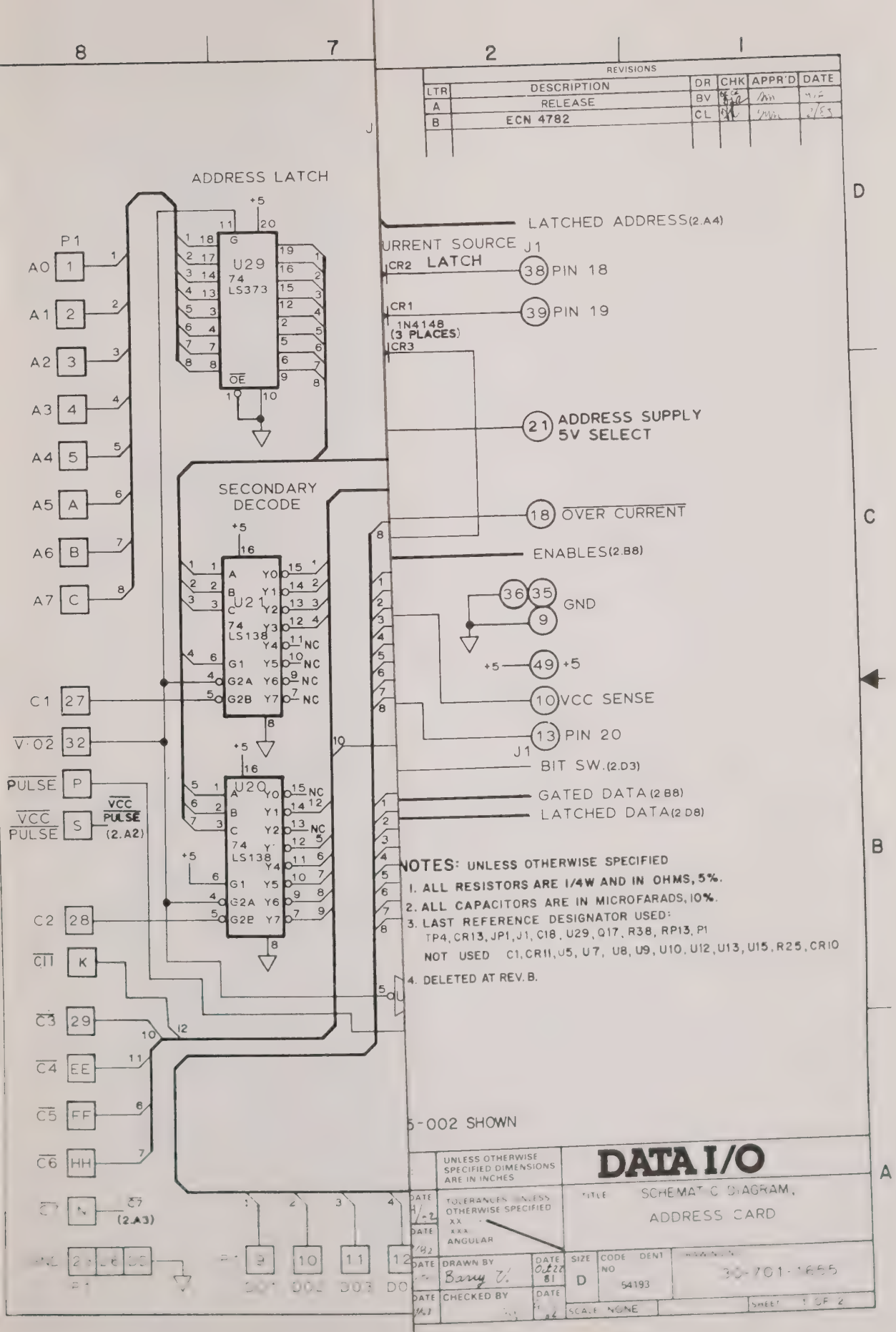
APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.	DATA I/O	
DSN. ENGR.	DATE 1/22	TOLERANCES, UNLESS OTHERWISE SPECIFIED .XX ± .XXX ANGULAR	TITLE SCHEMATIC DIAGRAM, MEMORY BOARD	
MFG. ENGR.	DATE 9/82			
QUAL ASSUR	DATE 9/82	DRAWN BY KONG	DATE 3/17/82	SIZE D / CODE IDENT NO 54193 / DRAWING NO 30-702-1650
ENGR MGR	DATE 9/82	CHECKED BY: BK CHK: BJK	DATE 9/14/82	SCALE NONE / SHEET 1 OF 2


8
7
6
5
D
C
B
A
CURRENT SOURCE
R11 10K
R8 200 1%
R16 10 1.2W 1%
R9 470
+48
C4 .01/100V
C5 200 PF 1KV, 20%
R29 47K
U2
LF356
Q1 2N534
CR1 1N4749A 24V
R6 2.2K
+5
U5 AD7524
RFB
OUT1
OUT2
GND
VREF
CS WR
U22 LM148
Q3 MPQ 3725A
DATA BUS (1.B3)
CURRENT DAC CS (1.A3)
R21 10K 1%
R31 20K 1%
R30 220
VR3 TL431
R1 510 1%
R4 6.65K 1%
VR1 78L12 5%
OUT
IN
C2 0.1
R2 500 15T
R3 5K 20T
PULSE CONTROL (1.D3)
CURRENT DAC PULSE EN (1.B3)
CURRENT DAC CONTROL (1.B3)
U11 7426
20 MA CONTROL/ CURRENT DAC EN (1.B3)
U17 74HC32
R5 330
ADDRESS SUPPLY
C13 0.1
R26 1K
R27 2.7K
R20 2.2K
U23 AD7524
R25 10K 1%
R24 10K 1%
VR2 TL431
ADDRESS DAC CS (1.A3)

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
	SEE SHEET ONE				



APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
DSN ENGR	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED XX ± XXX ± ANGULAR	TITLE: SCHEMATIC DIAGRAM, MEMORY BOARD	
MFG ENGR	DATE			
QUAL. ASSUR.	DATE	DRAWN BY: KONG	DATE: 2/22/82	SIZE: D; CODE IDENT NO: 54193; DRAWING NO: 30-702-1650
ENGR. MGR.	DATE	CHECKED BY:	DATE	SCALE: NONE; SHEET 2 OF 2

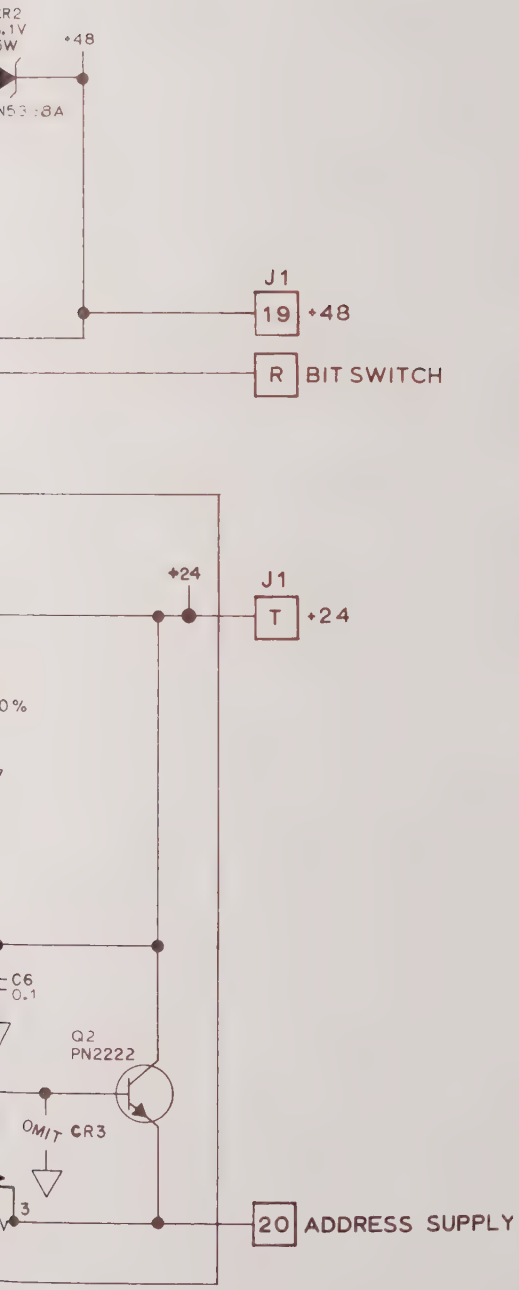


REVISIONS
LTR DESCRIPTION DR CHK APPR'D DATE
A RELEASE BV
B ECN 4782 CL
ADDRESS LATCH
U29 74 LS373
P1
A0 A1 A2 A3 A4 A5 A6 A7
LATCHED ADDRESS(2.A4)
URRENT SOURCE LATCH
CR2 CR1 CR3
1N4148 (3 PLACES)
J1
38 PIN 18
39 PIN 19
21 ADDRESS SUPPLY 5V SELECT
18 OVER CURRENT
ENABLES(2.B8)
36 35 9 GND
49 +5
10 VCC SENSE
13 PIN 20
BIT SW.(2.D3)
GATED DATA(2.B8)
LATCHED DATA(2.D8)
SECONDARY DECODE
U21 74 LS138
U20 74 LS138
C1 27
V·02 32
PULSE P
VCC PULSE S
VCC PULSE (2.A2)
C2 28
C11 K
C3 29
C4 EE
C5 FF
C6 HH
C7 N
C7 (2.A3)
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 10%.
3. LAST REFERENCE DESIGNATOR USED:
TP4, CR13, JP1, J1, C18, U29, Q17, R38, RP13, P1
NOT USED C1, CR11, U5, U7, U8, U9, U10, U12, U13, U15, R25, CR10
4. DELETED AT REV. B.
5-002 SHOWN
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE SPECIFIED
XX
XXX
ANGULAR
DATA I/O
TITLE SCHEMATIC DIAGRAM, ADDRESS CARD
DRAWN BY Barry V.
DATE Oct 27 81
CHECKED BY
SIZE D
CODE IDENT NO 54193
30-701-1655
SCALE NONE
SHEET 1 OF 2

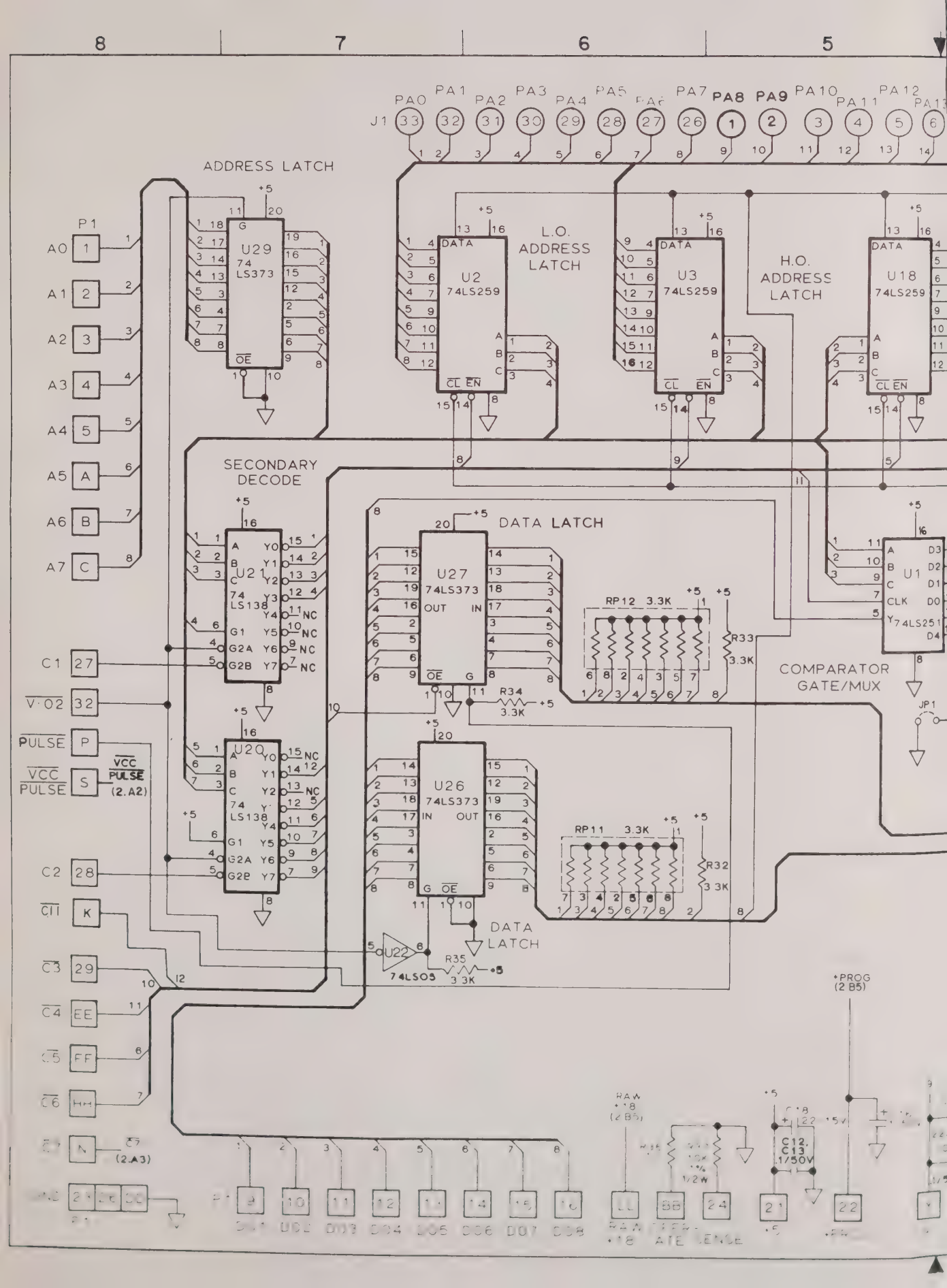
4 3 2 1

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
	SEE SHEET ONE				

D C B A

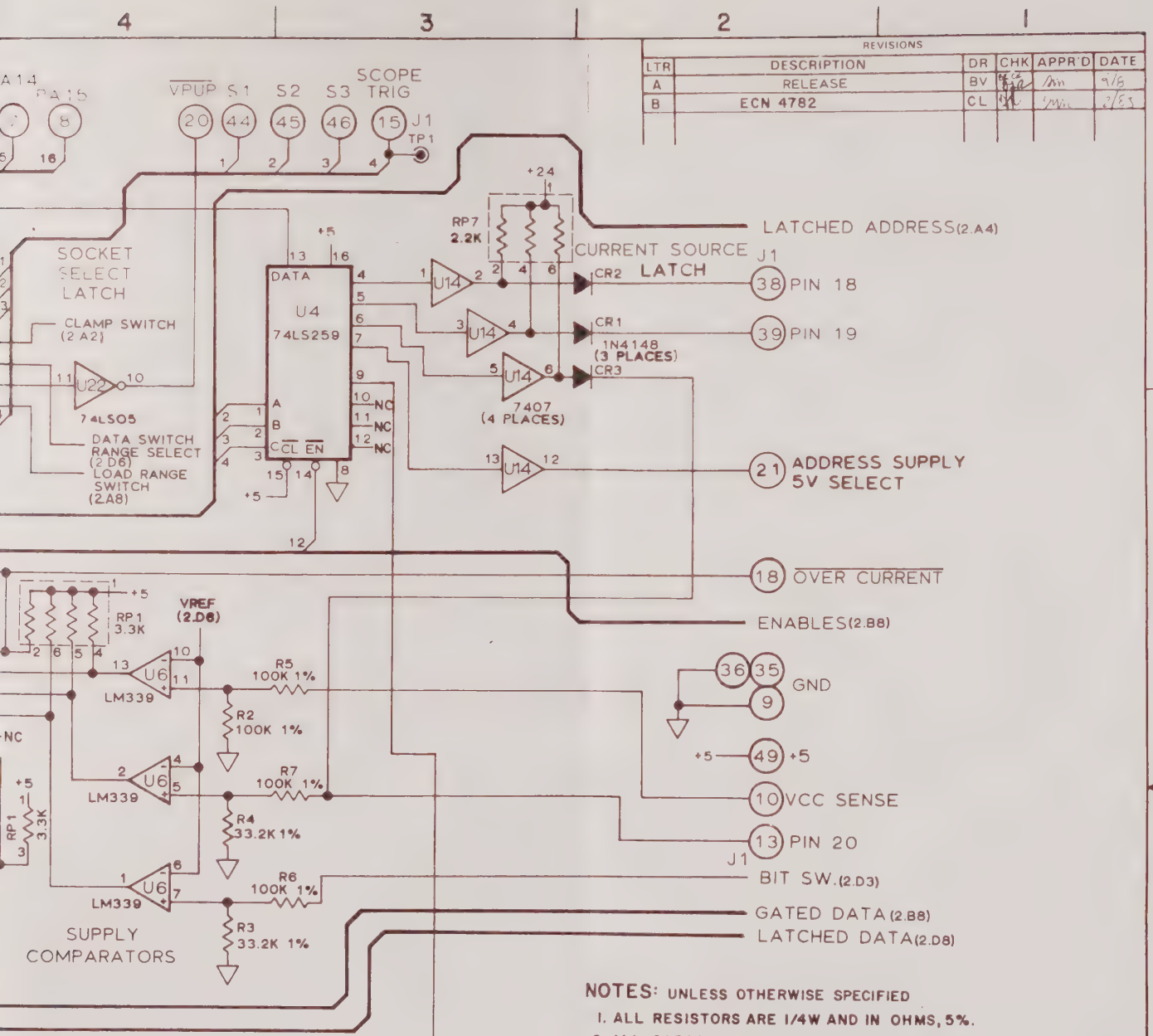


APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O	
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED XX - XXX - ANGULAR		TITLE SCHEMATIC DIAGRAM, MEMORY BOARD	
MFG ENGR	DATE				
QUAL ASSUR	DATE	DRAWN BY KONG	DATE 2/22/82	SIZE D	CODE INDENT NO 54193
ENGR MGR	DATE	CHECKED BY	DATE	DRAWING NO 30-702-1650	
				SCALE NONE	SHEET 2 OF 2



8
7
6
5
J1
PA0
PA1
PA2
PA3
PA4
PA5
PA7
PA8
PA9
PA10
PA11
PA12
ADDRESS LATCH
U29
74
LS373
L.O.
ADDRESS
LATCH
U2
74LS259
H.O.
ADDRESS
LATCH
U3
74LS259
U18
74LS259
P1
A0
A1
A2
A3
A4
A5
A6
A7
SECONDARY
DECODE
U21
74
LS138
U20
74
LS138
DATA LATCH
U27
74LS373
U26
74LS373
RP12 3.3K
R33
3.3K
R34
3.3K
RP11 3.3K
R32
3.3K
R35
3.3K
U22
74LS05
DATA
LATCH
U1
74LS251
COMPARATOR
GATE/MUX
JP1
C1
V·02
PULSE
VCC
PULSE
(2.A2)
C2
C3
C4
C5
C6
C7
(2.A3)
+PROG
(2 B5)
RAW
+18
(2 B5)
C12,
C13
1/50V

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	BV	[illegible]	[illegible]	9/8
B	ECN 4782	CL	[illegible]	[illegible]	2/83



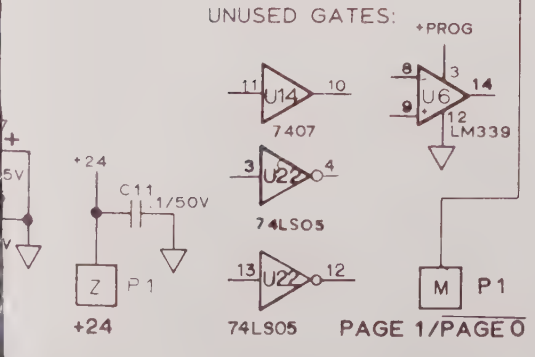
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 10%.
3. LAST REFERENCE DESIGNATOR USED:
   TP4, CR13, JP1, J1, C18, U29, Q17, R38, RP13, P1
   NOT USED C1, CR11, U5, U7, U8, U9, U10, U12, U13, U15, R25, CR10
4. DELETED AT REV. B.

NOT SHOWN

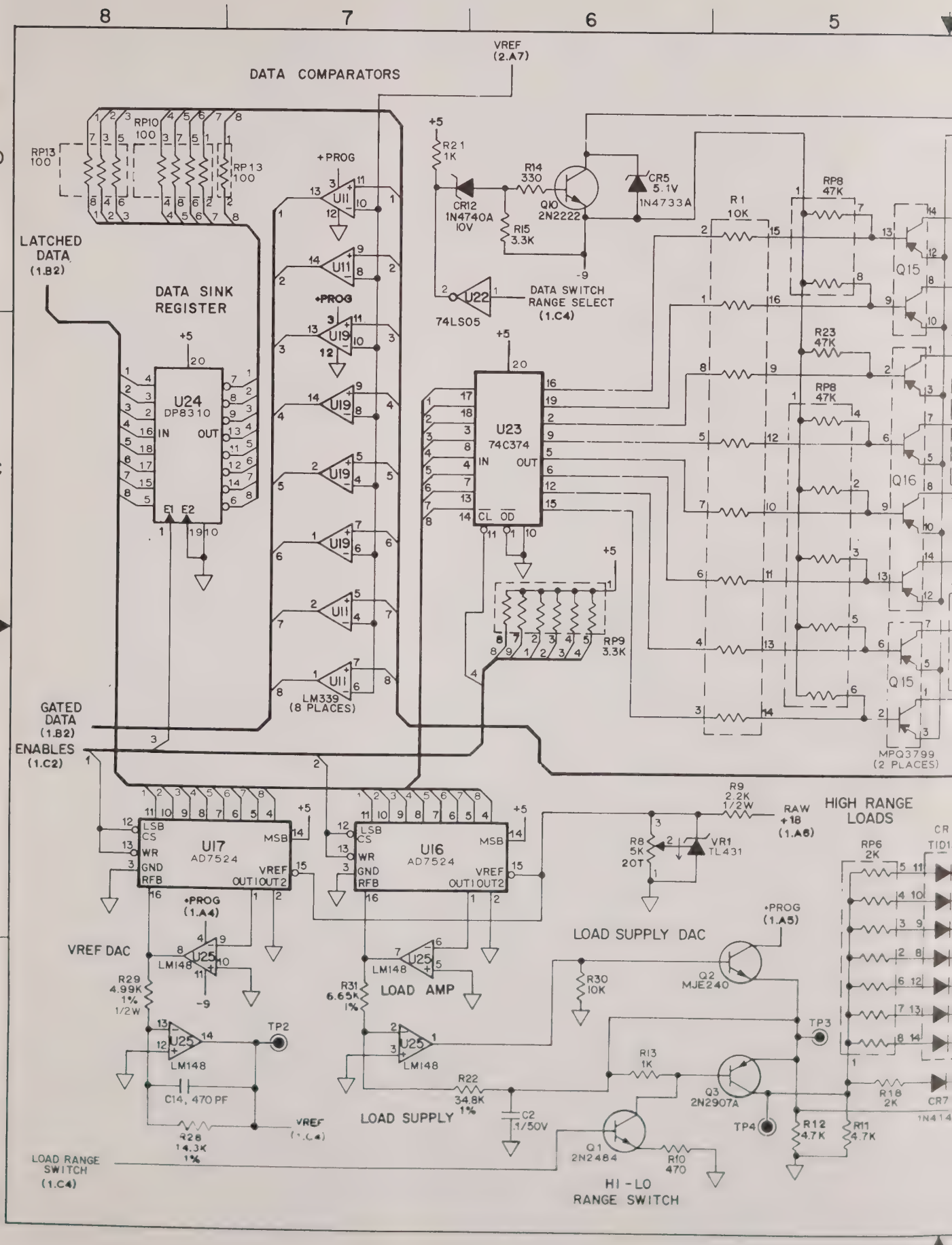
IC. NO.	+5	GND
U22	PIN14	PIN7
U14	PIN14	PIN7

UNUSED GATES:

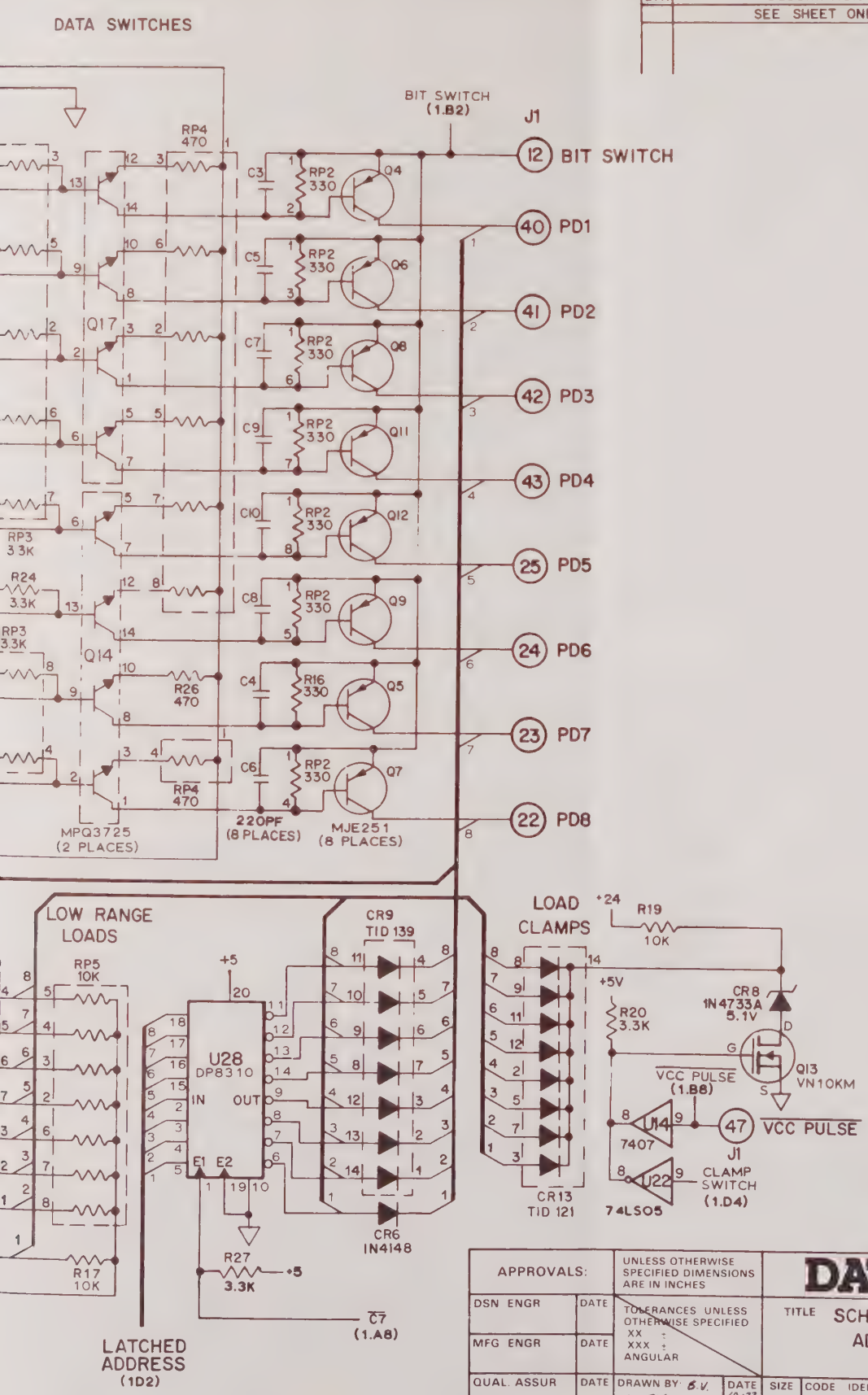


30-701-1655-002 SHOWN

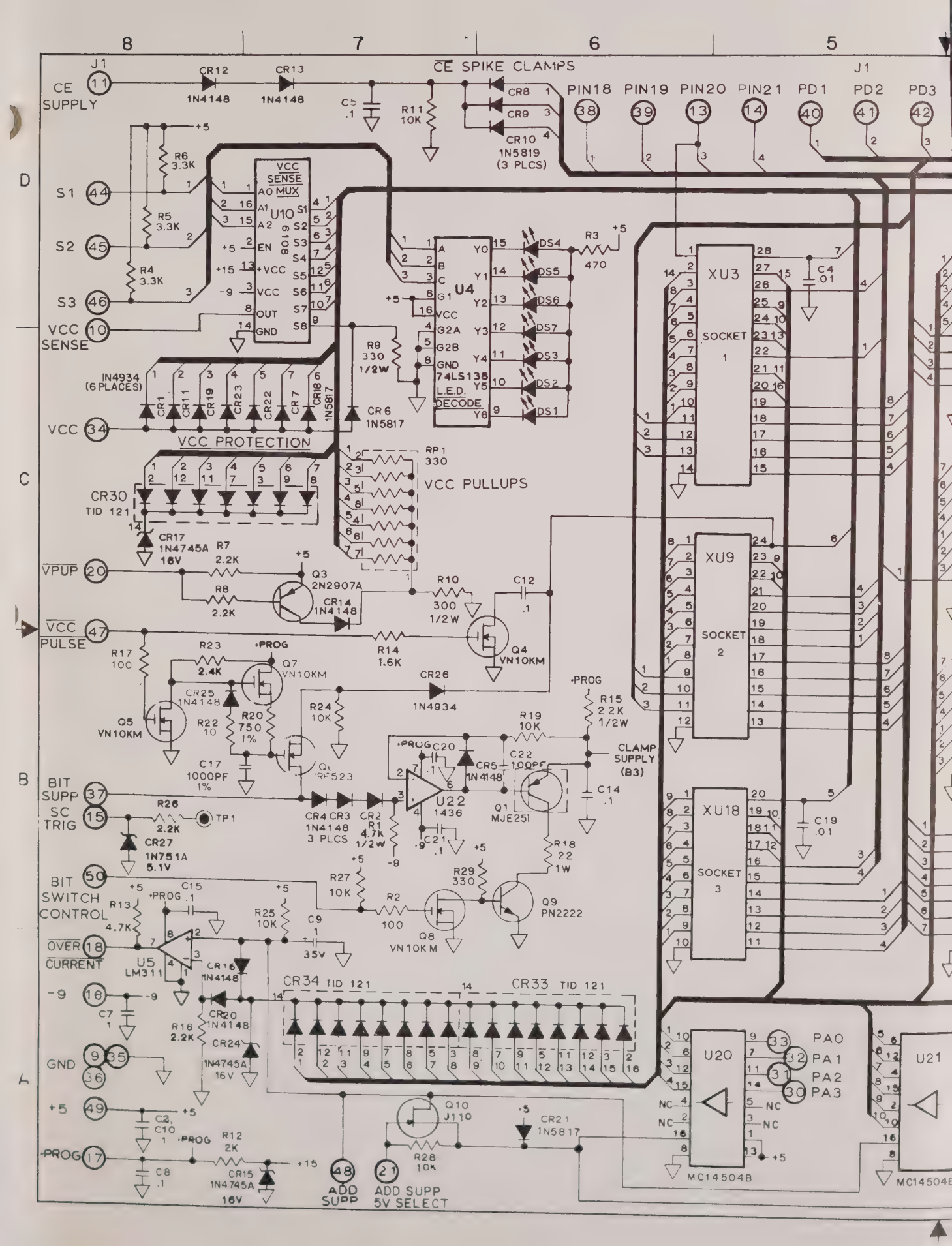
APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O
DSN ENGR [illegible]	DATE 4/82	TOLERANCES UNLESS OTHERWISE SPECIFIED XX - XXX - ANGULAR	TITLE SCHEMATIC DIAGRAM, ADDRESS CARD
MFG ENGR [illegible]	DATE 9/82		
QUAL ASSUR [illegible]	DATE [illegible]	DRAWN BY Barry V. DATE Oct 22 81	SIZE D · CODE IDENT NO 54193 · DRAWING NO 30-701-1655
ENGR MGR. [illegible]	DATE 9/82	CHECKED BY [illegible] DATE 4/12 82	SCALE NONE · SHEET 1 OF 2

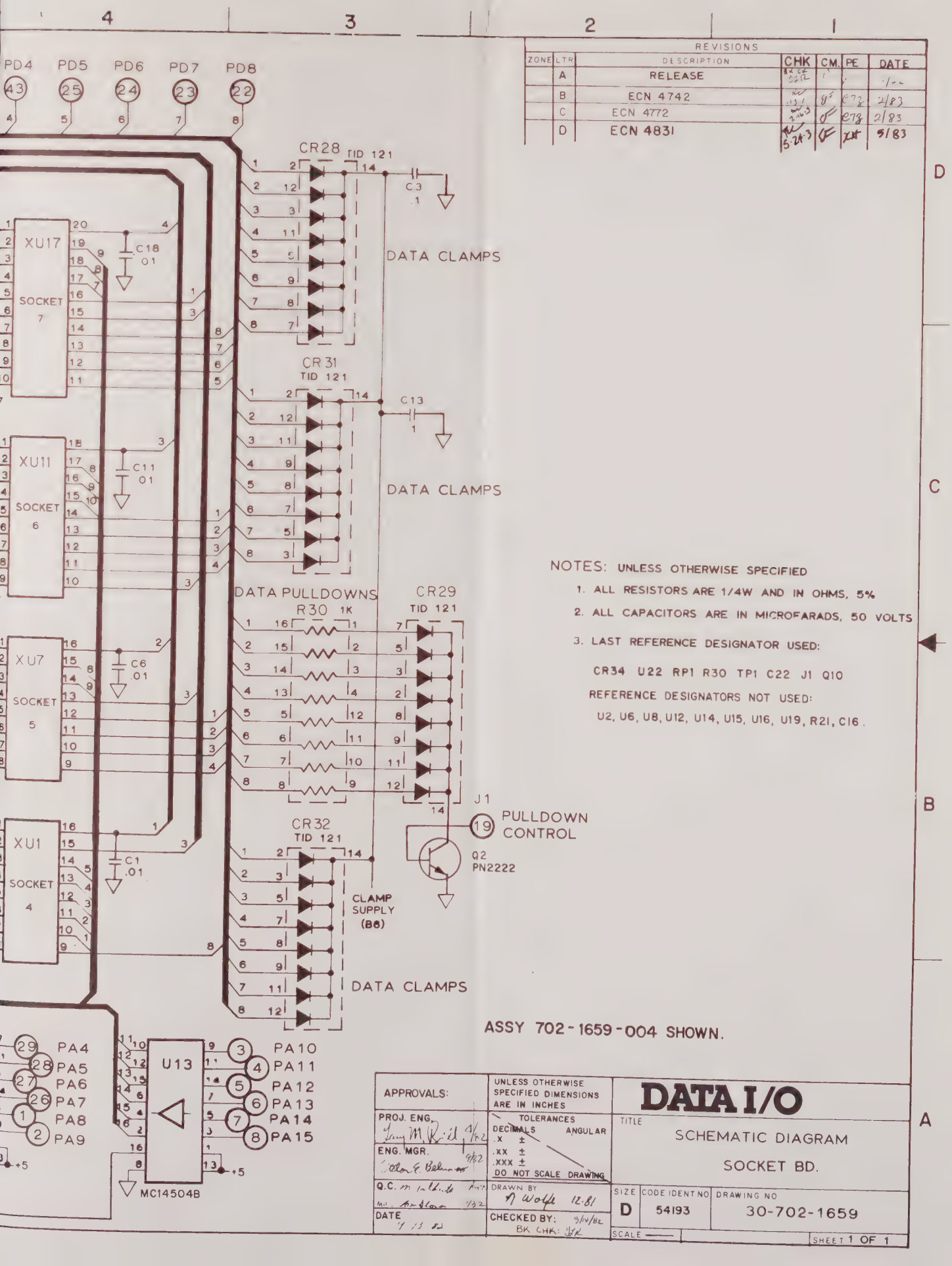

8
7
6
5
D
C
B
A
DATA COMPARATORS
VREF (2.A7)
RP10 100
RP13 100
RP13 100
+PROG
U11
U19
LM339 (8 PLACES)
LATCHED DATA (1.B2)
DATA SINK REGISTER
U24 DP8310
IN
OUT
E1 E2
+5
R21 1K
CR12 1N4740A 10V
R14 330
R15 3.3K
Q10 2N2222
CR5 5.1V 1N4733A
-9
U22
74LS05
DATA SWITCH RANGE SELECT (1.C4)
U23 74C374
CL OD
R1 10K
RP8 47K
R23 47K
Q15
Q16
MPQ3799 (2 PLACES)
RP9 3.3K
GATED DATA (1.B2)
ENABLES (1.C2)
U17 AD7524
U16 AD7524
LSB
MSB
CS
WR
GND
RFB
VREF
OUT1
OUT2
R9 2.2K 1/2W
RAW +18 (1.A6)
R8 5K 20T
VR1 TL431
HIGH RANGE LOADS
RP6 2K
CR TID1
+PROG (1.A4)
+PROG (1.A5)
VREF DAC
LOAD SUPPLY DAC
LM148
R29 4.99K 1% 1/2W
R31 6.65K 1%
LOAD AMP
R30 10K
Q2 MJE240
TP2
TP3
R13 1K
Q3 2N2907A
C14, 470 PF
R22 34.8K 1%
LOAD SUPPLY
C2 1/50V
TP4
R12 4.7K
R11 4.7K
R18 2K
CR7 1N414
R28 14.3K 1%
VREF (1.C4)
Q1 2N2484
R10 470
LOAD RANGE SWITCH (1.C4)
HI-LO RANGE SWITCH

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
	SEE SHEET ONE	BV/RB	BK CK DKR	CTZ	2/83



APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O
DSN ENGR	DATE	TOLERANCES UNLESS OTHERWISE SPECIFIED XX ± XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, ADDRESS CARD
MFG ENGR	DATE		
QUAL. ASSUR	DATE	DRAWN BY B.V. G RYDER DATE 10-22 1981	SIZE D · CODE IDENT NO 54193 · DRAWING NO 30-701-1655
ENGR. MGR.	DATE	CHECKED BY DATE	SCALE NONE · SHEET 2 OF 2


8
7
6
5
CE SPIKE CLAMPS
J1
CE SUPPLY
CR12
CR13
1N4148
1N4148
C5 .1
R11 10K
CR8
CR9
CR10
1N5819 (3 PLCS)
PIN18
PIN19
PIN20
PIN21
PD1
PD2
PD3
S1
S2
S3
VCC SENSE
R6 3.3K
R5 3.3K
R4 3.3K
VCC SENSE
A0 MUX
U10
8108
EN
+VCC
VCC
OUT
GND
S1
S2
S3
S4
S5
S6
S7
S8
U4
74LS138
L.E.D. DECODE
DS4
DS5
DS6
DS7
DS3
DS2
DS1
R3 470
R9 330 1/2W
IN4934 (6 PLACES)
CR1
CR11
CR19
CR23
CR22
CR7
CR18 1N5817
CR6 1N5817
VCC
VCC PROTECTION
RP1 330
VCC PULLUPS
CR30 TID 121
CR17 1N4745A 16V
R7 2.2K
R8 2.2K
VPUP
Q3 2N2907A
CR14 1N4148
R10 300 1/2W
C12 .1
Q4 VN10KM
VCC PULSE
R14 1.6K
R17 100
R23 2.4K
PROG
Q7 VN10KM
Q5 VN10KM
CR25 1N4148
R22 10
R20 750 1%
C17 1000PF 1%
R24 10K
CR26 1N4934
R15 22K 1/2W
R19 10K
CLAMP SUPPLY (B3)
C14 .1
C22 100PF
Q1 MJE251
CR5 1N4148
C20 .1
U22 1436
C21 .1
R18 22 1W
BIT SUPP
SC TRIG
R26 2.2K
TP1
CR27 1N751A 5.1V
CR4 CR3 CR2 1N4148 3 PLCS
R1 4.7K 1/2W
BIT SWITCH CONTROL
R27 10K
R29 330
Q9 PN2222
R2 100
Q8 VN10KM
R13 4.7K
C15 .1
R25 10K
C9 1 35V
U5 LM311
OVER CURRENT
CR16 1N4148
CR20 1N4148
R16 2.2K
CR24 1N4745A 16V
CR34 TID 121
CR33 TID 121
-9
C7 1
GND
+5
C2, C10 1
C8 .1
R12 2K
CR15 1N4745A 16V
+15
Q10 J110
R28 10K
CR21 1N5817
ADD SUPP
ADD SUPP 5V SELECT
XU3
XU9
XU18
SOCKET 1
SOCKET 2
SOCKET 3
C4 .01
C19 .01
U20
U21
PA0
PA1
PA2
PA3
NC
MC14504B
MC14504B



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%
2. ALL CAPACITORS ARE IN MICROFARADS, 50 VOLTS
3. LAST REFERENCE DESIGNATOR USED:

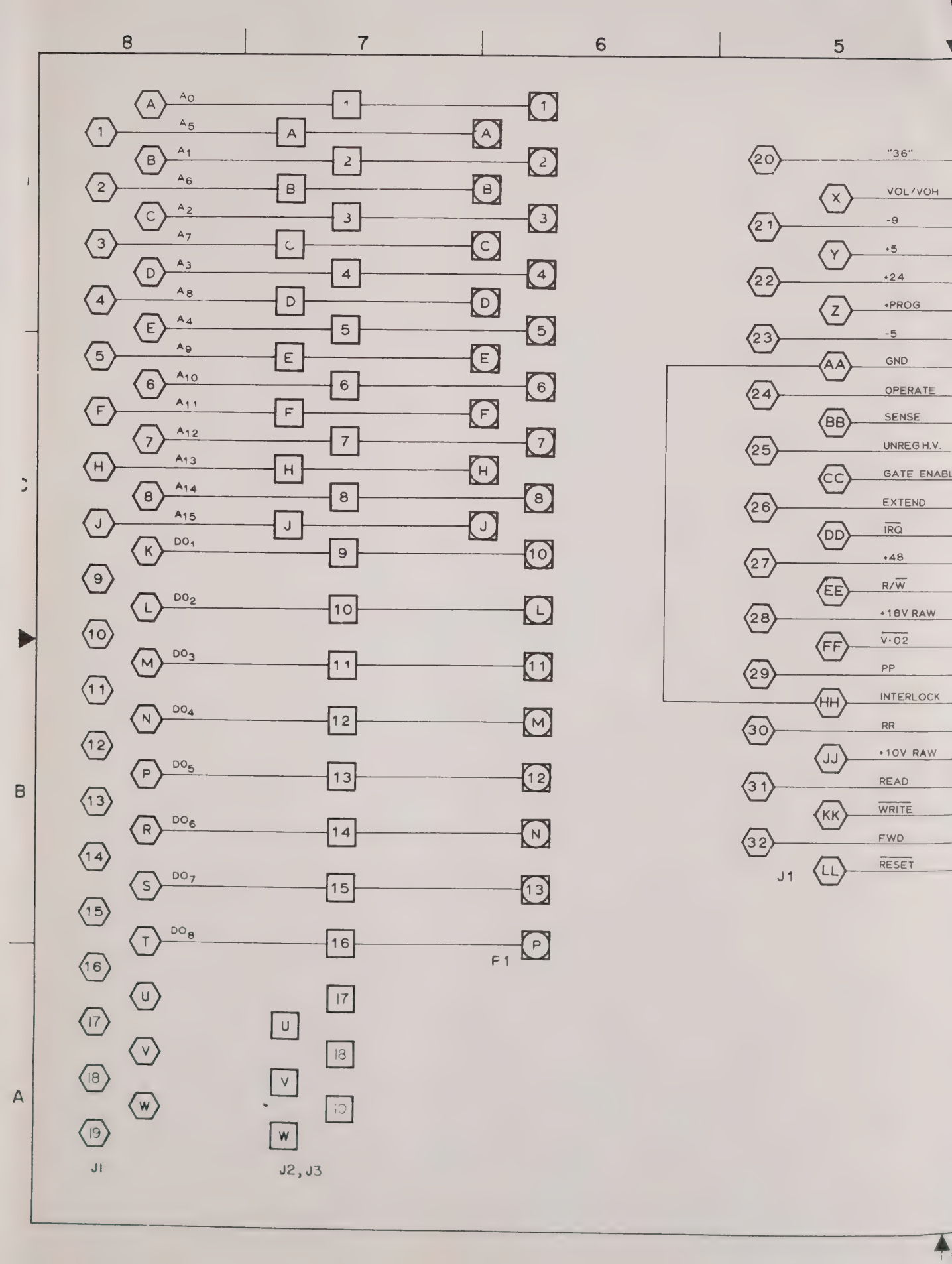
   CR34 U22 RP1 R30 TP1 C22 J1 Q10

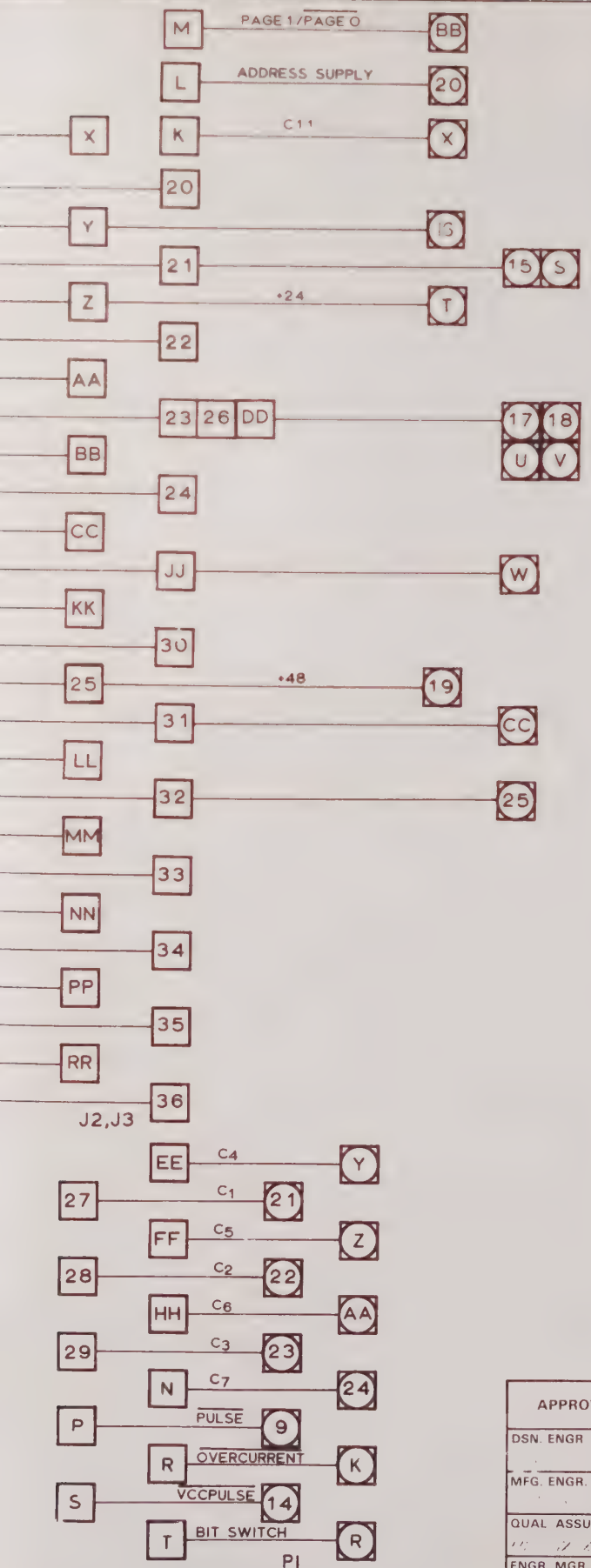
   REFERENCE DESIGNATORS NOT USED:

   U2, U6, U8, U12, U14, U15, U16, U19, R21, C16.

ASSY 702-1659-004 SHOWN.

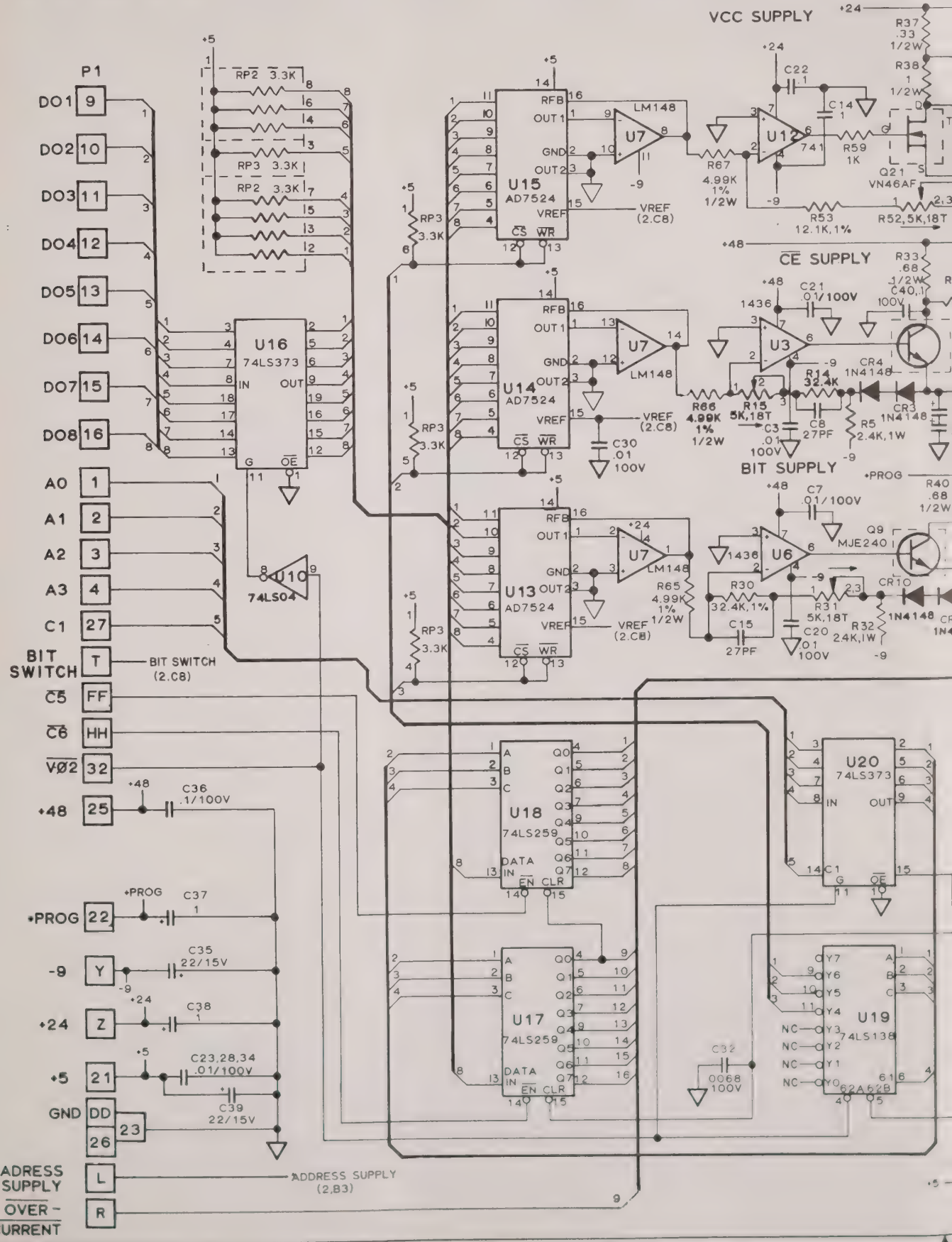
APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
PROJ. ENG. 4/82	TOLERANCES DECIMALS .X ± .XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM SOCKET BD.	
ENG. MGR. 9/82	DO NOT SCALE DRAWING		
Q.C. 1/32	DRAWN BY N Wolfe 12-81	SIZE D	CODE IDENT NO 54193
DATE 1/13/82	CHECKED BY: 9/14/82 BK CHK:	SCALE	DRAWING NO 30-702-1659
			SHEET 1 OF 1

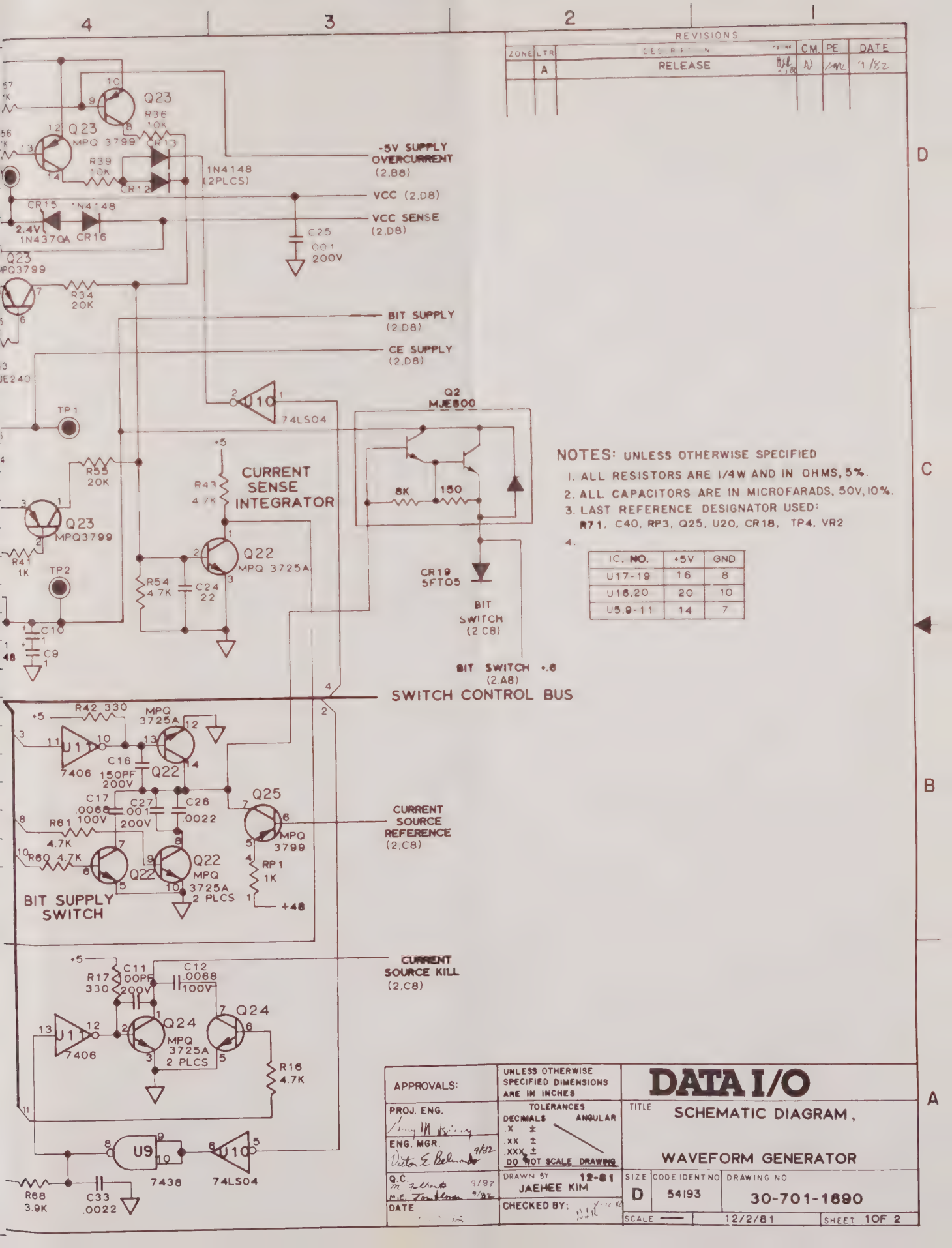

8
7
6
5
A0
A5
A1
A6
A2
A7
A3
A8
A4
A9
A10
A11
A12
A13
A14
A15
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
F1
J1
J2, J3
"36"
VOL/VOH
-9
+5
+24
+PROG
-5
GND
OPERATE
SENSE
UNREG H.V.
GATE ENABL
EXTEND
IRQ
+48
R/W
+18V RAW
V·02
PP
INTERLOCK
RR
+10V RAW
READ
WRITE
FWD
RESET
J1



REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
	RELEASE	R.B.			

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O		
DSN. ENGR	DATE	TOLERANCES, UNLESS OTHERWISE SPECIFIED XX ± .XXX ± ANGULAR	TITLE SCHEMATIC DIAGRAM, MOTHERBOARD		
MFG. ENGR.	DATE				
QUAL. ASSUR.	DATE	DRAWN BY R. BENN	DATE 12-21-81	SIZE D	CODE IDENT NO 54193
ENGR. MGR	DATE	CHECKED BY	DATE	DRAWING NO 30-702-1661	
				SCALE —	SHEET 1 OF 1


VCC SUPPLY
CE SUPPLY
BIT SUPPLY
P1
DO1 9
DO2 10
DO3 11
DO4 12
DO5 13
DO6 14
DO7 15
DO8 16
A0 1
A1 2
A2 3
A3 4
C1 27
BIT SWITCH T
C5 FF
C6 HH
VØ2 32
+48 25
•PROG 22
-9 Y
+24 Z
+5 21
GND DD 26 23
ADRESS SUPPLY L
OVER-CURRENT R
RP2 3.3K
RP3 3.3K
U16 74LS373
U10 74LS04
U15 AD7524
U14 AD7524
U13 AD7524
U7 LM148
U12 741
U3 1436
U6 1436
U18 74LS259
U17 74LS259
U20 74LS373
U19 74LS138
R67 4.99K 1% 1/2W
R66 4.99K 1% 1/2W
R65 4.99K 1% 1/2W
R53 12.1K,1%
R52,5K,18T
R59 1K
R14 32.4K
R15 5K,18T
R5 2.4K,1W
R30 32.4K,1%
R31 5K,18T
R32 2.4K,1W
Q21 VN46AF
Q9 MJE240
CR4 1N4148
CR3 1N4148
CR10 1N4148
C22 1
C14 1
C21 .01/100V
C8 27PF
C3 .01 100V
C30 .01 100V
C7 .01/100V
C15 27PF
C20 .01 100V
C36 .1/100V
C37 1
C35 22/15V
C38 1
C23,28,34 .01/100V
C39 22/15V
C32 0068 100V
VREF (2.C8)
BIT SWITCH (2.C8)
ADDRESS SUPPLY (2,B3)
•PROG
+24
+48
+5
-9



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 50V, 10%.
3. LAST REFERENCE DESIGNATOR USED: R71, C40, RP3, Q25, U20, CR18, TP4, VR2
4.

IC. NO.	+5V	GND
U17-19	16	8
U16,20	20	10
U5,9-11	14	7

APPROVALS:

PROJ. ENG.

ENG. MGR. Victor E. Belmondo 9/82

Q.C. M. Folkerts 9/82 M.E. Tomlinson 9/82

DATE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES
DECIMALS ANGULAR
.X ±
.XX ±
.XXX ±
DO NOT SCALE DRAWING

DRAWN BY 12-81 JAEHEE KIM

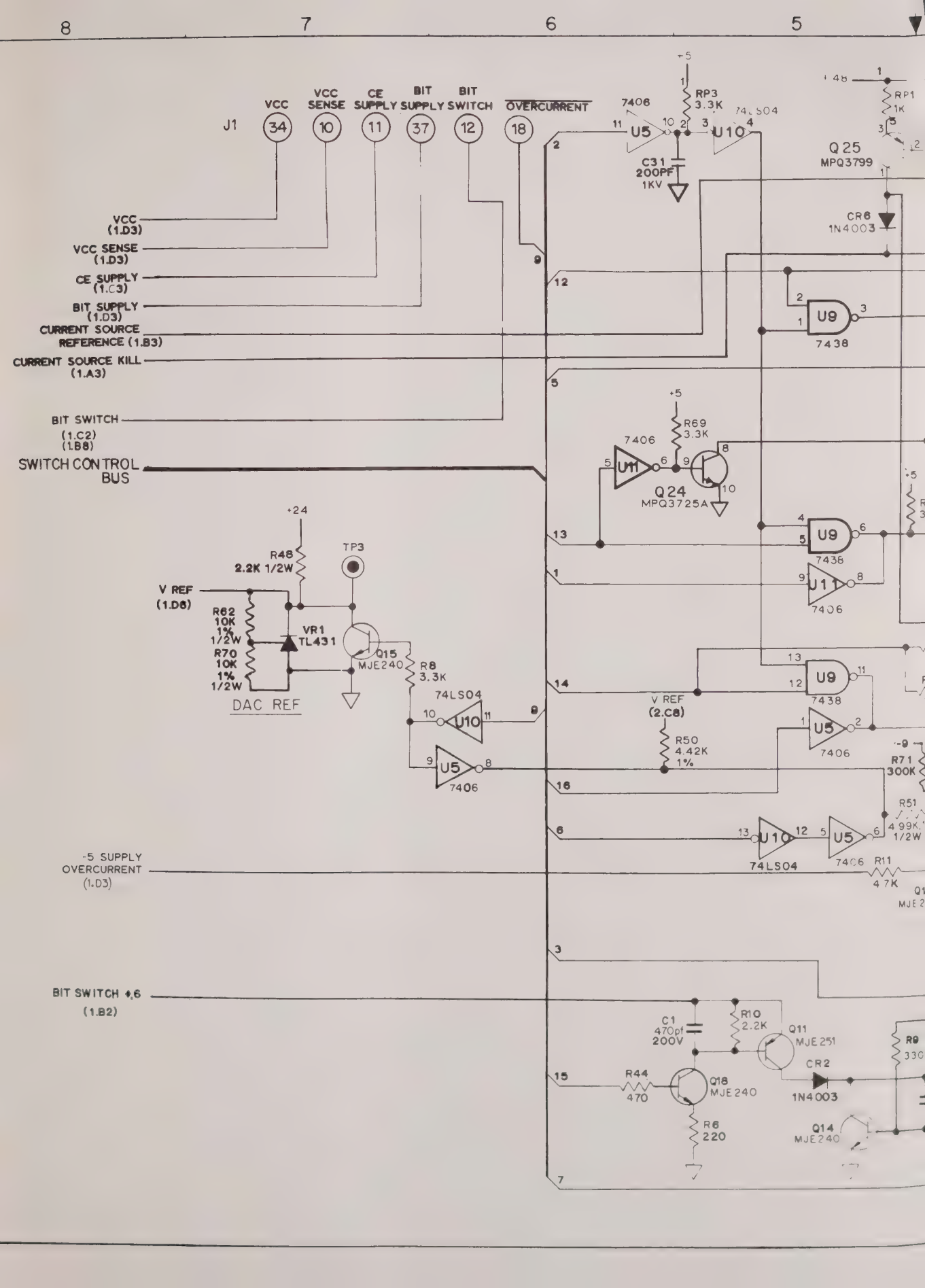
CHECKED BY:

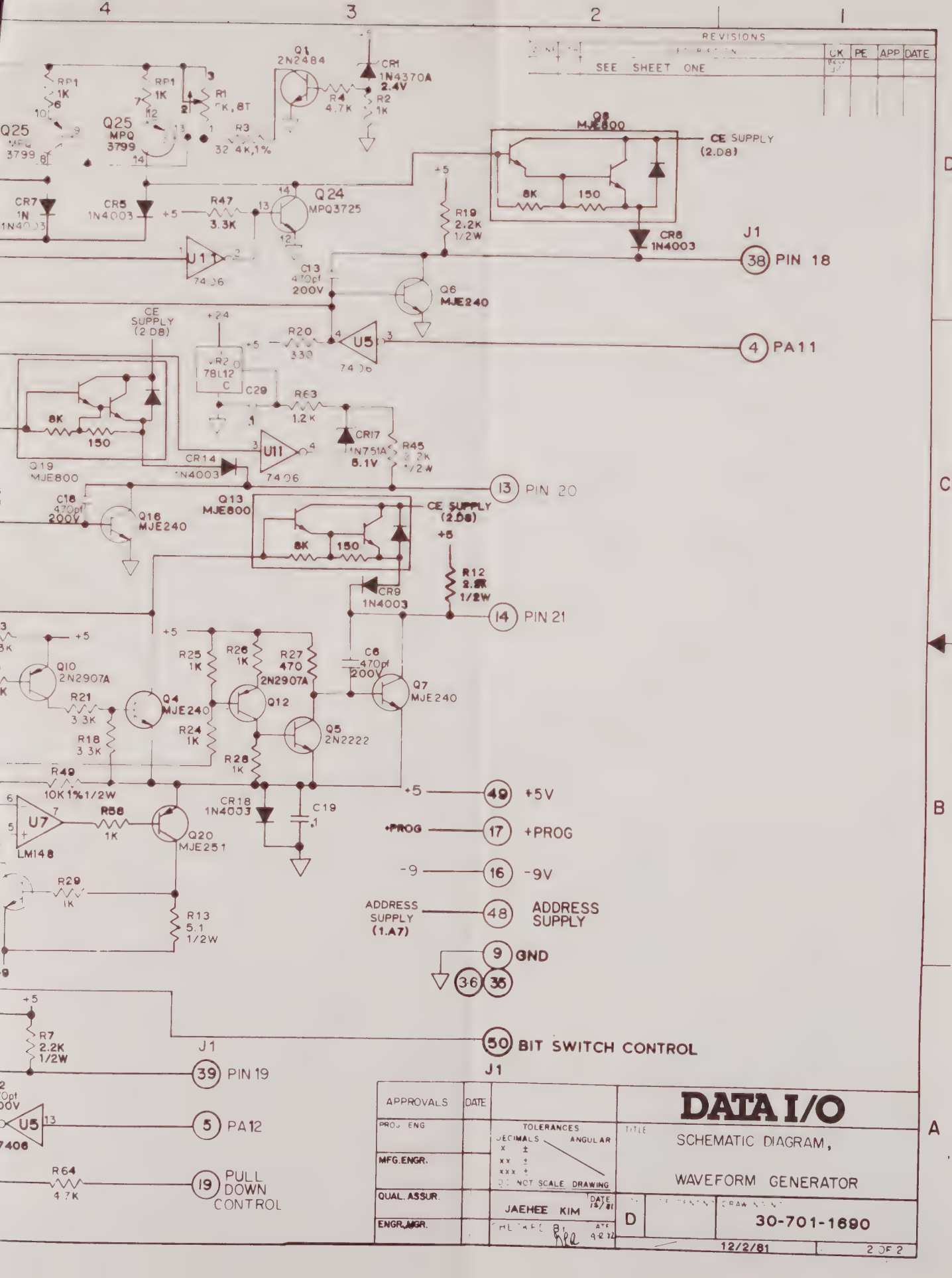
DATA I/O

TITLE SCHEMATIC DIAGRAM, WAVEFORM GENERATOR

SIZE D | CODE IDENT NO 54193 | DRAWING NO 30-701-1690

SCALE — | 12/2/81 | SHEET 1 OF 2


8
7
6
5
J1
VCC
VCC SENSE
CE SUPPLY
BIT SUPPLY
BIT SWITCH
OVERCURRENT
34
10
11
37
12
18
VCC (1.D3)
VCC SENSE (1.D3)
CE SUPPLY (1.C3)
BIT SUPPLY (1.D3)
CURRENT SOURCE REFERENCE (1.B3)
CURRENT SOURCE KILL (1.A3)
BIT SWITCH (1.C2) (1.B8)
SWITCH CONTROL BUS
+5
RP3 3.3K
7406
U5
74LS04
U10
C31 200PF 1KV
RP1 1K
Q25 MPQ3799
CR6 1N4003
U9
7438
R69 3.3K
U11
Q24 MPQ3725A
+24
R48 2.2K 1/2W
TP3
V REF (1.D6)
R62 10K 1% 1/2W
R70 10K 1% 1/2W
VR1 TL431
Q15 MJE240
R8 3.3K
DAC REF
V REF (2.C8)
R50 4.42K 1%
R71 300K
R51 4.99K 1/2W
-5 SUPPLY OVERCURRENT (1.D3)
R11 4.7K
BIT SWITCH 4,6 (1.B2)
C1 470pf 200V
R10 2.2K
Q11 MJE251
CR2 1N4003
R44 470
Q18 MJE240
R6 220
Q14 MJE240
R9 330


REVISIONS
SEE SHEET ONE
CK PE APP DATE
Q1 2N2484
CR1 1N4370A 2.4V
R4 4.7K
R2 1K
RP1 1K
R1 5K, 8T
R3 32.4K, 1%
Q25 MPQ 3799
Q8 MJE800
CE SUPPLY (2.D8)
8K
150
CR7 1N
CR5 1N4003
R47 3.3K
Q24 MPQ3725
R19 2.2K 1/2W
CR8 1N4003
J1
38 PIN 18
U11 7406
C13 470pf 200V
Q6 MJE240
CE SUPPLY (2.D8)
R20 330
U5 7406
4 PA11
VR2 78L12
C29
R63 1.2K
CR17 1N751A 5.1V
R45 2.2K 1/2W
Q19 MJE800
CR14 1N4003
13 PIN 20
C18 470pf 200V
Q16 MJE240
Q13 MJE800
CE SUPPLY (2.D8)
R12 2.2K 1/2W
CR9 1N4003
14 PIN 21
Q10 2N2907A
R21 3.3K
R18 3.3K
Q4 MJE240
R25 1K
R26 1K
R27 470
2N2907A
Q12
R24 1K
R28 1K
Q5 2N2222
C6 470pf 200V
Q7 MJE240
R49 10K 1% 1/2W
U7 LM148
R58 1K
Q20 MJE251
CR18 1N4003
C19 .1
+5 49 +5V
+PROG 17 +PROG
-9 16 -9V
ADDRESS SUPPLY (1.A7) 48 ADDRESS SUPPLY
9 GND
36 35
R29 1K
R13 5.1 1/2W
R7 2.2K 1/2W
50 BIT SWITCH CONTROL
J1
39 PIN 19
U5 7406
5 PA12
R64 4.7K
19 PULL DOWN CONTROL
APPROVALS
DATE
PROJ. ENG.
MFG. ENGR.
QUAL. ASSUR.
ENGR. MGR.
TOLERANCES
DECIMALS ANGULAR
DO NOT SCALE DRAWING
JAEHEE KIM
DATA I/O
TITLE
SCHEMATIC DIAGRAM,
WAVEFORM GENERATOR
D
30-701-1690
12/2/81
2 OF 2

.S. Sales Offices and Representatives
irect Sales and Service Offices

ata I/O Corporation
1525 Willows Road N.E.
O. Box 97046
edmond, WA 98073-9746
06) 881-6444
lex Dom. 15-2167,
t'l. 4740166 DIO UI

ORTHWEST REGION

ata I/O Corporation
00 Wyatt Drive
uite 1
anta Clara, CA 95054
08) 727-0641

OUTHWEST REGION

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70 South Harbor Blvd.
uite K
anta Ana, CA 92704
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14) 662-2498 *(Service)*
lex 755870

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oute 101A
mherst, NH 03031
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03) 889-8513 *(Service)*
lex 943431

ENTRAL REGION

ata I/O Corporation
310 N. Glenville Drive
uite 108
ichardson, TX 75081
214) 235-0044
elex 792474

epresentatives

LASKA, WASHINGTON
RI-CITIES, VANCOUVER),
OREGON

lorthwest Test and
Measurement
1196 Southwest Hall
Suite 217
Beaverton, OR 97005
503) 646-9966
-800-247-5700
Telex 910-467-8775

WESTERN WASHINGTON,
SPOKANE

Northwest Test and
Measurement
4020 148th Ave. N.E.
Suite F
Redmond, WA 98052
(206) 881-8857

ARKANSAS, LOUISIANA, OKLAHOMA, TEXAS

TESTECH, Inc.
1000 E. Campbell Road
Suite 108
Richardson, TX 75081
(214) 644-5010

4800 West 34th St.
Suite D-6
Houston, TX 77092
(713) 956-0837

1715 Capital of Texas Hwy S.
Suite 107
Austin, TX 78746
(512) 327-7033

OHIO

Electro Sales Associates
1635 Mardon Drive
Dayton, OH 45432
(513) 426-5551

26250 Euclid Avenue
Suite 331
Cleveland, OH 44132
(216) 261-5440

MICHIGAN

Electro Sales Associates
29200 Vassar Road
Suite 505
Livonia, MI 48152
(313) 474-7320

9816 Portage Road
Portage, MI 49002
(616) 323-2416

PENNSYLVANIA, WEST VIRGINIA, EASTERN KENTUCKY

Electro Sales Associates
3740 Mount Royal Blvd.
Allison Park, PA 15101
(412) 487-3801

UPSTATE NEW YORK

DB Associates, Inc.
7000 E. Genesee Street
Building D
Fayetteville, NY 13066
(315) 446-0220

KANSAS, NEBRASKA

Midtec Associates, Inc.
7702 Mize Road
DeSoto, KS 66018
(913) 441-6565
Telex 910-743-4129

MISSOURI

Midtec Associates, Inc.
8460 Lindbergh North
Suite 11
Florissant, MO 63031
(314) 837-5200

FLORIDA

Pen Tech Associates
201 S.E. 15th Terrace
Suite K
Deerfield Beach, FL 33441
(305) 421-4989

1398 Semoran Blvd.
Suite 106
Casselberry, FL 32707
(305) 645-3444

GEORGIA, TENNESSEE

Pen Tech Associates
627 Cherokee Street
Suite 21
Marietta, GA 30060
(404) 424-1931

NORTHERN FLORIDA, ALABAMA, TENNESSEE, MISSISSIPPI

Pen Tech Associates
3322 Memorial Pkwy. S.W.
Suite 36
Huntsville, AL 35801
(205) 881-9298

NORTH CAROLINA, SOUTH CAROLINA

Pen Tech Associates
3709 Alliance Drive
Suite C
Greensboro, NC 27407
(919) 852-6000

MINNESOTA, NORTH DAKOTA, SOUTH DAKOTA

Torkelson Associates
4940 Viking Drive
Minneapolis, MN 55435
(612) 835-2414
Telex 910-576-2740

NORTHERN ILLINOIS, IOWA, INDIANA

Torkelson Associates
108 Wilmot Road, Suite 110
Deerfield, IL 60015
(312) 945-8700
Telex 910-992-1438

INDIANA, WESTERN KENTUCKY

Torkelson Associates
2346 S. Lynhurst
Room B101
Indianapolis, IN 46241
(317) 244-7867
Telex 810-341-3141

WISCONSIN

Torkelson Associates
2840 N. Brookfield Road
Brookfield, WI 53005
(414) 784-7736

ARIZONA, NEVADA

Zeus Electronics, Inc.
1428 E. Pierson Street
Phoenix, AZ 85014
(602) 263-6022
1-800-528-4512
Telex 910-951-1362

NEW MEXICO, EL PASO CO., TEXAS

Zeus Electronics, Inc.
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